Si5334

Pin-Controlled Any-Frequency, Any-Output Quad Clock Generator

Features

- Low-power MultiSynth technology enables independent, any-frequency synthesis on four differential output drivers
- Highly-configurable output drivers support up to four differential outputs or eight single-ended clock outputs or a combination of both
- Low phase jitter: 0.7 ps RMS typ
- High-precision synthesis allows true 0 ppm frequency accuracy on all outputs
- Flexible input reference
  - External crystal: 8 to 30 MHz
  - CMOS input: 5 to 200 MHz
  - SSTL/HSTL input: 5 to 350 MHz
  - Differential input: 5 to 710 MHz
- Independently-configurable outputs support any frequency or format
  - LVPECL/LVDS: 0.16 to 710 MHz
  - HCSL: 0.16 to 250 MHz
  - CMOS: 0.16 to 200 MHz
  - SSTL/HSTL: 0.16 to 350 MHz
- Independent output voltage per driver
  - 1.5, 1.8, 2.5, or 3.3 V
- Independent core supply voltage
  - 1.8, 2.5, or 3.3 V
- Frequency increment/decrement feature enables glitchless frequency adjustments in 1 ppm steps
- Phase adjustment on each of the output drivers with <20 ps steps
- SSC on any or all outputs that is compliant to PCI Express
- Optional external feedback mode allows zero-delay implementation
- Loss-of-lock and loss-of-signal alarm
- Simple pin control
- Small size: 4x4 mm, 24-QFN
- Low power: 45 mA core supply typ
- Wide temperature range: –40 to +85 °C
- Contact Skyworks Solutions for custom versions

Applications

- Ethernet switch/router
- PCI Express 2.0/3.0
- Broadcast video/audio timing
- Processor and FPGA clocking
- Any-frequency clock conversion
- MSAN/DSLAM/PON
- Fibre Channel, SAN
- Telecom line cards
- 1 GbE and 10 GbE

Description

The Si5334 is a high performance, low jitter clock generator capable of synthesizing any frequency on each of the device's four differential output clocks. The device accepts an external reference clock or crystal and generates four differential clock outputs, each of which is independently configurable to any frequency up to 350 MHz and select frequencies to 710 MHz. Using Skyworks Solutions' patented MultiSynth technology, each output clock is generated with very low jitter and zero ppm frequency error. To provide additional design flexibility, each output clock is independently configurable to support any signal format and reference voltage. The Si5334 provides low jitter frequency synthesis with outstanding frequency flexibility in a space-saving 4 x 4 mm QFN package. The device configuration is factory or field programmed and, upon power up, the device will begin operation in the predefined configuration without user intervention. The device supports operation from a 1.8, 2.5, or 3.3 V core supply.

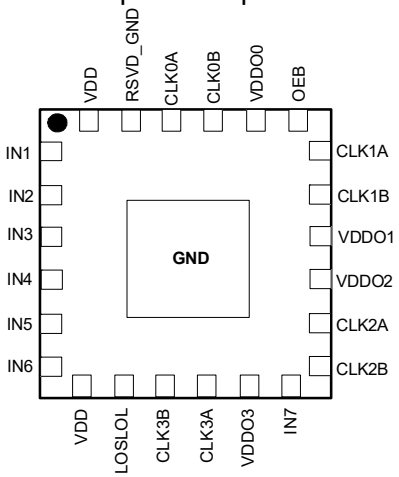


Ordering Information:

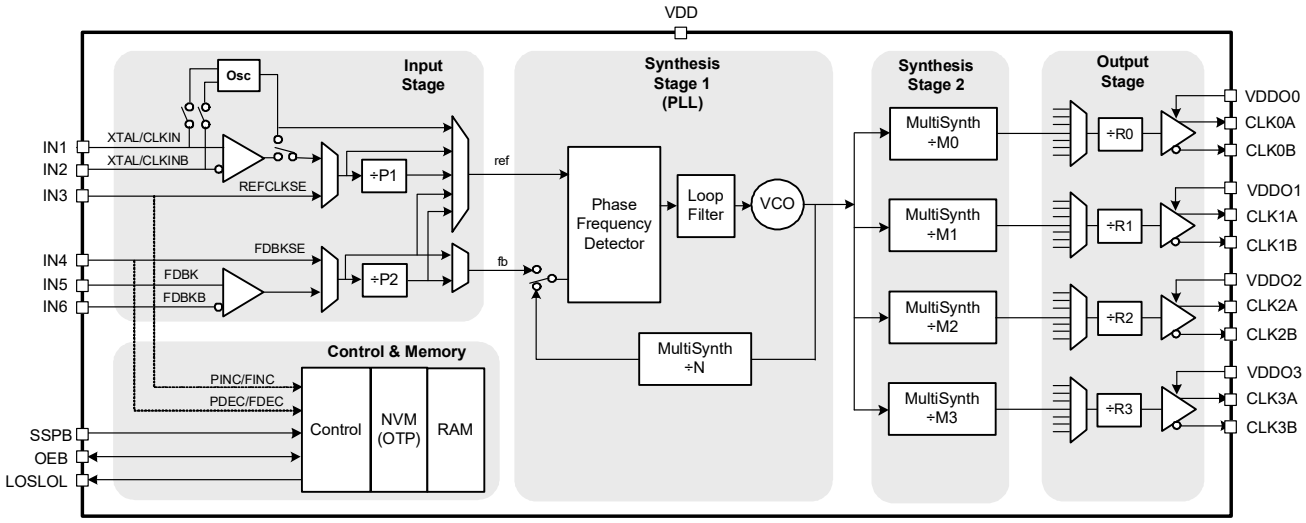
See page 32.

Pin Assignments

Si5334
Transparent Top View



Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.98	V
Output Buffer Supply Voltage	V_{DDOn}		1.4	—	3.63	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current	I_{DD}	100 MHz on all outputs, 25 MHz refclk	—	45	60	mA
Core Supply Current (Buffer Mode)	I_{DDB}	50 MHz refclk	—	12	—	mA
Output Buffer Supply Current	I_{DDOx}	LVPECL, 710 MHz	—	—	30	mA
		LVDS, 710 MHz	—	—	8	mA
		HCSL, 250 MHz 2 pF load	—	—	20	mA
		CML, 350 MHz	—	12	—	mA
		SSTL, 350 MHz	—	—	19	mA
		CMOS, 50 MHz 15 pF load[1]	—	6	9	mA
		CMOS, 200 MHz[1,2] 3.3 V VDD0	—	13	18	mA
		CMOS, 200 MHz[1,2] 2.5 V	—	10	14	mA
		CMOS, 200 MHz[1,2] 1.8 V	—	7	10	mA
		HSTL, 350 MHz	—	—	19	mA

Notes:
1. Single CMOS driver active.
2. Measured into a 5” 50 Ω trace with 2 pF load.

Table 3. Performance Characteristics
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Acquisition Time	t_{ACQ}		—	—	25	ms
PLL Tracking Range	f_{TRACK}		5000	20,000	—	ppm
PLL Loop Bandwidth	f_{BW}		—	1.6	—	MHz
MultiSynth Frequency Synthesis Resolution	f_{RES}	Output frequency ≤ Fvco/8	0	0	1	ppb
CLKIN Loss of Signal Assert Time	t_{LOS}		—	2.6	5	µs
CLKIN Loss of Signal Deassert Time	t_{LOS_b}		0.01	0.2	1	µs
PLL Loss of Lock Detect Time	t_{LOL}		—	5	10	ms
POR to Output Clock Valid	t_{RDY}		—	—	2	ms
Input-to-Output Propagation Delay	t_{PROP}	Buffer Mode (PLL Bypass)	—	2.5	4	ns
Output-Output Skew	t_{DSKEW}	Rn divider = 1[1]	—	—	100	ps
Programmable Initial Phase Offset	P_{OFFSET}		–45	—	+45	ns
Phase Increment/Decrement Accuracy	P_{STEP}		—	—	20	ps
Phase Increment/Decrement Range	P_{RANGE}		–45	—	+45	ns
Frequency range for phase increment/decrement	f_{PRANGE}		—	—	350[2]	MHz
Phase Increment/Decrement Update Rate	P_{UPDATE}	Pin control	—	—	1500	kHz
Frequency Increment/Decrement Step Size	f_{STEP}	R divider not used[3]	1	—	See Note [3]	ppm
Frequency Increment/Decrement Range	f_{RANGE}	R divider not used[3]	—	—	350[2]	MHz
Frequency Increment/Decrement Update Rate	f_{UPDATE}	Pin control[2,3]	—	—	1500	kHz

Notes:
1. Outputs at integer-related frequencies and using the same driver format.
2. Keep MultiSynth output frequency between 5 MHz to Fvco/8.
3. Only MultiSynth0 can have frequency inc/dec but MultiSynth0 can be routed to any output.
4. Spread spectrum is only available on clock outputs that are at 100 MHz and have the Rn divider set to 1.

Table 3. Performance Characteristics (Continued)

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spread Spectrum PP Frequency Deviation	SS_{DEV}	Clock frequency of 100 MHz[4]	—	–0.5	—	%
Spread Spectrum Modulation Rate	SS_{DEV}	Clock frequency of 100 MHz	30	—	33	kHz

Notes:
1. Outputs at integer-related frequencies and using the same driver format.
2. Keep MultiSynth output frequency between 5 MHz to Fvco/8.
3. Only MultiSynth0 can have frequency inc/dec but MultiSynth0 can be routed to any output.
4. Spread spectrum is only available on clock outputs that are at 100 MHz and have the Rn divider set to 1.

Table 4. Input and Output Clock Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC Coupled Differential Input Clocks on Pins IN1/2, IN5/6)[1]						
Frequency	f_{IN}		5	—	710	MHz
Differential Voltage Swing	V_{PP}	710 MHz input	0.4	—	2.4	V_{PP}
Rise/Fall Time[2]	t_R/t_F	20%–80%	—	—	1.0	ns
Duty Cycle	DC	< 1 ns tr/tf	40	—	60	%
Input Impedance[1]	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		—	3.5	—	pF
Input Clock (DC-coupled Single-Ended Input Clock on Pins IN3/4)						
Frequency	f_{IN}	CMOS	5	—	200	MHz
Input Voltage	V_I		–0.1	—	3.73	V_{PP}
Input Voltage Swing		200 MHz	0.8	—	V_{DD} + 10%	V_{PP}
Rise/Fall Time[3]	t_R/t_F	10%–90%	—	—	4	ns
Rise/Fall Time[3]	t_R/t_F	20%–80%	—	—	2.3	ns
Duty Cycle	DC	< 2 ns tr/tf	40	—	60	%
Input Capacitance	C_{IN}		—	2.0	—	pF
Output Clocks (Differential)						

Notes:
1. Use an external 100 Ω resistor to provide load termination for a differential clock. See "2.2. Crystal/Clock Input" on page 15.
2. For best jitter performance, keep the input slew rate on IN1/2, IN5/6 faster than 0.3 V/ns.
3. For best jitter performance, keep the input single ended slew rate on pins 3 or 4 faster than 1 V/ns.
4. Only two unique frequencies above Fvco/8 can be simultaneously output, Fvco/4 and Fvco/6.
5. CML output format requires ac-coupling of the differential outputs to a differential 100 Ω load at the receiver.
6. Includes effect of internal series 22 Ω resistor.

Table 4. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency[4]	f_{OUT}	LVPECL, LVDS	0.16	—	350	MHz
			367	—	473.33	MHz
			550	—	710	MHz
		HCSL	0.16	—	250	MHz
LVPECL Output Voltage	V_{OC}	common mode	—	V_{DDO} – 1.45 V	—	V
	V_{SEPP}	peak-to-peak single-ended swing	0.55	0.8	0.96	V_{PP}
LVDS Output Voltage (2.5/3.3 V)	V_{OC}	common mode	1.125	1.2	1.275	V
	V_{SEPP}	peak-to-peak single-ended swing	0.25	0.35	0.45	V_{PP}
LVDS Output Voltage (1.8 V)	V_{OC}	common mode	0.8	0.875	0.95	V
	V_{SEPP}	peak-to-peak single-ended swing	0.25	0.35	0.45	V_{PP}
HCSL Output Voltage	V_{OC}	common mode	0.35	0.375	0.400	V
	V_{SEPP}	peak-to-peak single-ended swing	0.575	0.725	0.85	V_{PP}
CML Output Voltage	V_{OC}	Common Mode	—	See Note [5]	—	V
	V_{SEPP}	Peak-to-Peak Single-ended Swing	0.67	0.860	1.07	V_{PP}
Rise/Fall Time	t_R/t_F	20%–80%	—	—	450	ps
Duty Cycle	DC		45	—	55	%
Output Clocks (Single-Ended)						
Frequency	f_{OUT}	CMOS	0.16	—	200	MHz
		SSTL, HSTL	0.16	—	350	MHz
CMOS 20%–80% Rise/Fall Time	t_R/t_F	2 pF load	—	0.45	0.85	ns
CMOS 20%–80% Rise/Fall Time	t_R/t_F	15 pF load	—	—	2.0	ns

Notes:
1. Use an external 100 Ω resistor to provide load termination for a differential clock. See "2.2. Crystal/Clock Input" on page 15.
2. For best jitter performance, keep the input slew rate on IN1/2, IN5/6 faster than 0.3 V/ns.
3. For best jitter performance, keep the input single ended slew rate on pins 3 or 4 faster than 1 V/ns.
4. Only two unique frequencies above Fvco/8 can be simultaneously output, Fvco/4 and Fvco/6.
5. CML output format requires ac-coupling of the differential outputs to a differential 100 Ω load at the receiver.
6. Includes effect of internal series 22 Ω resistor.

Table 4. Input and Output Clock Characteristics (Continued)
(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CMOS Output Resistance		See Note 6	—	50	—	Ω
SSTL Output Resistance			—	50	—	Ω
HSTL Output Resistance			—	50	—	Ω
CMOS Output Voltage[6]	V_{OH}	4 mA load	VDDO – 0.3	—		V
	V_{OL}	4 mA load		—	0.3	V
SSTL Output Voltage	V_{OH}	SSTL-3 VDDOx = 2.97 to 3.63 V	0.45xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.45xVDDO–0.41	V
	V_{OH}	SSTL-2 VDDOx = 2.25 to 2.75 V	0.5xVDDO+0.41	—	—	V
	V_{OL}		—	—	0.5xVDDO–0.41	V
	V_{OH}	SSTL-18 VDDOx = 1.71 to 1.98 V	0.5xVDDO+0.34	—		V
	V_{OL}		—	—	0.5xVDDO–0.34	V
HSTL Output Voltage	V_{OH}	VDDO = 1.4 to 1.6 V	0.5xVDDO+0.3	—	—	V
	V_{OL}		—	—	0.5xVDDO –0.3	V
Duty Cycle	DC		45	—	55	%

Notes:
1. Use an external 100 Ω resistor to provide load termination for a differential clock. See "2.2. Crystal/Clock Input" on page 15.
2. For best jitter performance, keep the input slew rate on IN1/2, IN5/6 faster than 0.3 V/ns.
3. For best jitter performance, keep the input single ended slew rate on pins 3 or 4 faster than 1 V/ns.
4. Only two unique frequencies above Fvco/8 can be simultaneously output, Fvco/4 and Fvco/6.
5. CML output format requires ac-coupling of the differential outputs to a differential 100 Ω load at the receiver.
6. Includes effect of internal series 22 Ω resistor.

Table 5. Control Pins

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Control Pins (IN3, IN4)						
Input Voltage Low	V_{IL}		–0.1	—	0.3 x V_{DD}	V
Input Voltage High	V_{IH}		0.7 x V_{DD}	—	3.73	V
Input Capacitance	C_{IN}		—	—	4	pF
Input Resistance	R_{IN}		—	20	—	kΩ
Output Control Pins (LOSLOL)						
Output Voltage Low	V_{OL}	I_{SINK} = 3 mA	0	—	0.4	V
Rise/Fall Time 20–80%	t_R/t_F	C_L < 10 pf, pull up = 1 kΩ	—	—	10	ns

Table 6. Crystal Specifications for 8 to 11 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	8	—	11	MHz
Load Capacitance (on-chip differential)	c_L (supported)*	11	12	13	pF
	c_L (recommended)	17	18	19	pF
Crystal Output Capacitance	c_O	—	—	6	pF
Equivalent Series Resistance	r_{ESR}	—	—	300	Ω
Crystal Max Drive Level	d_L	100	—	—	µW
***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for more information.					

Table 7. Crystal Specifications for 11 to 19 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	11	—	19	MHz
Load Capacitance (on-chip differential)	c_L (supported)*	11	12	13	pF
	c_L (recommended)	17	18	19	pF
Crystal Output Capacitance	c_O	—	—	5	pF
Equivalent Series Resistance	r_{ESR}	—	—	200	Ω
Crystal Max Drive Level	d_L	100	—	—	µW
***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for more information.					

Table 8. Crystal Specifications for 19 to 26 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	19		26	MHz
Load Capacitance (on-chip differential)	c_L (supported)*	11	12	13	pF
	c_L (recommended)	17	18	19	pF
Crystal Output Capacitance	c_O			5	pF
Equivalent Series Resistance	r_{ESR}			100	Ω
Crystal Max Drive Level	d_L	100			µW
***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for more information.					

Table 9. Crystal Specifications for 26 to 30 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	26		30	MHz
Load Capacitance (on-chip differential)	c_L (supported)*	11	12	13	pF
	c_L (recommended)	17	18	19	pF
Crystal Output Capacitance	c_O			5	pF
Equivalent Series Resistance	r_{ESR}			75	Ω
Crystal Max Drive Level	d_L	100			µW
***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for more information.					

Table 10. Jitter Specifications[1,2,3]

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
GbE Random Jitter (12 kHz–20 MHz)[4]	J_{GbE}	CLKIN = 25 MHz All CLKn at 125 MHz[5]	—	0.7	1	ps RMS
GbE Random Jitter (1.875–20 MHz)	R_{JGbE}	CLKIN = 25 MHz All CLKn at 125 MHz[5]	—	0.38	0.79	ps RMS
OC-12 Random Jitter (12 kHz–5 MHz)	J_{OC12}	CLKIN = 19.44 MHz All CLKn at 155.52 MHz[5]	—	0.7	1	ps RMS
PCI Express 1.1 Common Clocked		Total Jitter[6]	—	20.1	33.6	ps pk-pk
PCI Express 2.1 Common Clocked		RMS Jitter[6], 10 kHz to 1.5 MHz	—	0.15	1.47	ps RMS
		RMS Jitter[6], 1.5 MHz to 50 MHz	—	0.58	0.75	ps RMS
PCI Express 3.0 Common Clocked		RMS Jitter[6]	—	0.15	0.45	ps RMS
Period Jitter	J_{PER}	N = 10,000 cycles[7]	—	10	30	ps pk-pk
Cycle-Cycle Jitter	J_{CC}	N = 10,000 cycles Output MultiSynth operated in integer or fractional mode[7]	—	9	29	ps pk[8]
Random Jitter (12 kHz–20 MHz)	R_J	Output and feedback MultiSynth in integer or fractional mode[7]	—	0.7	1.5	ps RMS

Notes:

1. All jitter measurements apply for LVDS/HCSL/LVPECL output format with a low noise differential input clock and are made with an Agilent 90804 oscilloscope. All RJ measurements use RJ/DJ separation.
2. For best jitter performance, keep the single ended clock input slew rates at Pins 3 and 4 more than 1.0 V/ns and the differential clock input slew rates more than 0.3 V/ns.
3. All jitter data in this table is based upon all output formats being differential. When single-ended outputs are used, there is the potential that the output jitter may increase due to the nature of single-ended outputs. If your configuration implements any single-ended output and any output is required to have jitter less than 3 ps rms, contact Skyworks Solutions for support to validate your configuration and ensure the best jitter performance. In many configurations, CMOS outputs have little to no effect upon jitter.
4. D_J for PCI and GbE is < 5 ps pp
5. Output MultiSynth in Integer mode.
6. All output clocks 100 MHz HCSL format. Jitter is from the PCIE jitter filter combination that produces the highest jitter. See AN562 for details. Jitter is measured with the Intel Clock Jitter Tool, Ver.1.6.4.
7. Input frequency to the Phase Detector between 25 and 40 MHz and any output frequency $\geq$ 5 MHz.
8. Measured in accordance with JEDEC standard 65.
9. Rj is multiplied by 14; estimate the pp jitter from Rj over 2^{12} rising edges.

Table 10. Jitter Specifications[1,2,3] (Continued)

(V_{DD} = 1.8 V –5% to +10%, 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Deterministic Jitter	D_J	Output MultiSynth operated in fractional mode[7]	—	3	15	ps pk-pk
		Output MultiSynth operated in integer mode[7]	—	2	10	ps pk-pk
Total Jitter (12 kHz–20 MHz)	$T_J = D_J+14xR_J$ (See Note [9])	Output MultiSynth operated in fractional mode[7]	—	13	36	ps pk-pk
		Output MultiSynth operated in integer mode[7]	—	12	20	ps pk-pk

Notes:

1. All jitter measurements apply for LVDS/HCSL/LVPECL output format with a low noise differential input clock and are made with an Agilent 90804 oscilloscope. All RJ measurements use RJ/DJ separation.
2. For best jitter performance, keep the single ended clock input slew rates at Pins 3 and 4 more than 1.0 V/ns and the differential clock input slew rates more than 0.3 V/ns.
3. All jitter data in this table is based upon all output formats being differential. When single-ended outputs are used, there is the potential that the output jitter may increase due to the nature of single-ended outputs. If your configuration implements any single-ended output and any output is required to have jitter less than 3 ps rms, contact Skyworks Solutions for support to validate your configuration and ensure the best jitter performance. In many configurations, CMOS outputs have little to no effect upon jitter.
4. D_J for PCI and GbE is < 5 ps pp
5. Output MultiSynth in Integer mode.
6. All output clocks 100 MHz HCSL format. Jitter is from the PCIE jitter filter combination that produces the highest jitter. See AN562 for details. Jitter is measured with the Intel Clock Jitter Tool, Ver.1.6.4.
7. Input frequency to the Phase Detector between 25 and 40 MHz and any output frequency $\geq$ 5 MHz.
8. Measured in accordance with JEDEC standard 65.
9. Rj is multiplied by 14; estimate the pp jitter from Rj over 2^{12} rising edges.

Table 11. Typical Phase Noise Performance

Offset Frequency	25MHz XTAL to 156.25 MHz	27 MHz Ref In to 148.3517 MHz	19.44 MHz Ref In to 155.52 MHz	Units
100 Hz	–90	–87	–110	dBc/Hz
1 kHz	–120	–117	–116	dBc/Hz
10 kHz	–126	–123	–123	dBc/Hz
100 kHz	–132	–130	–128	dBc/Hz
1 MHz	–132	–132	–128	dBc/Hz
10 MHz	–145	–145	–145	dBc/Hz

Table 12. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	37	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	25	°C/W

Table 13. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
Storage Temperature Range	T_{STG}		–55 to 150	°C
ESD Tolerance		HBM (100 pF, 1.5 kΩ)	2.5	kV
ESD Tolerance		CDM	550	V
ESD Tolerance		MM	175	V
Latch-up Tolerance			JESD78 Compliant	
Junction Temperature	T_J		150	°C
Peak Soldering Reflow Temperature[2]			260	°C

Notes:
1. Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Refer to JEDEC J-STD-020 standard for more information.

2. Functional Description

2.1. Overview

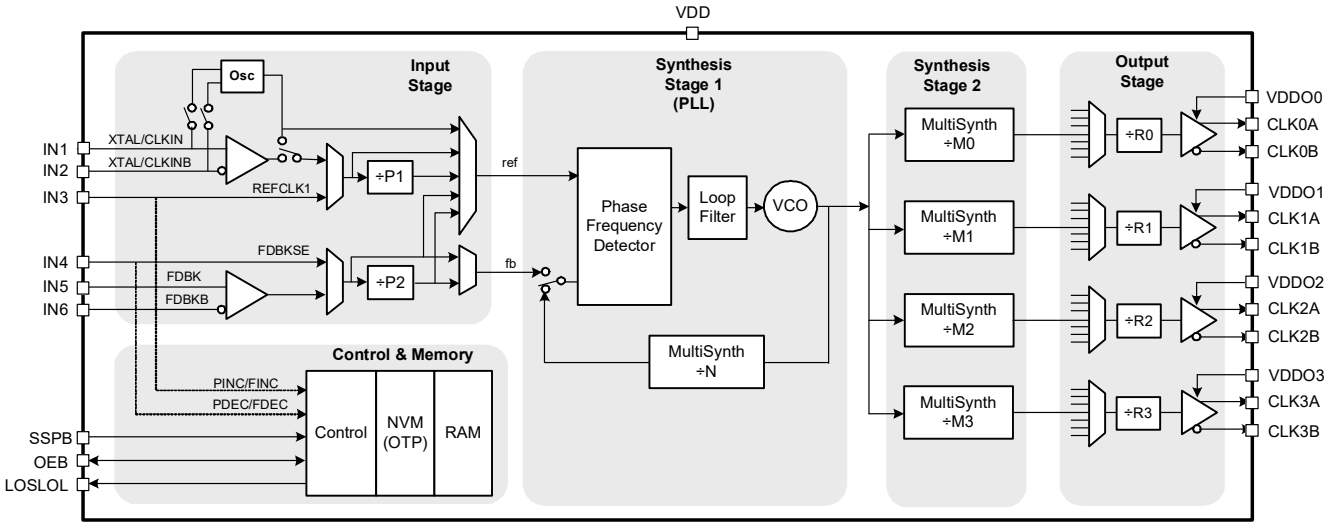


Figure 1. Si5334 Block Diagram

The Si5334 is a high-performance, low-jitter clock generator capable of synthesizing any frequency on each of the device's four differential output clocks. The device accepts an external crystal from 8 to 30 MHz or an input clock ranging from 5 to 710 MHz. Each output is independently factory-programmable to any frequency up to Fvco/8 (max of 350 MHz) and select frequencies to 710 MHz.

The Si5334 fractional-N PLL, comprised of a phase detector, charge pump, loop filter, VCO, and dividers, is fully integrated on chip to simplify design. Using Skyworks Solutions' patented MultiSynth technology, each output clock is generated with low jitter and zero ppm frequency error. The device has four MultiSynth output dividers to provide non-integer frequency synthesis on every differential output clock.

The Si5334 output driver is highly flexible. The signal format of each output clock can be user-specified to support LVPECL, LVDS, HCSL, CMOS, HSTL, or SSTL. Each output clock has its own supply voltage to allow for the utmost flexibility in mixed supply operations. The core of the Si5334 has its own supply voltage that can be 1.8, 2.5, or 3.3 V.

The Si5334 supports an optional zero delay mode of operation. In this mode, one of the device output clocks is fed back to the FDBK/FDBKB clock input pins to implement the PLL feedback path and nullify the phase difference between the reference input and the output clocks.

The Si5334D/E/F has a pin-controlled phase increment/decrement feature that allows the user to adjust the phase of each output clock in relation to the other output clocks. The phase of each differential output clock can be set to an accuracy of 20 ps over a range of ±45 ns. This feature is available over the 0.16 to Fvco/8 MHz frequency range at a maximum rate of phase change of 1.5 MHz.

The Si5334G/H/J has a pin-controlled frequency increment/decrement feature that allows the user to change frequency in steps as small as 1 ppm of the initial frequency to as large as possible as long as the frequency at the output of the MultiSynth stays within the range of 5 MHz to Fvco/8 MHz. This feature is available on CLK0A/B only. The frequency step is glitchless. This feature is useful in applications that require a variable clock frequency. It can also be used in frequency margining applications to margin test system clocks during design/verification/test or manufacturing test applications.

For EMI reduction, the Si5334K/L/M supports PCI Express 2.0 compliant spread spectrum on all output clocks that are 100 MHz.

The Si5334 is pin-controlled. No I^2C interface is provided. The LOLLOS output pin indicates the lock condition of the PLL. An output enable input pin is available on the Si5334A/B/C which affects all the programmed clock outputs. All device specifications are guaranteed across these three core supply voltages. Packaged in a ROHS-6, Pb-free 4x4 mm QFN package, the device supports the industrial temperature range of –40 to +85 °C.

After core power is applied, the Si5334 downloads the factory-programmed NVM into RAM and begins operation.

2.2. Crystal/Clock Input

The device can be driven from either a low frequency fundamental mode crystal (8–30 MHz) or an external reference clock (5–710 MHz). The crystal is connected across pins IN1 and IN2.

The PCB traces between the crystal and the device must be kept very short to minimize stray capacitance. To ensure maximum compatibility with crystals from multiple vendors, the internal crystal oscillator provides adaptive crystal drive strength based upon the crystal frequency.

The crystal load capacitors are placed on-chip to reduce external component count. If a crystal with a load capacitance outside the range specified in Tables 2, 3, and 12 is supplied to the device, it will result in a slight ppm error in the device clock output frequencies. This error can be compensated for by a small change in the input to output multiplication ratio.

If a reference clock is used, the device accepts a single-ended input reference on IN3 or a differential LVPECL, LVDS, or HCSL source on IN1 and IN2. The input at IN3 can accept an input frequency up to 200 MHz. The signal applied at IN3 should be dc-coupled because internally this signal is ac-coupled to the receive input. A single-ended reference clock up to 350 MHz can be ac-coupled to IN1. A differential reference clock, such as LVPECL, LVDS or HCSL, is input on IN1,2 for frequencies up to 700 MHz. The differential input to IN1,2 requires 0.1 µF ac coupling caps to be located near the device and a 100 Ω termination resistor to be located between these caps and the transmission line going back to the differential driver. See “AN408: Termination Options for Any-Frequency, Any-Output Clock Generators and Clock Buffers” for more information on connecting input signals to IN1,2,3.

This application note can be downloaded from https://www.skyworksinc.com/en/Products/Timing.

2.3. Zero Delay Mode

A clock that is input to the Si5334 will have an unspecified amount of delay from the input pins to the output pins. The zero delay mode can be used to reduce the delay through the Si5334 to typically less than 100 ps. This is accomplished by feeding back the CLK3 output to either IN4 or IN5,6. Using CLK3 allows for an easy PCB route of this signal back to the input. The R3 divider must be set to 1 when using feedback from CLK3 to implement the zero delay mode. All output clocks that are required to have zero delay must also have their Rn divider set to 1. A single-ended signal up to 200 MHz from CLK3 can be input to IN4. A single-ended signal up to 350 MHz from CLK3 can be input to IN5 using the technique shown in AN408. A differential signal up to 710 MHz from CLK3a,b must be input to IN5,IN6.

The IN4 input is electrically the same as IN3 described above. The IN5,IN6 inputs are electrically the same as the IN1,IN2 inputs described above. See AN408 for additional information on signal connections for the zero delay mode.

2.4. Breakthrough MultiSynth Technology

Next-generation timing IC architectures require a wide range of frequencies which are often non-integer related. Traditional clock architectures address this by using multiple single PLL ICs, often at the expense of BOM complexity and power. The Si5334 and Si5338 use patented MultiSynth technology to dramatically simplify timing architectures by integrating the frequency synthesis capability of 4 Phase-Locked Loops (PLLs) in a single device, greatly minimizing size and power requirements versus traditional solutions.

Based on a fractional-N PLL, the heart of the architecture is a low phase noise, high frequency VCO. The VCO supplies a high frequency output clock to the MultiSynth block on each of the four independent output paths. Each MultiSynth operates as a high speed fractional divider with Skyworks Solutions' proprietary phase error correction to divide down the VCO clock to the required output frequency with very low jitter.

The first stage of the MultiSynth architecture is a fractional-N divider which switches seamlessly between the two closest integer divider values to produce the exact output clock frequency with 0 ppm error. To eliminate phase error generated by this process, MultiSynth calculates the relative phase difference between the clock produced by the fractional-N divider and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform. This novel approach makes it possible to generate any output clock frequency without sacrificing jitter performance.

Based on this architecture, the output of each MultiSynth can produce any frequency from 5 to Fvco/8 MHz. To support higher frequency operation, the MultiSynth divider can be bypassed. In bypass mode integer divide ratios of 4 and 6 are supported, which allows for output frequencies of Fvco/4 and Fvco/6 MHz which translates to 367–473.3 MHz and 550–710 MHz respectively. Because each MultiSynth uses the same VCO output there are output frequency limitations when output frequencies greater than Fvco/8 are desired.

For example, if 375 MHz is needed at the output of MultiSynth0, the VCO frequency would need to be 2.25 GHz. Now, all the other MultiSynths can produce any frequency from 5 MHz up to a maximum frequency of 2250/8 = 281.25 MHz. MultiSynth1,2,3 could also produce Fvco/4 = 562.5 MHz or Fvco/6 = 375 MHz. Only two unique frequencies above Fvco/8 can be output: Fvco/6 and Fvco/4.

2.5. Output Driver

There are four clock output channels on the Si5334 (CLK0,CLK1,CLK2,CLK3) with two signal outputs per channel. Each channel may be programmed to be a differential driver or a dual single ended driver. If a channel is factory-programmed to be single ended, then the two outputs for that channel can be factory-programmed to be in-phase or out-of-phase. Si5334 output drivers can be configured as single ended CMOS, SSTL, HSTL or differential LVPECL, LVDS, and HCSL formats.

The supply voltage requirement for each driver format is selectable as shown in Table 14. All unused clock output channels must have their respective VDD0x supply voltage connected to pin 7 and 24 VDD.

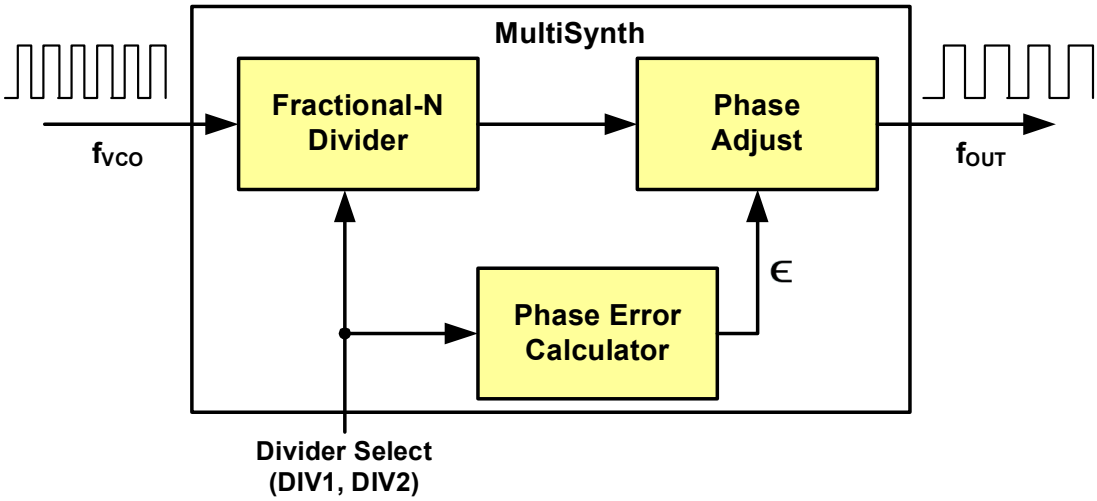


Figure 2. Skyworks Solutions' MultiSynth Technology

Table 14. Output Driver Signal Format Selection

VDD0x Supply Voltage	CMOS	SSTL	HSTL	LVPECL	LVDS	HCSL
1.5			X			
1.8	X	X			X	X
2.5	X	X		X	X	X
3.3	X	X		X	X	X

An OEB pin is provided to enable/disable the output clocks. When OEB = 0, all outputs that have been factory programmed will be on. When OEB = 1, all clock outputs that have been factory programmed will be off and held to a low level.

2.6. Output Clock Initial Phase Offset

Each CLKn output of the Si5334 can have its own unique initial phase offset over a range of +- 45 ns with an accuracy of 20 ps. When the respective R divider is not set to 1, this function is not supported.

2.7. Output Clock Phase Increment and Decrement

The Si5334D/E/F has a pin-controlled phase increment/decrement feature that allows the user to adjust the phase of 1 or more output clocks via pin control. Since their is only 1 pin for increment and 1 pin for decrement, each output clock channel needs to be enabled or disabled for this feature. In addition, the magnitude of the phase step must be set for each clock output channel. The phase adjustment accuracy is 20 ps over a range of ±45 ns, and the phase transition is glitchless. This feature is not available on any clock output that has Spread Spectrum enabled. The maximum clock output frequency supported in this mode of operation is Fvco/8, where Fvco is the frequency of the device's internal voltage controlled oscillator for the configured frequency plan. The phase can be changed at a maximum rate of 1.5 MHz. In order to increment or decrement phase it is necessary to input a positive pulse of >100ns followed by a low of >100 ns. Since this feature uses pins 3 and 4, the reference clock must be input at pins 1 and 2 or the crystal used across these pins. Once a Si5334/D/E/F is factory-programmed, the phase increment/decrement parameters cannot be changed. If one desires to subsequently change the phase increment/decrement parameters on a factory-programmed part, the Si5338 clock generator must be used.

If a phase decrement causes a single MultiSynth clock period to be less than 8/Fvco, all clock outputs may turn off for up to 10 clock periods and then come back on with the phase setting before the illegal decrement.

2.8. Output Clock Frequency Increment and Decrement

The Si5334G/H/J has a pin-controlled frequency increment/decrement feature that allows the user to adjust the frequency at the output of MultiSynth0 only. MultiSynth0 can be connected to any or all of the four output clock buffers with the muxes shown in the " Functional Block Diagram" on page 2. If frequency increment and decrement is required on the other clock outputs the Si5338 should be used. The magnitude of a single frequency step must be factory-programmed. Spread Spectrum and frequency increment/decrement cannot both be active on the same clock output. There is a single pin to control the frequency increment and a single pin to control the frequency decrement. The frequency increment or decrement step size can be factory-programmed from as low as 1 ppm of the initial frequency to a maximum that keeps the output of the MultiSynth within the limits of 5 MHz to Fvco/8. If a frequency increment causes the MultiSynth0 output frequency to go above Fvco/8, then all output clocks may turn off for up to 10 clock cycles and then come back on at the frequency before the increment. If the output frequency needs to go below 5 MHz, refer to "2.9. R Divider Considerations" on page 17 for further information. The frequency transition is glitchless. The frequency can be changed at a maximum rate of 1.5 MHz. In order to increment or decrement frequency it is necessary to input a positive pulse of >100 ns followed by a low of > 100 ns. Since this feature uses pins 3 and 4, the reference clock must be input at pins 1 and 2 or the crystal used across these pins. Once a Si5334/G/H/J is factory-programmed, the frequency increment/decrement parameters cannot be changed. If one desires to subsequently change the frequency increment/decrement parameters on a programmed part, the Si5338 clock generator must be used.

2.9. R Divider Considerations

When the requested output frequency of a channel is below 5 MHz, the Rn (n = 0,1,2,3) divider will automatically be set and enabled. When the Rn divider is active the step size range of the frequency increment and decrement function will decrease by the Rn divide ratio. The Rn divider can be set to {1, 2, 4, 8, 16, 32}.

Non-unity settings of R0 will affect the Finc/Fdec step size at the MultiSynth0 output. For example, if the MultiSynth0 output step size is 2.56 MHz and R0 = 8, the step size at the output of R0 will be 2.56 MHz divided by 8 = .32 MHz. When the Rn divider is set to non-unity, the initial phase of the CLKn output with respect to other CLKn outputs is not guaranteed.

2.10. Spread Spectrum

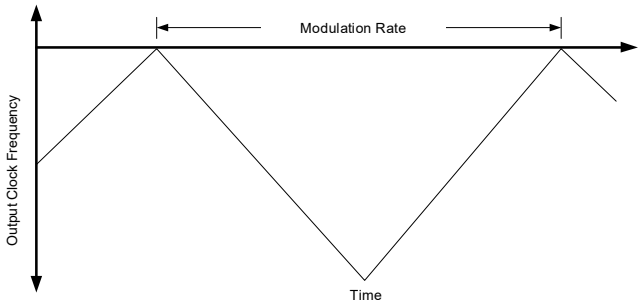


Figure 3. Spread Spectrum Triangle Waveform

To reduce the electromagnetic interference (EMI), the Si5334K/L/M supports PCI Express compliant spread spectrum on all outputs that are 100 MHz. If CLK0 has spread spectrum enabled, then the Finc/Fdec function is not available on CLK0. Spread spectrum modulation spreads the energy across many frequencies to reduce the EMI across a narrow range of frequencies.

The modulation rate is the time required to transition from the maximum spread spectrum frequency to the minimum spread spectrum frequency and then back to the maximum frequency as shown in Figure 3.

The Si5334K/L/M supports 0.5% downspread at a 30–33 kHz rate with a clock frequency of 100 MHz in compliance with the PCI Express standard. When pin 12 (SSPB) is low the factory-programmed clock outputs will have spread spectrum turned on.

2.11. Device Reset

To reset the device, a power cycle must be performed.

2.12. LOSLOL Pin

When either a Loss of Lock (LOL) or Loss of Signal (LOS) condition occurs, the LOSLOL pin will assert.

The LOS condition occurs when there is no input clock input to the Si5334. The loss of lock algorithm works by continuously monitoring the frequency difference between the two inputs of the phase frequency detector. When this frequency difference is greater than 1000 ppm, a loss of lock condition is declared. Note that the VCO will track the input clock frequency for up to ~50000 ppm, which will keep the inputs to the phase frequency detector at the same frequency until the PLL comes out of lock. When a clock input is removed, the LOSLOL pin will assert, and the clock outputs may drift up to 5%. When the input clock with an appropriate frequency is re-applied, the PLL will again lock.

2.13. Power-Up

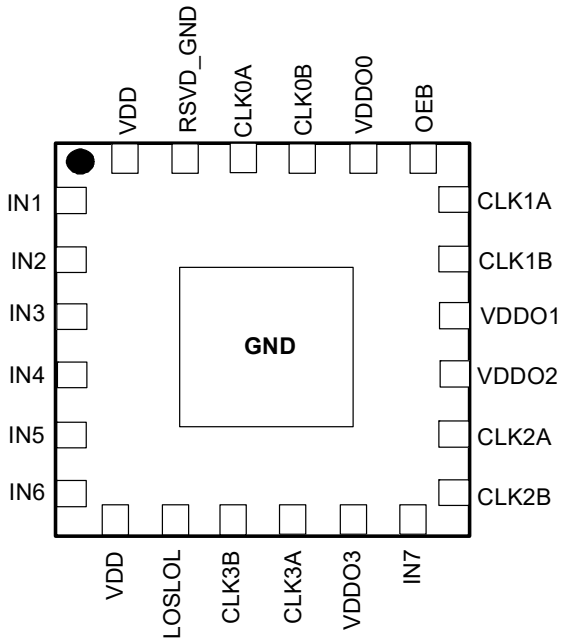
Upon powerup, the device performs an internal self-calibration before operation to optimize loop parameters and jitter performance. While the self-calibration is being performed, the device VCO is being internally controlled by the self-calibration state machine and the LOL alarm is masked. The output clocks appear after the device finishes self calibration.

2.14. Factory Programming Options

Skyworks Solutions Si5334 clock generators are factory-programmable devices. The functions and frequency plans can be customized to meet the needs of your applications. Contact your local Skyworks Solutions sales representative.

Refer to https://www.skyworksinc.com/en/application-pages/clockbuilder-pro-software to access downloadable software to configure the Si5334.

3. Pin Descriptions



Note: Center pad must be tied to GND for normal operation.

Table 15. Si5334 Pin Descriptions

Pin #	Pin Name	I/O	Signal Type	Description
1,2	IN1/IN2	I	Multi	**CLKIN/CLKINB.** These pins are used as the main differential clock input or as the XTAL input. Clock inputs to these pins must be ac-coupled. A crystal should be directly connected to pins 1,2 with the shortest traces possible. Keep the traces from pins 1,2 to the crystal as short as possible and keep other signals and radiating sources away from the crystal. When not in use, leave IN1 unconnected and IN2 connected to GND.

Table 15. Si5334 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
3	IN3	I	Multi	Keep the input level ≥ –0.1 V and < V_{DD}+.1 V. **REFCLKSE** High impedance input for single-ended clock signals such as CMOS. The input should be dc-coupled. **PINC** This pin function is active for devices Si5334D/E/F. A positive pulse of greater than 100 ns width (followed by >100 ns low) will increase the input to output device latency by a factory-programmed amount. The function of this pin is factory programmed. **FINC** This pin function is active for devices Si5334G/H/J. A positive pulse of greater than 100 ns width (followed by >100 ns low) will increase the output frequency of the clock output by a factory-programmed amount. The function of this pin is factory-programmed. If this pin is unused, it should be grounded.
4	IN4	I	LVCMOS	Keep the input level ≥ –0.1 V and < VDD+ 0.1 V. **FDBKSE** High Impedance input for single-ended clock signals, such as CMOS, when the zero delay mode of operation is required. This input should be dc-coupled. **PDEC** This pin function is active for devices Si5334D/E/F. A positive pulse of greater than 100 ns width (followed by >100 ns low) will decrease the input to output device latency by a factory-programmed amount. The function of this pin is factory-programmed. **FDEC** This pin function is active for devices Si5334G/H/J. A positive pulse of greater than 100 ns width (followed by >100 ns low) will decrease the output frequency of the clock output by a factory-programmed amount. The function of this pin is factory-programmed. If this pin is unused, it should be grounded.
5,6	IN5/IN6	I	Multi	**FDBK/FDBKB** These pins form a differential input for feedback clock signals when a zero delay mode of operation is in effect. Always AC couple into these pins. When not is use leave FDBK unconnected and connect FDBKB to ground.
7	VDD	VDD	Supply	**Core Supply Voltage** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.

Table 15. Si5334 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
8	LOSLOL	O	Open Drain	**Loss of Signal or Loss of Lock Indicator.** 0 = No LOS or LOL condition. 1 = A LOS or LOL condition has occurred. For this pin a 1–5 kΩ pull-up resistor to a voltage is required. This voltage may be as high as 3.63 V regardless of the voltage on pin 7.
9	CLK3B	O	Multi	**Output Clock B for Channel 3** May be a single-ended output or half of a differential output with CLK3A being the other differential half. If unused leave this pin floating.
10	CLK3A	O	Multi	**Output Clock A for Channel 3** May be a single-ended output or half of a differential output with CLK3B being the other differential half. If unused leave this pin floating.
11	VDDO3	VDD	Supply	**Output Clock Supply Voltage** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK3A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK3 is not used, this pin must be tied to VDD (pin 7, 24).
12	IN7	I	LVCMOS	**SSPB*.** When low, Spread Spectrum is enabled on every output clock that is programmed for Spread Spectrum. This option is available on the Si5334K/L/M. On an Si5334 that does not contain the spread spectrum functionality, this pin should be connected to GND.
13	CLK2B	O	Multi	**Output Clock B for Channel 2** May be a single-ended output or half of a differential output with CLK2A being the other differential half. If unused leave this pin floating.
14	CLK2A	O	Multi	**Output Clock A for Channel 2** May be a single-ended output or half of a differential output with CLK2B being the other differential half. If unused leave this pin floating.
15	VDDO2	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK2A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK2 is not used, this pin must be tied to VDD (pin 7, 24).
16	VDDO1	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK1A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK1 is not used, this pin must be tied to VDD (pin 7, 24).

Table 15. Si5334 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Type	Description
17	CLK1B	O	Multi	**Output Clock B for Channel 1** May be a single-ended output or half of a differential output with CLK1A being the other differential half. If unused, this pin must be tied to VDD pin 24. If unused leave this pin floating.
18	CLK1A	O	Multi	**Output Clock A for Channel 1** May be a single-ended output or half of a differential output with CLK1B being the other differential half. If unused leave this pin floating.
19	OEB	I	LVCMOS	**Output Enable Low** When low, all the factory-programmed outputs are enabled. When high all factory programmed outputs are forced to a logic low.
20	VDDO0	VDD	Supply	**Output Clock Supply Voltage.** Supply voltage (3.3, 2.5, 1.8, or 1.5 V) for CLK0A,B. A 0.1 µF capacitor must be located very close to this pin. If CLK0 is not used, this pin must be tied to VDD (pin 7, 24).
21	CLK0B	O	Multi	**Output Clock B for Channel 0** May be a single-ended output or half of a differential output with CLK0A being the other differential half. If unused leave this pin floating.
22	CLK0A	O	Multi	**Output Clock A for Channel 0** May be a single-ended output or half of a differential output with CLK0B being the other differential half. If unused leave this pin floating.
23	RSVD_GND	GND	GND	**Ground.** Must be connected to system ground.
24	VDD	VDD	Supply	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
GND PAD	GND	GND	GND	**Ground Pad.** This is the large pad in the center of the package. Device specifications cannot be guaranteed unless the ground pad is properly connected to a ground plane on the PCB. See section 6.0 for the PCB pad sizes and ground via requirements.

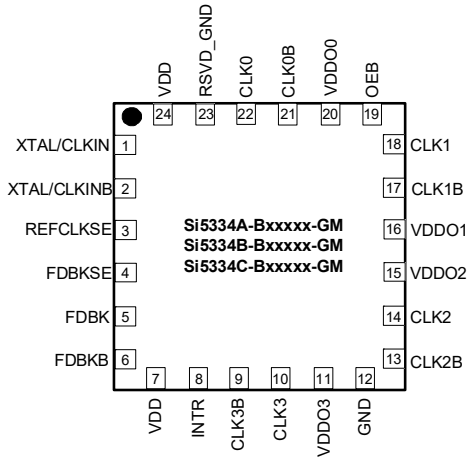
4. Device Pinout by Part Number

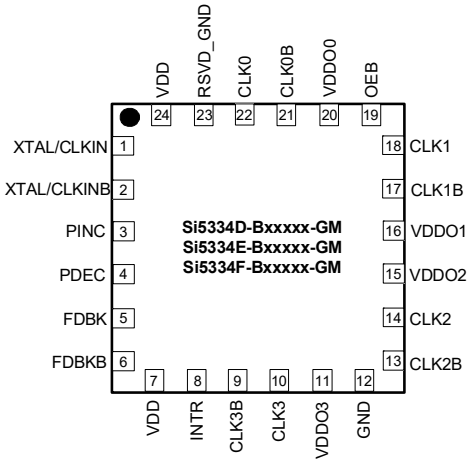
The Si5334 is orderable in three different speed grades: Si5334A/D/G/K have a maximum output clock frequency limit of 710 MHz. Si5338B/E/H/L have a maximum output clock frequency of 350 MHz. Si5338C/F/J/M have a maximum output clock frequency of 200 MHz.

Brief pin functions follow.

- **XTAL/CLKIN**—crystal or one side of differential input clock
- **XTAL/CLKINB**—crystal or one side of differential input clock
- **REFCLKSE**—single-ended reference clock input
- **FDBKSE**—single-ended feedback clock input
- **FDBK**—differential feedback input
- **FDBKB**—differential feedback input inverted
- **FINC**—frequency increment pin
- **FDEC**—frequency decrement pin
- **PINC**—phase increment pin
- **PDEC**—phase decrement pin
- **OEB**—output enable low

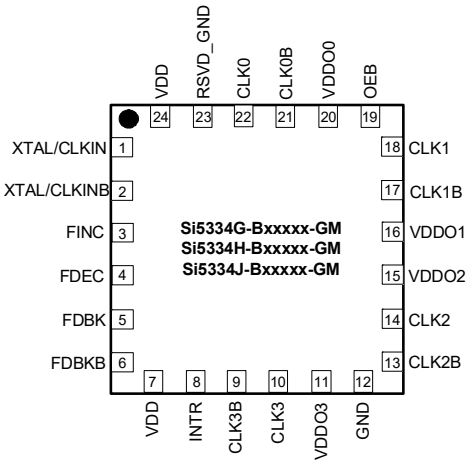
See the four groupings below for the available pin control functions on pins 3, 4 and 12.

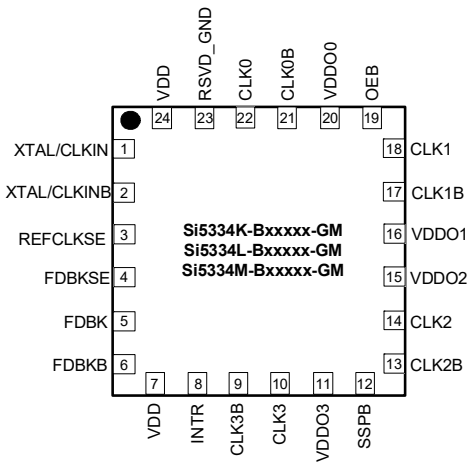




Pin #	Function	Pin #	Function
1	XTAL/CLKIN	13	CLK2B
2	XTAL/CLKINB	14	CLK2
3	REFCLKSE	15	VDDO2
4	FDBKSE	16	VDDO1
5	FDBK	17	CLK1B
6	FDBKB	18	CLK1
7	VDD	19	OEB
8	INTR	20	VDDO0
9	CLK3B	21	CLK0B
10	CLK3	22	CLK0
11	VDDO3	23	RSVDGND
12	GND	24	VDD

Pin #	Function	Pin #	Function
1	XTAL/CLKIN	13	CLK2B
2	XTAL/CLKINB	14	CLK2
3	PINC	15	VDDO2
4	PDEC	16	VDDO1
5	FDBK	17	CLK1B
6	FDBKB	18	CLK1
7	VDD	19	OEB
8	INTR	20	VDDO0
9	CLK3B	21	CLK0B
10	CLK3	22	CLK0
11	VDDO3	23	RSVDGND
12	GND	24	VDD



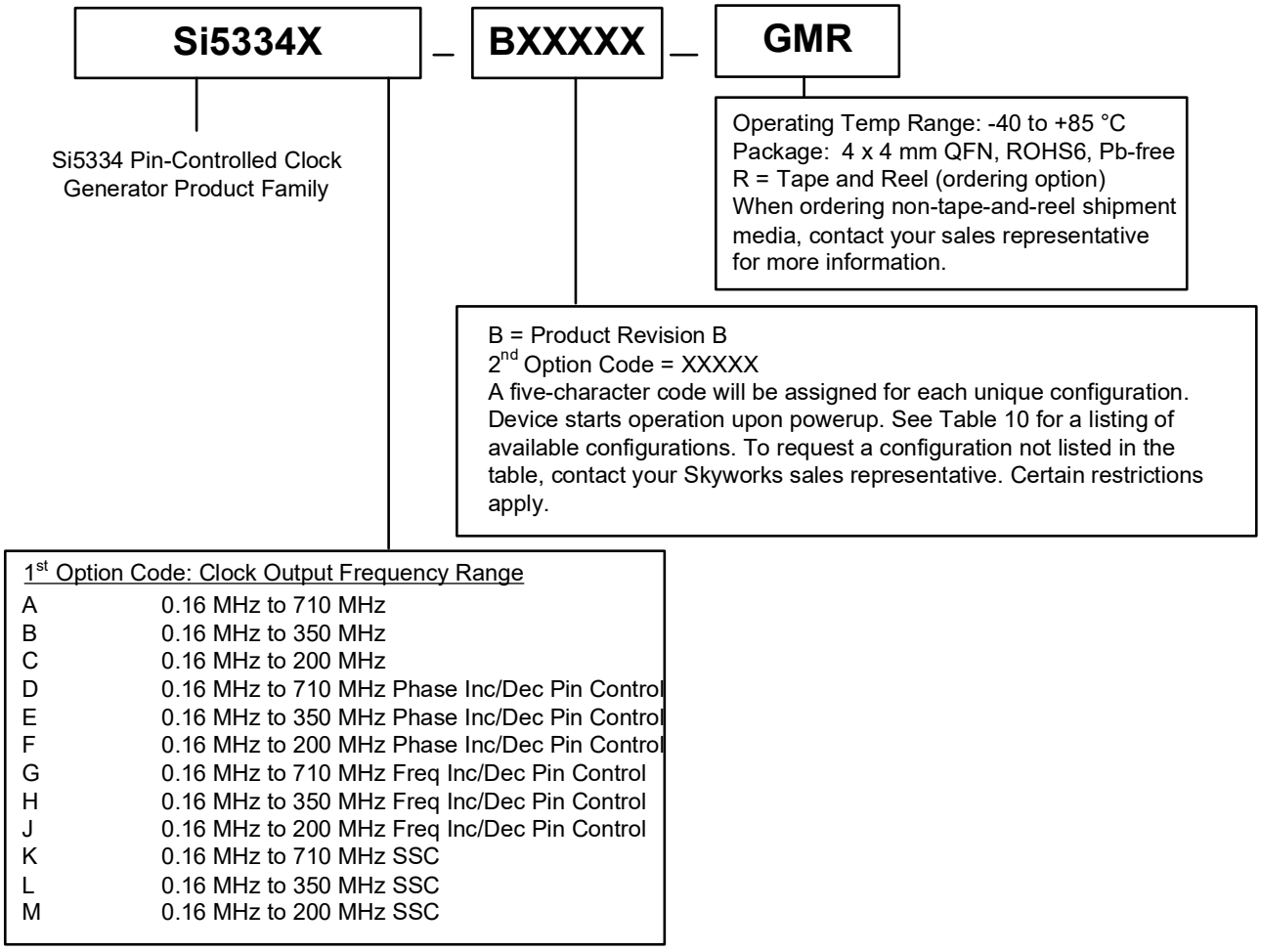


Pin #	Function	Pin #	Function
1	XTAL/CLKIN	13	CLK2B
2	XTAL/CLKINB	14	CLK2
3	FINC	15	VDDO2
4	FDEC	16	VDDO1
5	FDBK	17	CLK1B
6	FDBKB	18	CLK1
7	VDD	19	OEB
8	INTR	20	VDDO0
9	CLK3B	21	CLK0B
10	CLK3	22	CLK0
11	VDDO3	23	RSVDGND
12	GND	24	VDD

Pin #	Function	Pin #	Function
1	XTAL/CLKIN	13	CLK2B
2	XTAL/CLKINB	14	CLK2
3	REFCLKSE	15	VDDO2
4	FDBKSE	16	VDDO1
5	FDBK	17	CLK1B
6	FDBKB	18	CLK1
7	VDD	19	OEB
8	INTR	20	VDDO0
9	CLK3B	21	CLK0B
10	CLK3	22	CLK0
11	VDDO3	23	RSVDGND
12	SSPB	24	VDD

5. Ordering Information and Standard Frequency Plans

5.1. Ordering Information



5.2. Evaluation Boards

Si5338 – EVB

The Si5338 evaluation board allows creation of custom and standard configurations for the Si5334. Refer to https://www.skyworksinc.com/en/products/timing/evaluation-kits/si5338-evaluation-kit for more information.

5.3. Standard Frequency Plans

Table 16. Si5334 Standard Frequency Plans

			CLKIN		CLK0		CLK1		CLK2		CLK3	
Application	**OPN**	**Input**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**
SONET/SDH	Si5334C-B00099-GM	Clock	19.4400	3.3 V CMOS	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL	77.7600	3.3 V LVPECL	77.7600	3.3 V LVPECL
	Si5334C-B00101-GM	Clock	19.4400	3.3 V CMOS	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL
	Si5334A-B00102-GM	Clock	19.4400	3.3 V CMOS	622.0800	3.3 V LVPECL	622.0800	3.3 V LVPECL	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL
	Si5334C-B00103-GM	Clock	38.8800	3.3 V CMOS	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL	77.7600	3.3 V LVPECL	77.7600	3.3 V LVPECL
	Si5334C-B00104-GM	Clock	38.8800	3.3 V CMOS	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL
	Si5334A-B00105-GM	Clock	38.8800	3.3 V CMOS	622.0800	3.3 V LVPECL	622.0800	3.3 V LVPECL	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL
	Si5334C-B00106-GM	Clock	155.5200	3.3 V LVPECL	161.1328	3.3 V LVPECL	156.2500	3.3 V LVPECL	156.2500	3.3 V LVPECL	155.5200	3.3 V LVPECL

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Table 16. Si5334 Standard Frequency Plans (Continued)

			CLKIN		CLK0		CLK1		CLK2		CLK3	
Application	**OPN**	**Input**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**
Ethernet/Fibre Channel	Si5334C-B00107-GM	Xtal	25.0000	n/a	161.1328	3.3 V LVPECL	156.2500	3.3 V LVPECL	125.0000	3.3 V LVPECL	25.0000	3.3 V CMOS
	Si5334C-B00108-GM	Clock	25.0000	3.3 V CMOS	161.1328	3.3 V LVPECL	156.2500	3.3 V LVPECL	125.0000	3.3 V LVPECL	25.0000	3.3 V CMOS
	Si5334B-B00109-GM	Xtal	25.0000	n/a	312.5000	3.3 V LVPECL	156.2500	3.3 V LVPECL	125.0000	3.3 V LVPECL	62.5000	3.3 V CMOS
	Si5334B-B00110-GM	Clock	25.0000	3.3 V CMOS	312.5000	3.3 V LVPECL	156.2500	3.3 V LVPECL	125.0000	3.3 V LVPECL	62.5000	3.3 V CMOS
	Si5334C-B00111-GM	Xtal	25.0000	n/a	125.0000	3.3 V CMOS	125.0000	3.3 V CMOS	125.0000	3.3 V CMOS	125.0000	3.3 V CMOS
	Si5334C-B00112-GM	Clock	25.0000	3.3 V CMOS	125.0000	3.3 V CMOS	125.0000	3.3 V CMOS	125.0000	3.3 V CMOS	125.0000	3.3 V CMOS
	Si5334C-B00113-GM	Xtal	25.0000	n/a	125.0000	1.8 V LVDS	125.0000	1.8 V LVDS	125.0000	1.8 V LVDS	125.0000	1.8 V LVDS
	Si5334C-B00114-GM	Clock	25.0000	3.3 V CMOS	125.0000	1.8 V LVDS	125.0000	1.8 V LVDS	125.0000	1.8 V LVDS	125.0000	1.8 V LVDS
	Si5334C-B00115-GM	Xtal	25.0000	n/a	156.2500	1.8 V LVDS	156.2500	1.8 V LVDS	125.0000	1.8 V LVDS	125.0000	1.8 V LVDS

Table 16. Si5334 Standard Frequency Plans (Continued)

			CLKIN		CLK0		CLK1		CLK2		CLK3	
Application	**OPN**	**Input**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**
Ethernet/Fibre Channel (Continued)	Si5334C-B00116-GM	Clock	25.0000	3.3 V CMOS	156.2500	1.8 V LVDS	156.2500	1.8 V LVDS	125.0000	1.8 V LVDS	125.0000	1.8 V LVDS
	Si5334C-B00117-GM	Xtal	25.0000	n/a	125.0000	3.3 V CMOS	125.0000	3.3 V CMOS	106.2500	3.3 V CMOS	106.2500	3.3 V CMOS
	Si5334C-B00118-GM	Clock	25.0000	3.3 V CMOS	125.0000	3.3 V CMOS	125.0000	3.3 V CMOS	106.2500	3.3 V CMOS	106.2500	3.3 V CMOS
	Si5334C-B00119-GM	Xtal	25.0000	n/a	125.0000	1.8 V LVDS	125.0000	1.8 V LVDS	106.2500	3.3 V LVPECL	106.2500	3.3 V LVPECL
	Si5334C-B00120-GM	Clock	25.0000	3.3 V CMOS	125.0000	1.8 V LVDS	125.0000	1.8 V LVDS	106.2500	3.3 V LVPECL	106.2500	3.3 V LVPECL
	Si5334B-B00121-GM	Xtal	25.0000	n/a	212.5000	3.3 V LVPECL	212.5000	3.3 V LVPECL	106.2500	3.3 V LVPECL	106.2500	3.3 V LVPECL
	Si5334B-B00122-GM	Clock	25.0000	3.3 V CMOS	212.5000	3.3 V LVPECL	212.5000	3.3 V LVPECL	106.2500	3.3 V LVPECL	106.2500	3.3 V LVPECL
	Si5334B-B00123-GM	Xtal	25.0000	n/a	212.5000	3.3 V LVDS	212.5000	3.3 V LVDS	106.2500	3.3 V LVDS	106.2500	3.3 V LVDS
	Si5334B-B00124-GM	Clock	25.0000	3.3 V CMOS	212.5000	3.3 V LVDS	212.5000	3.3 V LVDS	106.2500	3.3 V LVDS	106.2500	3.3 V LVDS
	Si5334C-B00125-GM	Xtal	25.0000	n/a	156.2500	3.3 V LVPECL	155.5200	3.3 V LVPECL	125.0000	1.8 V LVDS	106.2500	3.3 V LVPECL
	Si5334C-B00126-GM	Clock	25.0000	3.3 V CMOS	156.2500	3.3 V LVPECL	155.5200	3.3 V LVPECL	125.0000	1.8 V LVDS	106.2500	3.3 V LVPECL
	Si5334C-B00127-GM	Clock	125.0000	3.3 V LVPECL	156.2500	3.3 V LVPECL	156.2500	3.3 V LVPECL	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL
	Si5334C-B00128-GM	Clock	156.2500	3.3 V LVPECL	155.5200	3.3 V LVPECL	155.5200	3.3 V LVPECL	125.0000	3.3 V LVPECL	125.0000	3.3 V LVPECL

Table 16. Si5334 Standard Frequency Plans (Continued)

			CLKIN		CLK0		CLK1		CLK2		CLK3	
Application	**OPN**	**Input**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**
Synchronous Ethernet (RX-Side)	Si5334C-B00129-GM	Clock	19.4400	3.3 V CMOS	25.0000	3.3 V CMOS	25.0000	3.3 V CMOS	25.0000	3.3 V CMOS	25.0000	3.3 V CMOS
	Si5334C-B00130-GM	Clock	25.0000	3.3 V CMOS	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS
	Si5334C-B00131-GM	Clock	125.0000	3.3 V CMOS	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS
	Si5334C-B00132-GM	Clock	156.2500	3.3 V LVPECL	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS
	Si5334C-B00133-GM	Clock	161.1328	3.3 V LVPECL	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS	19.4400	3.3 V CMOS
PDH	Si5334C-B00134-GM	Clock	19.4400	3.3 V CMOS	1.5440	3.3 V CMOS	1.5440	3.3 V CMOS	1.5440	3.3 V CMOS	1.5440	3.3 V CMOS
	Si5334C-B00135-GM	Clock	19.4400	3.3 V CMOS	2.0480	3.3 V CMOS	2.0480	3.3 V CMOS	2.0480	3.3 V CMOS	2.0480	3.3 V CMOS
	Si5334C-B00136-GM	Clock	19.4400	3.3 V CMOS	2.0480	3.3 V CMOS	2.0480	3.3 V CMOS	1.5440	3.3 V CMOS	1.5440	3.3 V CMOS
	Si5334C-B00137-GM	Clock	19.4400	3.3 V CMOS	8.1920	3.3 V CMOS	4.0960	3.3 V CMOS	2.0480	3.3 V CMOS	2.0480	3.3 V CMOS
	Si5334C-B00138-GM	Clock	19.4400	3.3 V CMOS	44.7360	3.3 V CMOS	44.7360	3.3 V CMOS	34.3680	3.3 V CMOS	34.3680	3.3 V CMOS
Broadcast Video	Si5334C-B00139-GM	Xtal	27.0000	n/a	74.2500	3.3 V CMOS	74.1758	3.3 V CMOS	54.0000	3.3 V CMOS	27.0000	3.3 V CMOS
	Si5334C-B00140-GM	Clock	27.0000	3.3 V CMOS	74.2500	3.3 V CMOS	74.1758	3.3 V CMOS	54.0000	3.3 V CMOS	27.0000	3.3 V CMOS
	Si5334C-B00141-GM	Xtal	27.0000	n/a	74.2500	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS	27.0000	3.3 V CMOS
	Si5334C-B00142-GM	Clock	27.0000	3.3 V CMOS	74.2500	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS	27.0000	3.3 V CMOS
	Si5334C-B00143-GM	Xtal	27.0000	n/a	108.0000	3.3 V LVDS	74.2500	3.3 V LVDS	74.1758	3.3 V LVDS	54.0000	3.3 V LVDS
	Si5334C-B00144-GM	Clock	27.0000	3.3 V CMOS	108.0000	3.3 V LVDS	74.2500	3.3 V LVDS	74.1758	3.3 V LVDS	54.0000	3.3 V LVDS

Table 16. Si5334 Standard Frequency Plans (Continued)

			CLKIN		CLK0		CLK1		CLK2		CLK3	
Application	**OPN**	**Input**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**
Broadcast Video (Continued)	Si5334C-B00145-GM	Xtal	27.0000	n/a	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS
	Si5334C-B00146-GM	Clock	27.0000	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS
	Si5334C-B00147-GM	Xtal	27.0000	n/a	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS
	Si5334C-B00148-GM	Clock	27.0000	3.3 V CMOS	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS
	Si5334C-B00149-GM	Xtal	27.0000	n/a	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS
	Si5334C-B00150-GM	Clock	27.0000	3.3 V CMOS	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS
	Si5334C-B00151-GM	Xtal	27.0000	n/a	148.5000	3.3 V LVDS	148.3516	3.3 V LVDS	74.2500	3.3 V CMOS	74.1758	3.3 V CMOS
	Si5334C-B00152-GM	Clock	27.0000	3.3 V CMOS	148.5000	3.3 V LVDS	148.3516	3.3 V LVDS	74.2500	3.3 V CMOS	74.1758	3.3 V CMOS
	Si5334C-B00153-GM	Xtal	27.0000	n/a	156.2500	3.3 V LVDS	148.5000	3.3 V LVDS	148.3516	3.3 V LVDS	108.0000	3.3 V LVDS
	Si5334B-B00154-GM	Clock	27.0000	3.3 V CMOS	156.2500	3.3 V LVDS	148.5000	3.3 V LVDS	148.3516	3.3 V LVDS	108.0000	3.3 V LVDS
	Si5334C-B00155-GM	Xtal	27.0000	n/a	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS
	Si5334B-B00156-GM	Clock	27.0000	3.3 V CMOS	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS
	Si5334C-B00157-GM	Xtal	27.0000	n/a	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS
	Si5334C-B00158-GM	Clock	27.0000	3.3 V CMOS	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS
	Si5334C-B00159-GM	Xtal	27.0000	n/a	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS
	Si5334C-B00160-GM	Clock	27.0000	3.3 V CMOS	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS

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Table 16. Si5334 Standard Frequency Plans (Continued)

			CLKIN		CLK0		CLK1		CLK2		CLK3	
Application	**OPN**	**Input**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**	**Freq**	**Format**
Broadcast Video (Continued)	Si5334C-B00161-GM	Clock	74.1758	3.3 V CMOS	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS	74.2500	3.3 V CMOS
	Si5334C-B00162-GM	Clock	74.2500	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS	74.1758	3.3 V CMOS
	Si5334C-B00163-GM	Clock	148.3516	3.3 V LVDS	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS	148.5000	3.3 V LVDS
	Si5334B-B00164-GM	Clock	148.3516	3.3 V LVDS	270.0000	3.3 V LVDS	270.0000	3.3 V LVDS	270.0000	3.3 V LVDS	270.0000	3.3 V LVDS
	Si5334C-B00165-GM	Clock	148.5000	3.3 V LVDS	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS	148.3516	3.3 V LVDS
	Si5334B-B00166-GM	Clock	148.5000	3.3 V LVDS	270.0000	3.3 V LVDS	270.0000	3.3 V LVDS	270.0000	3.3 V LVDS	270.0000	3.3 V LVDS
PCIe*	Si5334M-B00167-GM	Xtal	25.0000	n/a	100.0000	3.3 V HCSL	100.0000	3.3 V HCSL	100.0000	3.3 V HCSL	100.0000	3.3 V HCSL
	Si5334M-B00168-GM	Clock	25.0000	3.3 V CMOS	100.0000	3.3 V HCSL	100.0000	3.3 V HCSL	100.0000	3.3 V HCSL	100.0000	3.3 V HCSL

Notes:
1. –0.5% downspread enabled on CLK0-CLK3
2. To request new frequency plans/device configurations, please contact your local Skyworks Solutions sales representative.

6. Package Outline: 24-Lead QFN

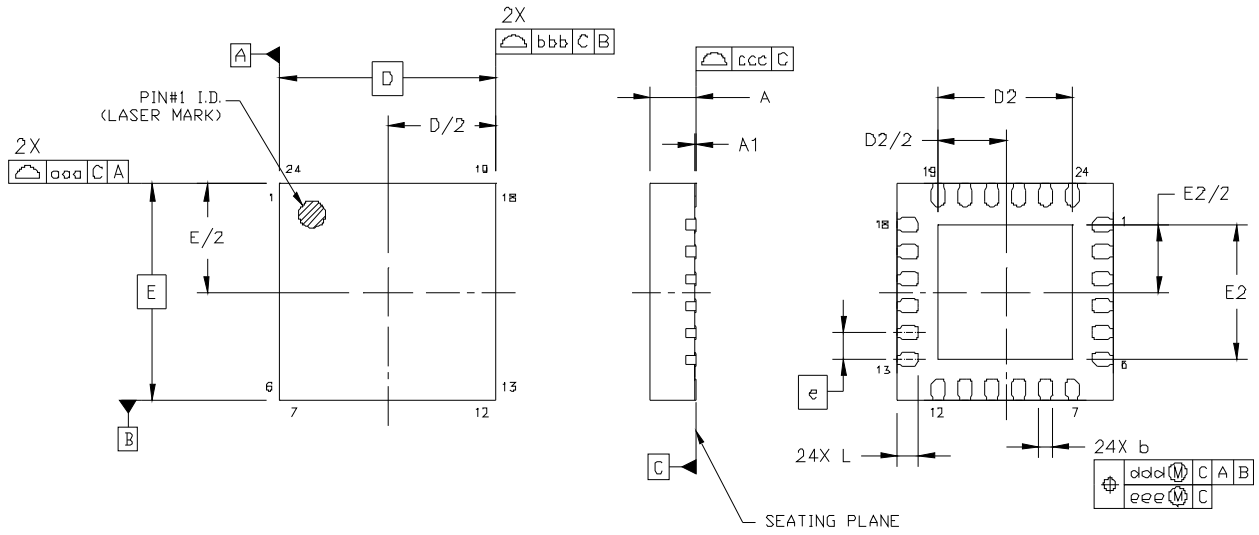


Figure 4. 24-Lead Quad Flat No-lead (QFN)

Table 17. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. Recommended PCB Land Pattern

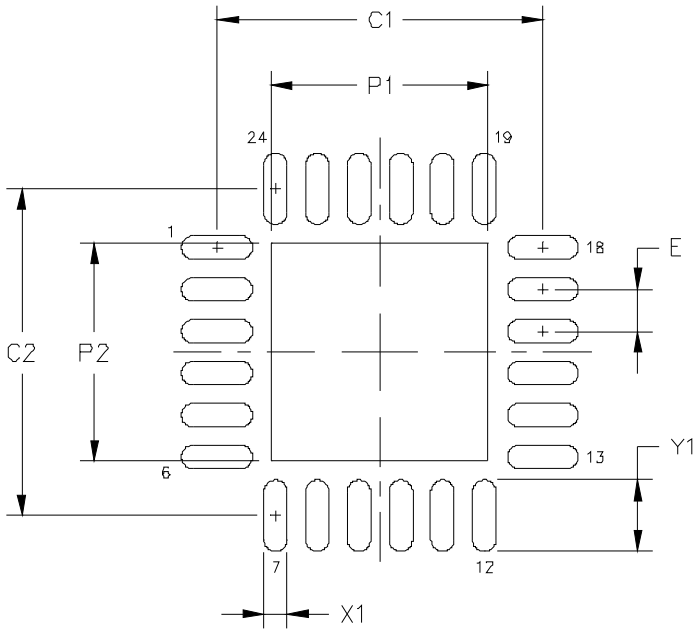


Table 18. PCB Land Pattern

Dimension	Min	Nom	Max
P1	2.50	2.55	2.60
P2	2.50	2.55	2.60
X1	0.20	0.25	0.30
Y1	0.75	0.80	0.85
C1	3.90		
C2	3.90		
E	0.50		

Notes

General:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. Connect the center ground pad to a ground plane with no less than five vias. These 5 vias should have a length of no more than 20 mils to the ground plane. Via drill size should be no smaller than 10 mils. A longer distance to the ground plane is allowed if more vias are used to keep the inductance from increasing.

Solder Mask Design:

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design:

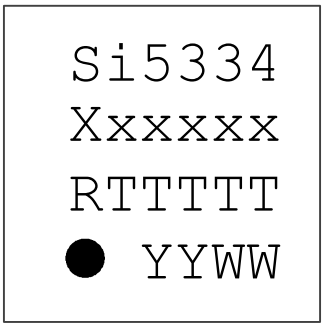
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
9. A 2x2 array of 1.0 mm square openings on 1.25 mm pitch should be used for the center ground pad.

Card Assembly:

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Marking

8.1. Si5334 Top Marking



8.2. Top Marking Explanation

Line	Characters	Description
Line 1	Si5334	Base part number.
Line 2	Xxxxxx	X = Frequency and configuration code. See "5. Ordering Information and Standard Frequency Plans" on page 25 for more information. xxxxx = NVM code. See “5. Ordering Information and Standard Frequency Plans” .
Line 3	RTTTTT	R = Product revision. TTTTT = Manufacturing trace code.
Line 4	Circle with 0.5 mm diameter; left-justified	Pin 1 indicator.
	YYWW	YY = Year. WW = Work week. Characters correspond to the year and work week of package assembly.

9. Device Errata

Please visit www.skyworksinc.com to access the device errata document.

Document Change List

Revision 0.1 to Revision 0.15

- Updated tables for ac/dc specs to remove TBDs.
- Updated ordering OPN in Table 10 from 34C to 34M-00167/00168-GM.
- Updated SSC information for correct part number.
- Removed diagram in Section 3.
- Corrected Pin 12 description
- Removed low-power LVPECL mode.
- Updated pin descriptions to say 710 MHz.
- Added PCB layout notes on via requirements for GND pad.
- Removed description of field programming as this is not supported.

Revision 0.15 to Revision 0.16

- Changed cycle-cycle jitter spec from pk-pk to pk.
- Change refclk1 pin name to refclkse.

Revision 0.16 to Revision 1.0

- Updated Table 2, “DC Characteristics,” on page 4.
  - Updated dc characteristics for CMOS loads.
  - Added core supply current in buffer mode.
  - Added CML output buffer supply current in CML mode.
- Updated Table 3, “Performance Characteristics,” on page 5.
  - PLL Lock Range test changed to PLL Tracking Range and added typical specification.
  - Added Maximum Propragation Delay value.
- Updated Table 4, “Input and Output Clock Characteristics,” on page 6.
  - Added CML Output specs.
  - Corrected VI to 3.73 V.
  - Corrected tR/tF (15 pF) to 2.0 ns.
  - Corrected LVPECL Output Voltage (typ) to VDDO – 1.45.
- Updated Table 5, “Control Pins,” on page 9.
  - Updated V_{IH} to 3.73 V.
  - Corrected V_{IL} and V_{OL}.
- Expanded Tables 6–9 with recommended and supported crystal load capacitance values.
- Updated Table 10, “Jitter Specifications[1,2,3],” on page 11.
  - Updated typical specifications for total jitter for PCI Express 1.1 Common clocked topology.
  - Updated typical specifications for RMS jitter for PCI Express 2.1 Common clocked topology.
  - Removed RMS jitter specification for PCI Express 2.1 and 3.0 Data clocked topology.
- Updated Table 12, “Thermal Characteristics,” on page 13.
- Updated Table 13, “Absolute Maximum Ratings[1],” on page 13
  - Added MSL level information.
  - Added Peak Soldering Reflow Temperature.
- Corrected Table 15, “Si5334 Pin Descriptions,” on page 19.
  - Changed “Supply” to “LVCMOS” for IN7 (pin 12).
- Updated and moved "5. Ordering Information and Standard Frequency Plans" on page 25.
- Added "8. Top Marking" on page 34.
- Added "9. Device Errata" on page 35.

Revision 1.0 to Revision 1.1

- Removed down spread errata that has been corrected in revision B.
- Updated ordering information to refer to Revision B silicon.
- Updated top marking explanation in section 8.2.
- Updated “Device Pinout by Part Number” part number references.
- Standard frequency plan OPNs in Table 16 updated to reflect Rev B part numbers.

Revision 1.1 to Revision 1.2

- Added link to errata document.

Revision 1.2 to Revision 1.3

- Removed MSL rating.

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