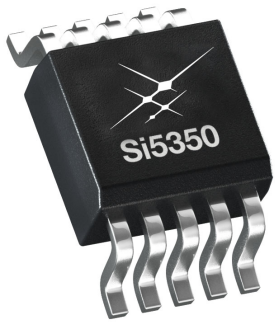
Si5350B-B

Factory-Programmable Any-Frequency CMOS Clock Generator + VCXO

Features

- https://www.skyworksinc.com/Products/Timing/CMOS-Clock-Generators
- Generates up to 8 non-integer-related frequencies from 2.5 kHz to 200 MHz
- Exact frequency synthesis at each output (0 ppm error)
- Highly linear VCXO gain (kv)
- Glitchless frequency changes
- Low output period jitter: < 70 ps pp, typ
- Configurable Spread Spectrum selectable at each output
- User-configurable control pins:
  - Output Enable (OEB_0/1/2)
  - Power Down (PDN)
  - Frequency Select (FS_0/1)
  - Spread Spectrum Enable (SSEN)
- Supports static phase offset
- Rise/fall time control
- Operates from a low-cost, fixed frequency AT-cut, non-pullable crystal: 25 or 27 MHz
- Separate voltage supply pins provide level translation:
  - Core VDD: 2.5 V or 3.3 V
  - Output VDDO: 1.8 V, 2.5 V, or 3.3 V
- Excellent PSRR eliminates external power supply filtering
- Very low power consumption (25 mA, core, typ)
- Available in three packages types:
  - 10-MSOP: 3 outputs
  - 16-QFN (3x3 mm): 4 output
  - 20-QFN (4x4 mm): 8 output
- PCIE Gen 1 compliant
- Supports HCSL compatible swing

10-MSOP



16-QFN



20-QFN



Ordering Information:
See page 23

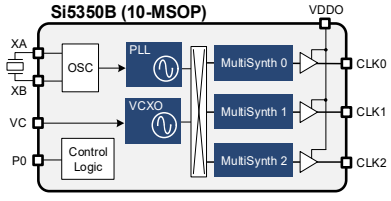
Applications

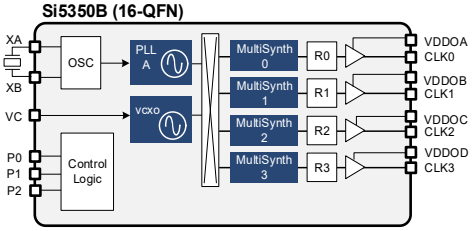
- HDTV, DVD/Blu-ray, set-top box
- Audio/video equipment, gaming
- Printers, scanners, projectors
- Handheld instrumentation
- Residential gateways
- Networking/communication
- Servers, storage
- XO replacement

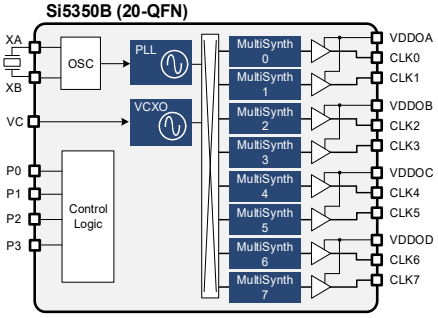
Description

The Si5350B combines a clock generator and VCXO function into a single device. A flexible architecture enables this user definable custom timing device to generate any of the specified output frequencies from either the internal PLL or the VCXO. This allows the Si5350B to replace multiple crystals, crystal oscillators, and VCXOs. Custom Si5350B configurations can be created using ClockBuilder Pro.

Functional Block Diagram







1. Ordering Guide

Table 1. Complete Si5350/51 Clock Generator Family

Part Number	I²C or Pin	Frequency Reference	Programmed?	Outputs	Data Sheet
Si5351A-B-GT	I²C	XTAL only	Blank	3	Si5351A/B/C-B
Si5351A-B-GM1	I²C	XTAL only	Blank	4	Si5351A/B/C-B
Si5351B-B-GM1	I²C	XTAL and/or Voltage	Blank	4	Si5351A/B/C-B
Si5351C-B-GM1	I²C	XTAL and/or CLKIN	Blank	4	Si5351A/B/C-B
Si5351A-B-GM	I²C	XTAL only	Blank	8	Si5351A/B/C-B
Si5351B-B-GM	I²C	XTAL and/or Voltage	Blank	8	Si5351A/B/C-B
Si5351C-B-GM	I²C	XTAL and/or CLKIN	Blank	8	Si5351A/B/C-B
Si5351A-Bxxxxx-GT	I²C	XTAL only	Factory Preprogrammed	3	Si5351A/B/C-B
Si5351A-Bxxxxx-GM1	I²C	XTAL only	Factory Preprogrammed	4	Si5351A/B/C-B
Si5351B-Bxxxxx-GM1	I²C	XTAL and/or Voltage	Factory Preprogrammed	4	Si5351A/B/C-B
Si5351C-Bxxxxx-GM1	I²C	XTAL and/or CLKIN	Factory Preprogrammed	4	Si5351A/B/C-B
Si5351A-Bxxxxx-GM	I²C	XTAL only	Factory Preprogrammed	8	Si5351A/B/C-B
Si5351B-Bxxxxx-GM	I²C	XTAL and/or Voltage	Factory Preprogrammed	8	Si5351A/B/C-B
Si5351C-Bxxxxx-GM	I²C	XTAL and/or CLKIN	Factory Preprogrammed	8	Si5351A/B/C-B
Si5350A-Bxxxxx-GT	Pin	XTAL only	Factory Preprogrammed	3	Si5350A-B
Si5350A-Bxxxxx-GM1	Pin	XTAL only	Factory Preprogrammed	4	Si5350A-B
Si5350A-Bxxxxx-GM	Pin	XTAL only	Factory Preprogrammed	8	Si5350A-B
Si5350B-Bxxxxx-GT	Pin	XTAL and/or Voltage	Factory Preprogrammed	3	Si5350B-B
Si5350B-Bxxxxx-GM1	Pin	XTAL and/or Voltage	Factory Preprogrammed	4	Si5350B-B
Si5350B-Bxxxxx-GM	Pin	XTAL and/or Voltage	Factory Preprogrammed	8	Si5350B-B
Si5350C-Bxxxxx-GT	Pin	XTAL and/or CLKIN	Factory Preprogrammed	3	Si5350C-B
Si5350C-Bxxxxx-GM1	Pin	XTAL and/or CLKIN	Factory Preprogrammed	4	Si5350C-B
Si5350C-Bxxxxx-GM	Pin	XTAL and/or CLKIN	Factory Preprogrammed	8	Si5350C-B

2. Technical Support Resources

Table 2. Technical Support Resources

Resource	URL
Si5350/51 Frequently Asked Questions	https://www.skyworksinc.com/en/Products/Timing
ClockBuilder Pro (CBPro) Software	https://www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software
Si535x Development Kits	https://www.skyworksinc.com/en/Products/Timing/Evaluation-Kits/si535x-b20qfn-evb-evaluation-kit

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3. Electrical Specifications

Table 3. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	25	85	°C
Core Supply Voltage	V_{DD}		3.0	3.3	3.60	V
			2.25	2.5	2.75	V
Output Buffer Voltage	V_{DDOx}		1.71	1.8	1.89	V
			2.25	2.5	2.75	
			3.0	3.3	3.60	
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted. VDD and VDDOx can be operated at independent voltages. Power supply sequencing for VDD and VDDOx requires that all VDDOx be powered up either before or at the same time as VDD.						

Table 4. DC Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current*	I_{DD}	Enabled 3 outputs	—	20	30	mA
		Enabled 4 outputs	—	21	32	mA
		Enabled 8 outputs	—	25	40	mA
		Power Down (PDN = V_{DD})	—	—	50	µA
Output Buffer Supply Current (Per Output)*	I_{DDOx}	C_L = 5 pF	—	2.2	5.6	mA
Input Current	I_{P0-P3}	Pins P0, P1, P2, P3 V_{P0-P3} < 3.6 V	—	—	10	µA
	I_{VC}	VC	—	—	30	µA
Output Impedance	Z_{OI}	3.3 V VDDO, default high drive	—	50	—	Ω
***Note:** Output clocks less than or equal to 100 MHz.						

Table 5. AC Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VCXO Control Voltage Range	Vc		0	$V_{DD}/2$	V_{DD}	V
VCXO Gain (configurable)	kv	Vc = 10–90% of V_{DD}	18	—	150	ppm/V
VCXO Control Voltage Linearity	KVL	Vc = 10–90% of V_{DD}	–5	—	+5	%
VCXO Pull Range (configurable)*	PR	V_{DD} = 3.3 V Vc = 10–90% of V_{DD}	±30	0	±240	ppm
VCXO Modulation Bandwidth			—	10	—	kHz
Power-Up Time	TRDY	From V_{DD} = V_{DDmin} to valid output clock, C_L = 5 pF, f_{CLKn} > 1 MHz	—	2	10	ms
Power-Up Time, PLL Bypass Mode	TBYP	From V_{DD} = V_{DDmin} to valid output clock, C_L = 5 pF, f_{CLKn} > 1 MHz	—	0.5	1	ms
Output Enable Time	T_{OE}	From OEB assertion to valid clock output, C_L = 5 pF, f_{CLKn} > 1 MHz	—	—	10	µs
Output Frequency Transition Time	T_{FREQ}	f_{CLKn} > 1 MHz	—	—	10	µs
Spread Spectrum Frequency Deviation	SS_{DEV}	Down spread. Selectable in 0.1% steps.	–0.1	—	–2.5	%
		Center spread. Selectable in 0.1% steps.	±0.1	—	±1.5	%
Spread Spectrum Modulation Rate	SS_{MOD}		30	31.5	33	kHz

***Note:** Contact Skyworks Solutions for VCXO operation at 2.5 V.

Table 6. Input Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	f_{XTAL}		25	—	27	MHz
VC Input Resistance			100	—	—	kΩ
P0-P3 Input Low Voltage	V_{IL_P0-3}		–0.1	—	0.3 x V_{DD}	V
P0-P3 Input High Voltage	V_{IH_P0-3}		0.7 x V_{DD}	—	3.60	V

Table 7. Output Characteristics

(V_{DD} = 2.5 V ±10%, or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency Range[1]	FCLK		0.0025	—	200	MHz
Load Capacitance	C_L	F_{CLK} < 100 MHz	—	—	15	pF
Duty Cycle	DC	$F_{CLK} \leq$ 160 MHz, measured at VDD/2	45	50	55	%
		F_{CLK} > 160 MHz, measured at VDD/2	40	50	60	%
Rise/Fall Time	t_r/t_f	20% - 80%, C_L = 5 pF	—	1	1.5	ns
Output High Voltage	VOH		V_{DD} – 0.6	—	—	V
Output Low Voltage	VOL		—	—	0.6	V
Period Jitter[2,3]	JPER	16, 20-QFN, 4 outputs running, 1 per VDDO	—	40	95	ps pk-pk
		10-MSOP or 20-QFN, all outputs running	—	70	155	
Cycle-to-Cycle Jitter[2,3]	JCC	16, 20-QFN, 4 outputs running, 1 per VDDO	—	50	90	ps pk
		10-MSOP or 20-QFN, all outputs running	—	70	150	
Period Jitter, VCXO[2,3]	JPER_VCXO	16, 20-QFN, 4 outputs running, 1 per VDDO	—	50	95	ps pk-pk
		10-MSOP or 20-QFN, all outputs running	—	70	155	
Cycle-to-Cycle Jitter, VCXO[2,3]	JCC_VCXO	16, 20-QFN, 4 outputs running, 1 per VDDO	—	50	90	ps pk
		10-MSOP or 20-QFN, all outputs running	—	70	150	

Notes:

1. Only two unique frequencies above 112.5 MHz can be simultaneously output.
2. Measured over 10k cycles. Jitter is only specified at the default high drive strength (50 Ω output impedance).
3. Jitter is highly dependent on device frequency configuration. Specifications represent a "worst case, real world" frequency plan; actual performance may be substantially better. Three-output 10MSOP package measured with clock outputs of 74.25, 24.576, and 48 MHz. Eight-output 20QFN package measured with clock outputs of 33.33, 74.25, 27, 24.576, 22.5792, 28.322, 125, and 48 MHz. Four-output, 16-QFN package measured with clock outputs of 33.333, 27, 28.322, and 48 MHz.

Table 8. 25 MHz Crystal Requirements[1,2]

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	—	25	—	MHz
Load Capacitance	C_L	6	—	12	pF
Equivalent Series Resistance	r_{ESR}	—	—	150	Ω
Crystal Max Drive Level	d_L	100	—	—	µW

Notes:
1. Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitance in addition to external 2 pF load capacitance (e.g., by using 4 pF capacitors on XA and XB). ClockBuilder Pro can be used to configure the internal load capacitors.
2. Refer to "AN551: Crystal Selection Guide" for more details.

Table 9. 27 MHz Crystal Requirements[1,2]

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	—	27	—	MHz
Load Capacitance	C_L	6	—	12	pF
Equivalent Series Resistance	r_{ESR}	—	—	150	Ω
Crystal Max Drive Level Spec	d_L	100	—	—	µW

Notes:
1. Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitance in addition to external 2 pF load capacitance (e.g., by using 4 pF capacitors on XA and XB). ClockBuilder Pro can be used to configure the internal load capacitors.
2. Refer to "AN551: Crystal Selection Guide" for more details.

Table 10. Thermal Characteristics (2-Layer Board)

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air[1]	10-MSOP	150	°C/W
			16-QFN	103	°C/W
			20-QFN	74.9	°C/W
Thermal Resistance Junction to Board	Ψ_{JB}	Still Air[1]	10-MSOP	82	°C/W
			16-QFN	37	°C/W
			20-QFN	9.94	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JT}	Still Air[1]	10-MSOP	0.84	°C/W
			16-QFN	4.26	°C/W
			20-QFN	1.3	°C/W

Notes:
1. Based on environment and board designed per JESD51-2A and JESD51-3.

Table 11. Thermal Characteristics (4-Layer Board)

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air[1]	10-MSOP	126	°C/W
			16-QFN	65	°C/W
			20-QFN	41	°C/W
Thermal Resistance Junction to Board	θ_{JB}	Junction to Board[2]	10-MSOP	84	°C/W
			16-QFN	48	°C/W
			20-QFN	16	°C/W
	Ψ_{JB}	Still Air[1]	10-MSOP	83	°C/W
			16-QFN	31	°C/W
			20-QFN	8.1	°C/W
Thermal Resistance Junction to Top Center	Ψ_{JT}	Still Air[1]	10-MSOP	0.74	°C/W
			16-QFN	3.8	°C/W
			20-QFN	0.98	°C/W

Notes:
1. Based on environment and board designed per JESD51-2A, JESD51-5, and JESD51-7.
2. Based on conditions set in JESD51-8.

Table 12. Thermal Characteristics (Junction-to-Case)

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Case[1]	θ_{JC}	Still Air	10-MSOP	36	°C/W
			16-QFN	82	°C/W
			20-QFN	51	°C/W

Notes:
1. Based on board designed per JESD51-1 (Top center of packages used).

Table 13. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	V_{DD_max}		–0.5 to 3.8	V
Input Voltage	V_{IN_P0-3}	Pins P0, P1, P2, P3	–0.5 to 3.8	V
	V_{IN_VC}	VC	–0.5 to (V_{DD}+0.3)	V
	$V_{IN_XA/B}$	Pins XA, XB	–0.5 to 1.3 V	V
Junction Temperature	T_J		–55 to 150	°C
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[2]	T_P		20–40	Sec

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

4. Typical Application

4.1. Si5350B Replaces Multiple Clocks and XOs

The Si5350B is a clock generation device that provides both synchronous and free-running clocks for applications where power, board size, and cost are critical. An application where both free-running and synchronous clocks are required is shown in Figure 1.

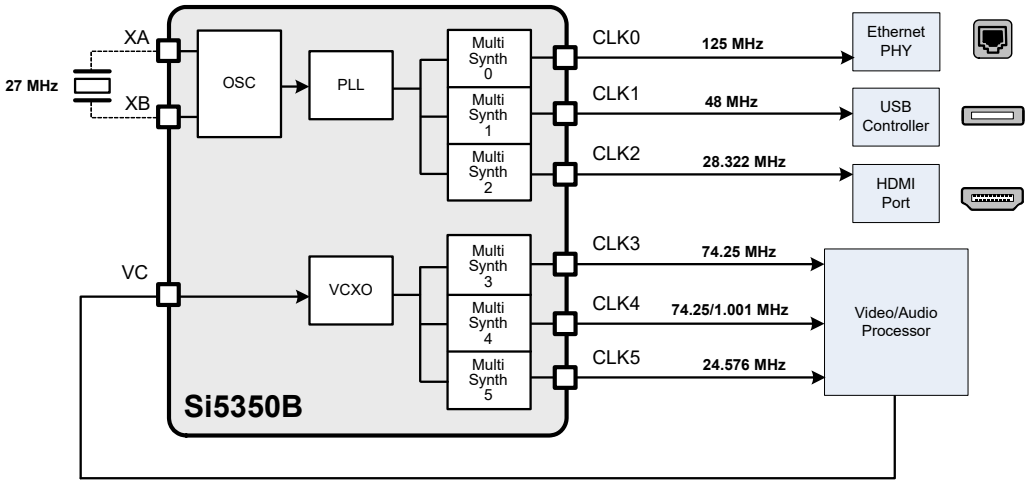
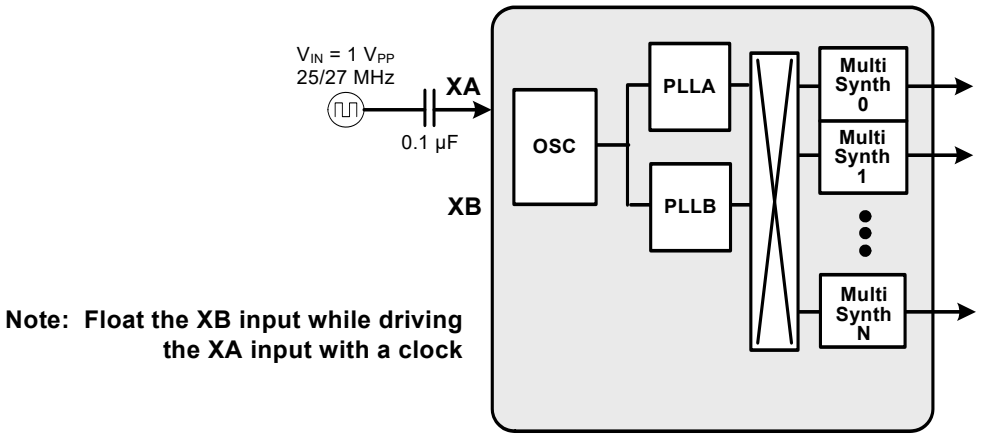


Figure 1. Example of an Si5350B in an Audio/Video Application

4.2. Applying a Reference Clock at XTAL Input

The Si5350B can be driven with a clock signal through the XA input pin.



Note: Float the XB input while driving the XA input with a clock

Figure 2. Si5350B Driven by a Clock Signal

4.3. HCSL Compatible Outputs

The Si5350B can be configured to support HCSL compatible swing when the VDDO of the output pair of interest is set to 2.5 V (i.e., VDDOA must be 2.5 V when using CLK0/1; VDDOB must be 2.5 V for CLK2/3 and so on).

The circuit in the figure below must be applied to each of the two clocks used, and one of the clocks in the pair must also be inverted to generate a differential pair. This functionality is only supported for the Si5350B in 10-MSOP or 20-QFN packages.

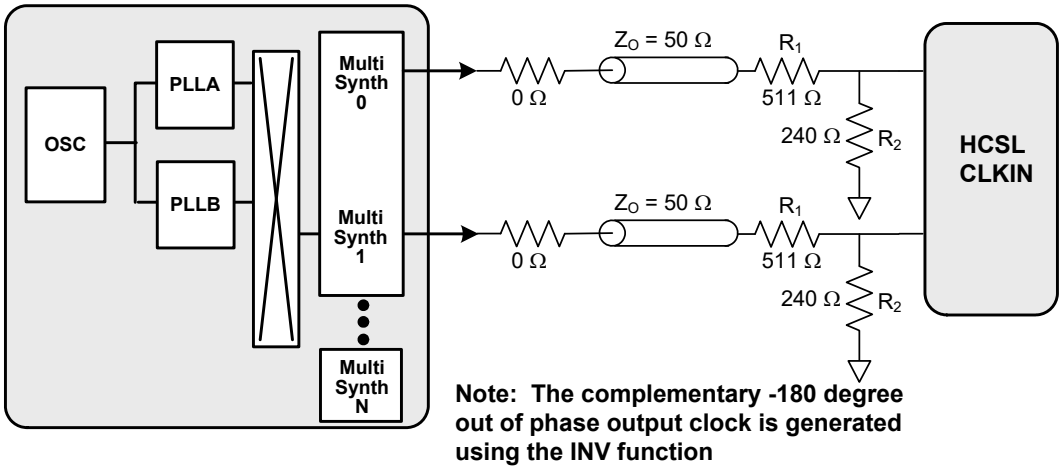


Figure 3. Si5350B Output is HCSL Compatible

5. Functional Description

The Si5350B features a high-frequency PLL, a high-frequency VCXO and a high-resolution fractional MultiSynth™ divider on each output. Block diagrams of 3-, 4-, and 8-output clock generators are shown in Figure 4. Free-running clocks are generated from the on-chip oscillator + PLL, and a separate voltage controlled oscillator (VCXO) is used to generate synchronous clocks. A fixed-frequency non-pullable standard AT-cut crystal provides frequency stability for both the internal oscillator and VCXO. The flexible synthesis architecture of the Si5350B generates up to eight non-integer related frequencies and any combination of free-running and/or synchronous clocks.

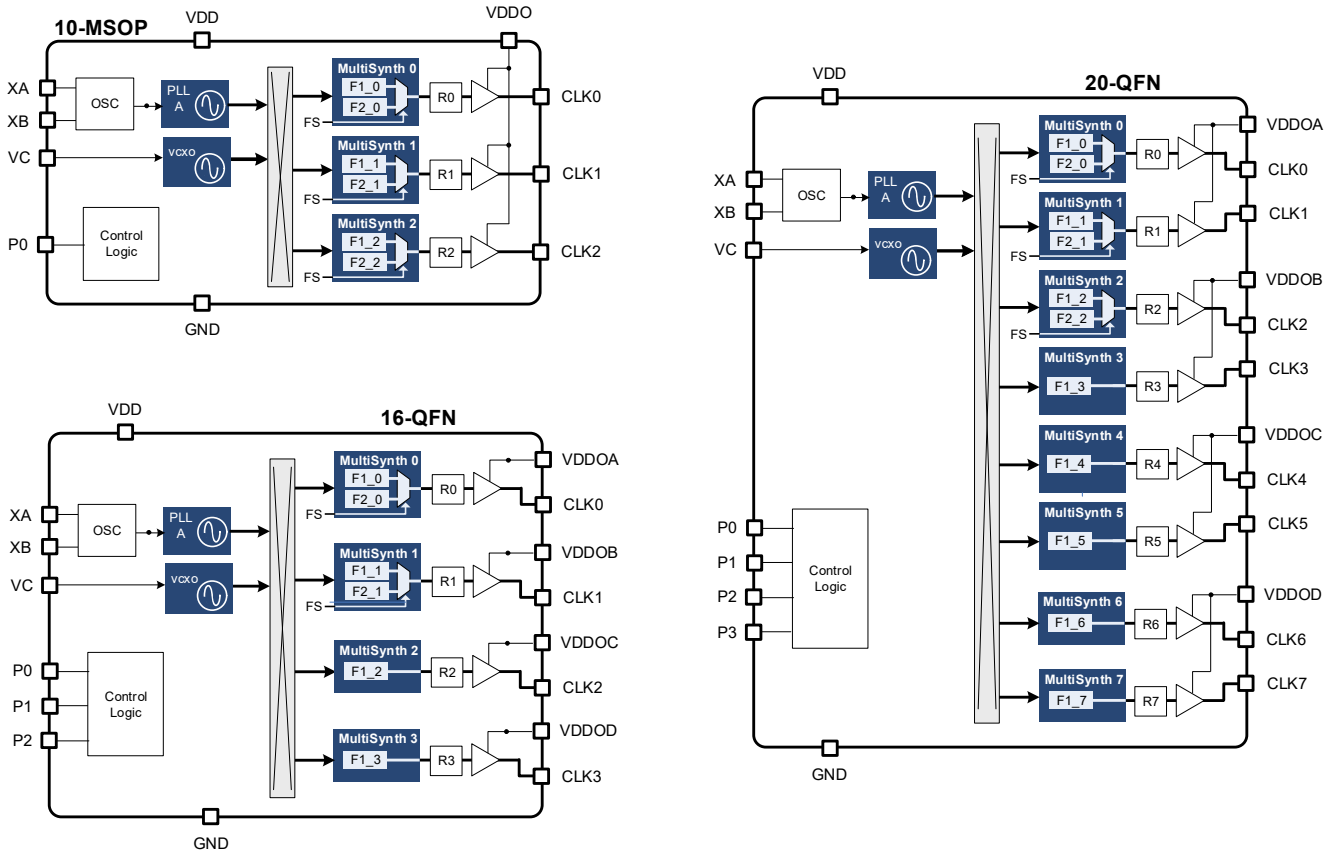


Figure 4. Block Diagrams of 3-Output, 4-Output, and 8-Output Si5350B Devices

6. Configuring the Si5350B

The Si5350B is a factory-programmed custom clock generator that is user definable with ClockBuilder Pro. ClockBuilder Pro provides a simple graphical interface that allows the user to enter input and output frequencies along with other custom features as described in the following sections. All synthesis calculations are automatically performed by ClockBuilder Pro to ensure an optimum configuration. A unique part number is assigned to each custom configuration.

6.1. Crystal Inputs (XA, XB)

The Si5350B uses a fixed-frequency non-pullable standard AT-cut crystal as a reference to synthesize its output clocks and to provide the frequency stability for the VCXO.

6.1.1. Crystal Frequency

The Si5350B can operate using either a 25 MHz or a 27 MHz crystal.

6.1.2. Internal XTAL Load Capacitors

Internal load capacitors are provided to eliminate the need for external components when connecting a XTAL to the Si5350B. The total internal XTAL load capacitance (C_L) can be selected to be 0, 6, 8, or 10 pF. XTALs with alternate load capacitance requirements are supported using additional external load capacitance ≤ 2 pF (e.g., by using ≤ 4 pF capacitors on XA and XB) as shown in Figure 5.

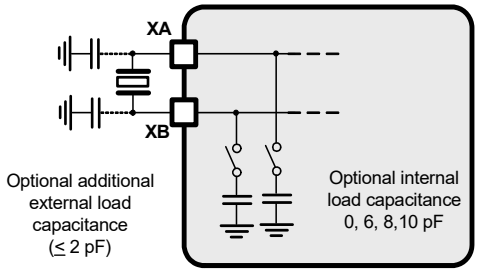


Figure 5. External XTAL with Optional Load Capacitors

6.2. Output Clocks (CLK0–CLK7)

The Si5350B is orderable as a 3-output (10-MSOP), 4-output (16-QFN), or 8-output (20-QFN) clock generator. Output clocks CLK0 to CLK2 can be ordered with two clock frequencies (F1_x, F2_x) which are selectable with the optional frequency select pins (FS0/1). See “6.3.3. Frequency Select (FS_0, FS_1)” for more details on the operation of the frequency select pins. Each output clock can select its reference either from the PLL or from the VCXO.

6.2.1. Output Clock Frequency

Outputs can be configured at any frequency from 2.5 kHz up to 200 MHz. However, only two unique frequencies above 112.5 MHz can be simultaneously output. For example, 125 MHz (CLK0), 130 MHz (CLK1), and 150 MHz (CLKx) is not allowed. Note that multiple copies of frequencies above 112.5 MHz can be provided, for example, 125 MHz could be provided on four outputs (CLKS0-3) simultaneously with 130 MHz on four different outputs (CLKs4-7).

6.2.2. .Spread Spectrum

Spread spectrum can be enabled on any of the clock outputs that use PLLA as its reference. Spread spectrum is useful for reducing electromagnetic interference (EMI). Enabling spread spectrum on an output clock modulates its frequency, which effectively reduces the overall amplitude of its radiated energy. Note that spread spectrum is not available on clocks synchronized to PLLB or to the VCXO.

The Si5350B supports several levels of spread spectrum allowing the designer to choose an ideal compromise between system performance and EMI compliance. An optional spread spectrum enable pin (SSEN) is configurable to enable or disable the spread spectrum feature. See “6.3.1. Spread Spectrum Enable (SSEN)” for details.

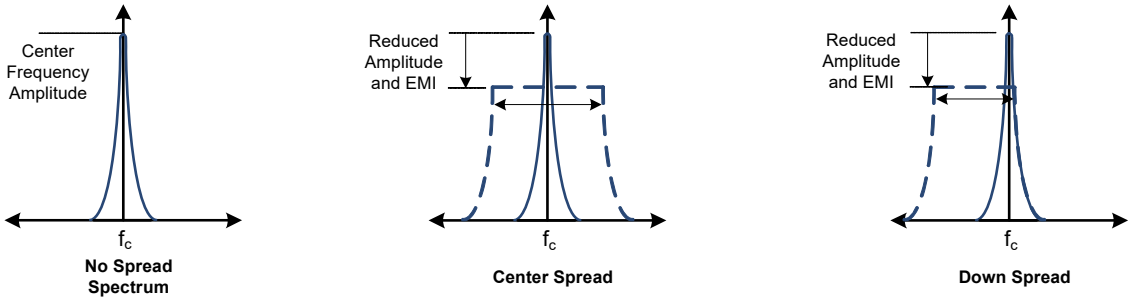


Figure 6. Available Spread Spectrum Profiles

6.2.3. Invert/Non-Invert

By default, each of the output clocks are generated in phase (non-inverted) with respect to each other. An option to invert any of the clock outputs is also available.

6.2.4. Output State When Disabled

There are up to three output enable pins configurable on the Si5350B as described in “6.3.4. Output Enable (OEB_0, OEB_1, OEB_2)” . The output state when disabled for each of the outputs is configurable as one of the following: disable low, disable high, or disable in high-impedance.

6.2.5. Powering Down Unused Outputs

Unused clock outputs can be completely powered down to conserve power.

6.3. Programmable Control Pins (P0–P3) Options

Up to four programmable control pins (P0-P3) are configurable allowing direct pin control of the following features:

6.3.1. Spread Spectrum Enable (SSEN)

An optional control pin allows disabling the spread spectrum feature for all outputs that were configured with spread spectrum enabled. Hold SSEN low to disable spread spectrum. The SSEN pin provides a convenient method of evaluating the effect of using spread spectrum clocks during EMI compliance testing.

6.3.2. Power Down (PDN)

An optional power down control pin allows a full shutdown of the Si5350B to minimize power consumption when its output clocks are not being used. The Si5350B is in normal operation when the PDN pin is held low and is in power down mode when held high. Power consumption when the device is in power down mode is indicated in Table 4 on page 5.

6.3.3. Frequency Select (FS_0, FS_1)

The Si5350B offers the option of configuring up to two frequencies per clock output (CLK0-CLK2) for either free-running or synchronous clocks. This is a useful feature for applications that need to support more than one free-running or synchronous clock rate on the same output. An example of this is shown in Figure 7. The FS pins select which frequency is generated from the clock output. In this example FS0 selects the output frequency on CLK0, and FS1 selects the frequency on CLK1.

FS0 Bit Level	Free-running Frequency
0	F1_0: 74.25 MHz
1	F2_0: $\frac{74.25}{1.001}$ MHz

FS1 Bit Level	Synchronous Frequency
0	F1_1: 24.576 MHz
1	F2_1: 22.5792 MHz

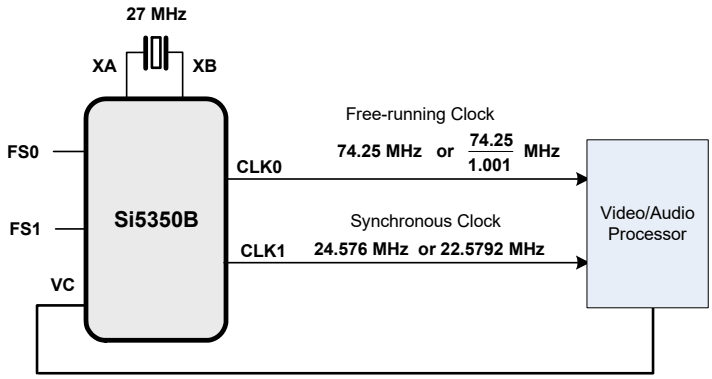


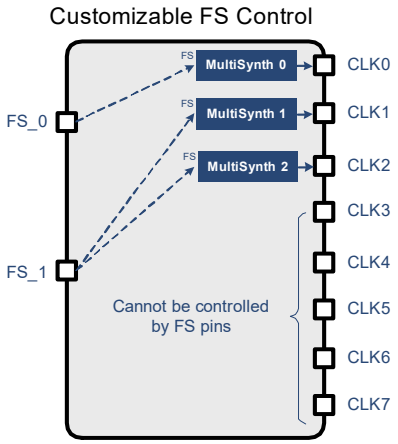
Figure 7. Example of Generating Two Clock Frequencies from the Same Clock Output

Up to two frequency select pins are available on the Si5350B. Each of the frequency select pins can be linked to CLK0, 1, and 2 for 20-QFN and 10-MSOP devices. 16-QFN devices allow frequency select on CLK0 and CLK1. See Figure 8 for an example of a potential 20-QFN frequency select configuration. In this example, FS_0 is linked to control clock frequency selection on CLK0; FS_1 can be used to control clock frequency selection on CLK1 and CLK2. Any other combination is also possible. The frequency select feature is not available for CLK3/4/5/6/7 in 20-QFN devices or for CLK2/3 in 16-QFN devices.

The Si5350B uses control circuitry to ensure that frequency changes are glitchless. This ensures that the clock always completes its last cycle before starting a new clock cycle of a different frequency.

FS_0	Output Frequency
0	F1_0
1	F2_0

FS_1	Output Frequency
0	F1_1, F1_2
1	F2_1, F2_2



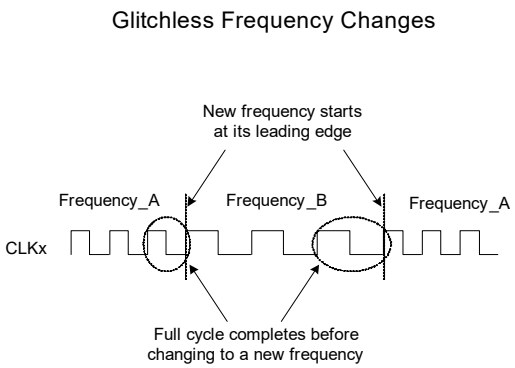


Figure 8. Example Configuration of a Pin-Controlled Frequency Select (FS)

6.3.4. Output Enable (OEB_0, OEB_1, OEB_2)

Up to three output enable pins (OEB_0/1/2) are available on the Si5350B. Each OEB pin can be linked to any of the output clocks. In the example shown in Figure 9, OEB_0 is linked to control CLK0, CLK3, and CLK5; OEB_1 is linked to control CLK6 and CLK7, and OEB_2 is linked to control CLK1, CLK2, CLK4, and CLK5. Any other combination is also possible. If more than one OEB pin is linked to the same CLK output, the pin forcing a disable state will be dominant. Clock outputs are enabled when the OEB pin is held low.

The output enable control circuitry ensures glitchless operation by starting the output clock cycle on the first leading edge after OEB is asserted (OEB = low). When OEB is released (OEB = high), the clock is allowed to complete its full clock cycle before going into a disabled state. This is shown in Figure 9. When disabled, the output state is configurable as disabled high, disabled low, or disabled in high-impedance.

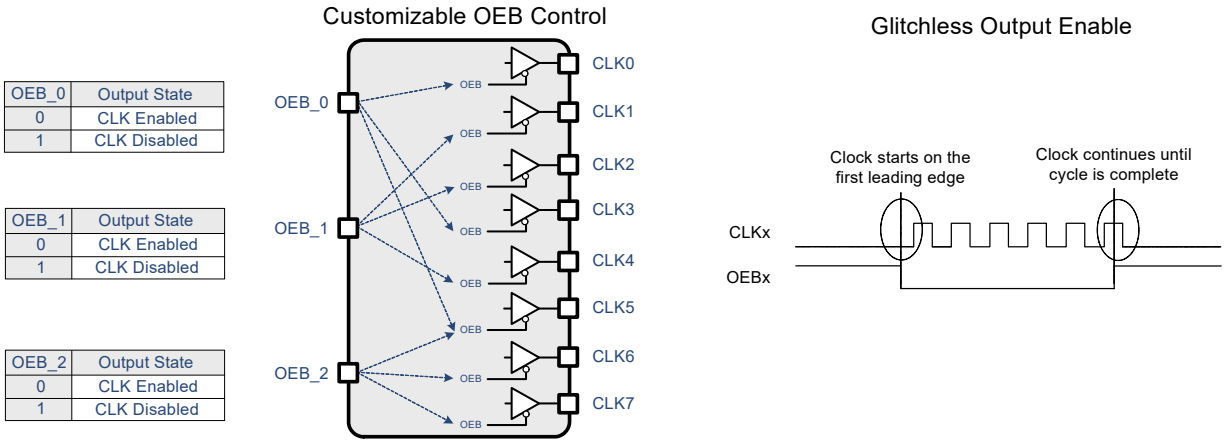


Figure 9. Example Configuration of a Pin-Controlled Output Enable

6.4. Voltage Control Input (VC)

The VCXO architecture of the Si5350B eliminates the need for an external pullable crystal. Only a standard, low-cost, fixed-frequency (25 or 27 MHz) AT-cut crystal is required.

The tuning range of the VCXO is configurable allowing for a wide variety of applications. Key advantages of the VCXO design in the Si5350B include high linearity, a wide operating range (linear from 10 to 90% of VDD), and reliable startup and operation. Refer to Table 5 on page 6 for VCXO specification details.

A unique feature of the Si5350B is its ability to generate multiple output frequencies controlled by the same control voltage applied to the VC pin. This replaces multiple PLLs or VCXOs that would normally be locked to the same reference. An example is illustrated in Figure 10.

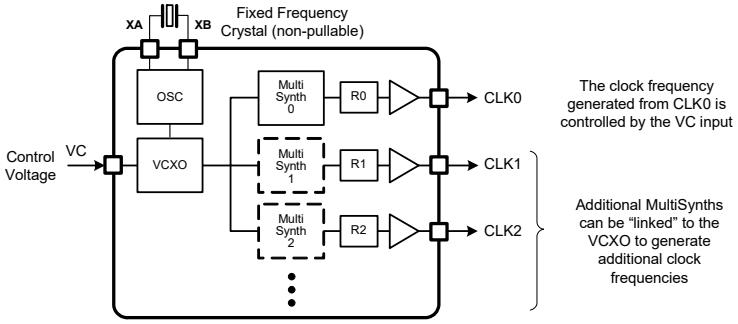


Figure 10. Using the Si5350B as a Multi-Output VCXO

6.4.1. Control Voltage Gain (kV)

The voltage level on the VC pin directly controls the output frequency. The rate of change in output clock frequency (kv) is configurable from 18 ppm/V up to 150 ppm/V. This allows a configurable pull range from ±30 ppm to ±240 ppm @ V_{DD} = 3.3 V as shown in Figure 11. Consult the factory for other pull range values.

A key advantage of the VCXO design in the Si5350B is its highly linear tuning range. This allows better control of PLL stability and jitter performance over the entire control voltage range.

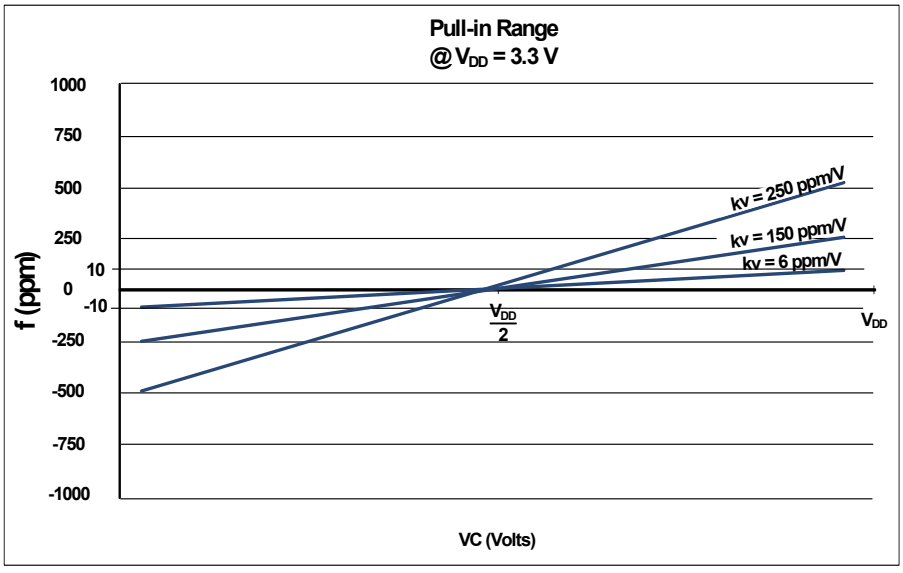


Figure 11. User-definable VCXO Pull Range

6.5. Design Considerations

The Si5350B is a self-contained clock generator that requires very few external components. The following general guidelines are recommended to ensure optimum performance.

6.5.1. Power Supply Decoupling/Filtering

The Si5350B has built-in power supply filtering circuitry to help keep the number of external components to a minimum. All that is recommended is one 0.1 to 1.0 µF decoupling capacitor per power supply pin. This capacitor should be mounted as close to the VDD and VDDO pins as possible without using vias.

6.5.2. Power Supply Sequencing

The VDD and VDDOx (i.e., VDDO0, VDDO1, VDDO2, VDDO3) power supply pins have been separated to allow flexibility in output signal levels. Power supply sequencing for VDD and VDDOx requires that all VDDOx be powered up either before or at the same time as VDD. Unused VDDOx pins should be tied to VDD.

6.5.3. External Crystal

The external crystal should be mounted as close to the pins as possible using short PCB traces. The XA and XB traces should be kept away from other high-speed signal traces. See “AN551: Crystal Selection Guide” for more details.

6.5.4. External Crystal Load Capacitors

The Si5350B provides the option of using internal and external crystal load capacitors. If external load capacitors are used, they should be placed as close to the XA/XB pads as possible. See “AN551: Crystal Selection Guide” for more details.

6.5.5. Unused Pins

Unused control pins (P0–P4) should be tied to GND.

Unused voltage control pin should be tied to GND.

Unused output pins (CLK0–CLK7) should be left floating.

Unused XA/XB pins should be left floating. Refer to "4.2. Applying a Reference Clock at XTAL Input" on page 11 when using XA as a clock input pin.

Unused VDD0x pins should be tied to VDD.

6.5.6. Trace Characteristics

The Si5350B features various output drive strength settings. It is recommended to configure the trace characteristics as shown in Figure 12 when the default high output drive setting is used.

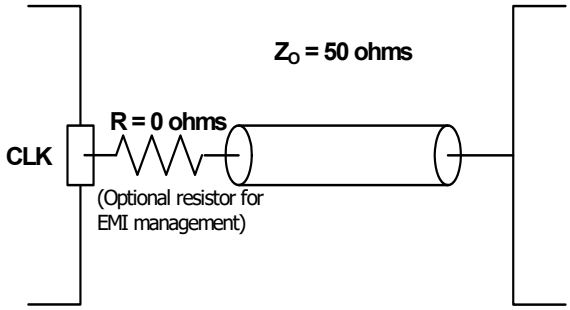


Figure 12. Recommended Trace Characteristics with Default Drive Strength Setting

7. Pin Descriptions

7.1. 20-pin QFN

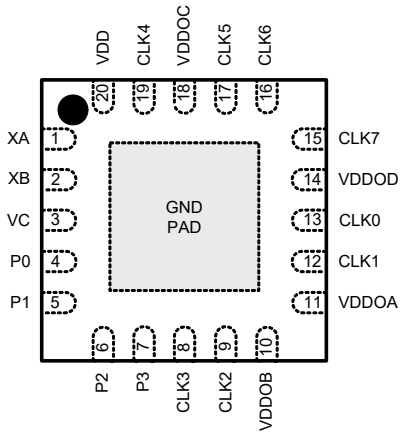


Figure 13. Si5350B 20-QFN Top View

Table 14. Si5350B 20-QFN Pin Descriptions

Pin Name	Pin Number	Pin Type*	Function
XA	1	I	Input pin for external XTAL
XB	2	I	Input pin for external XTAL
VC	3	I	VCXO control voltage input
CLK0	13	O	Output clock 0
CLK1	12	O	Output clock 1
CLK2	9	O	Output clock 2
CLK3	8	O	Output clock 3
CLK4	19	O	Output clock 4
CLK5	17	O	Output clock 5
CLK6	16	O	Output clock 6
CLK7	15	O	Output clock 7
P0	4	I	User configurable input pin 0. See Section 6.3.
P1	5	I	User configurable input pin 1. See Section 6.3.
P2	6	I	User configurable input pin 2. See Section 6.3.
P3	7	I	User configurable input pin 3. See Section 6.3.
VDD	20	P	Core voltage supply pin. See Section 6.5.2.
VDDOA	11	P	Output voltage supply pin for CLK0 and CLK1. See Section 6.5.2.
VDDOB	10	P	Output voltage supply pin for CLK2 and CLK3. See Section 6.5.2.
VDDOC	18	P	Output voltage supply pin for CLK4 and CLK5. See Section 6.5.2.
VDDOD	14	P	Output voltage supply pin for CLK6 and CLK7. See Section 6.5.2.
GND	Center Pad	P	Ground
***Note:** Pin Types: I = Input, O = Output, P = Power.			

7.2. 16-Pin QFN

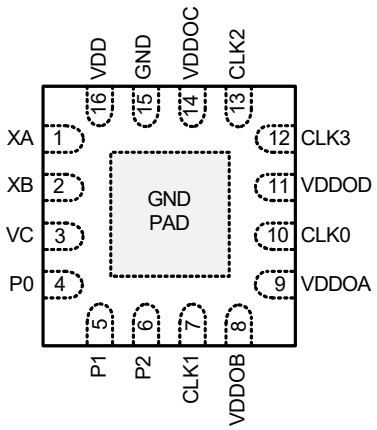


Figure 14. Si5350B 16-Pin QFN Top View

Table 15. Si5350B 16-QFN Pin Descriptions

Pin Name	Pin Number	Pin Type*	Function
XA	1	I	Input pin for external crystal.
XB	2	I	Input pin for external crystal.
VC	3	I	VCXO control voltage input.
P0	4	I	User configurable input P0. See Section 6.3.
P1	5	I	User configurable input P1. See Section 6.3.
P2	6	I	User configurable input P2. See Section 6.3.
CLK1	7	O	Output Clock 1.
VDDOB	8	P	Output voltage supply pin for CLK1. See Section 6.5.2.
VDDOA	9	P	Output voltage supply pin for CLK0. See Section 6.5.2.
CLK0	10	O	Output Clock 0. See Section 6.5.2.
VDDOD	11	P	Output voltage supply pin for CLK3. See Section 6.5.2.
CLK3	12	O	Output Clock 3. See Section 6.5.2.
CLK2	13	O	Output Clock 2. See Section 6.5.2.
VDDOC	14	P	Output voltage supply pin for CLK2. See Section 6.5.2.
GND	15	GND	Ground.
VDD	16	P	Core voltage supply pin. See Section 6.5.2.
GND PAD	Center Pad	GND	Ground pad. Use multiple vias to ensure a solid path to Ground.
***Note:** I = Input, O = Output, P = Power; GND = Ground. Input pins are not internally pulled up.			

7.3. 10-Pin MSOP

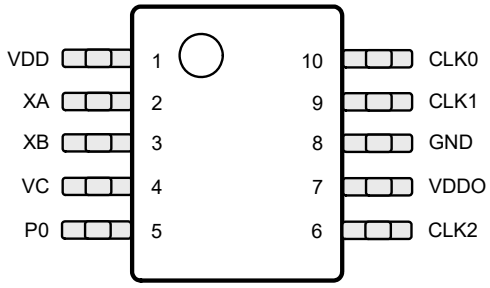


Figure 15. Si5350B 10-MSOP Top View

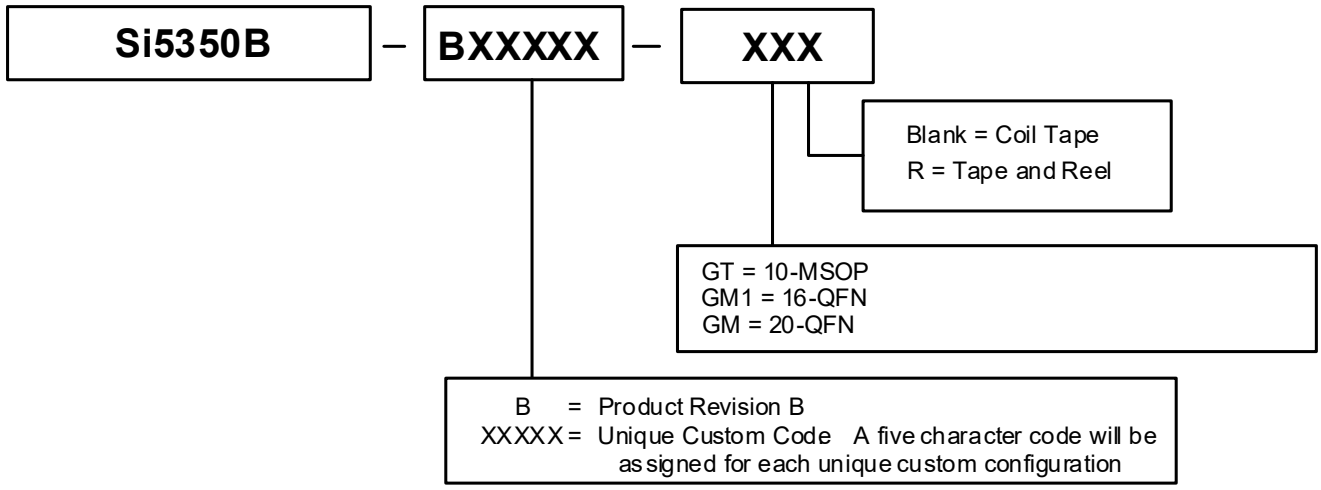
Table 16. Si5350B 10-MSOP Pin Descriptions

Pin Name	Pin Number	Pin Type*	Function
XA	2	I	Input pin for external XTAL.
XB	3	I	Input pin for external XTAL.
VC	4	I	VCXO control voltage input.
CLK0	10	O	Output clock 0.
CLK1	9	O	Output clock 1.
CLK2	6	O	Output clock 2.
P0	5	I	User configurable input pin 0. See Section 6.3.
VDD	1	P	Core voltage supply pin. See Section 6.5.2.
VDDO	7	P	Output supply pin for CLK0, CLK1, and CLK2. See Section 6.5.2.
GND	8	P	Ground.
***Note:** Pin Types: I = Input, O = Output, P = Power.			

8. Ordering Information

Factory programmed Si5350B devices can be requested through ClockBuilder Pro. A unique part number is assigned to each custom configuration as indicated in Figure 16. Use ClockBuilder Pro to create custom part numbers or consult a Skyworks Solutions sales representative for other custom NVM configurations.

The Si5351x-B20QFN-EVB evaluation kit, along with ClockBuilder Pro, enables easy testing of any Si5350B frequency plan. ClockBuilder Pro makes it simple to emulate all three Si5350B packages, including the 10-MSOP, 20-QFN, and 16-QFN, on the same evaluation board.



Evaluation Boards

Si535x-B20QFN-EVB – For evaluation of:
Si5350B-Bxxxxx-GM (20-QFN)
Si5350B-Bxxxxx-GM1 (16-QFN)
Si5350B-Bxxxxx-GT (10-MSOP)

Figure 16. Custom Clock Part Numbers

9. Packaging

9.1. 20-Pin QFN Package Outline

Figure 17 illustrates the package details for the Si5350B-B in a 20-pin QFN package. Table 17 lists the values for the dimensions shown in the illustration.

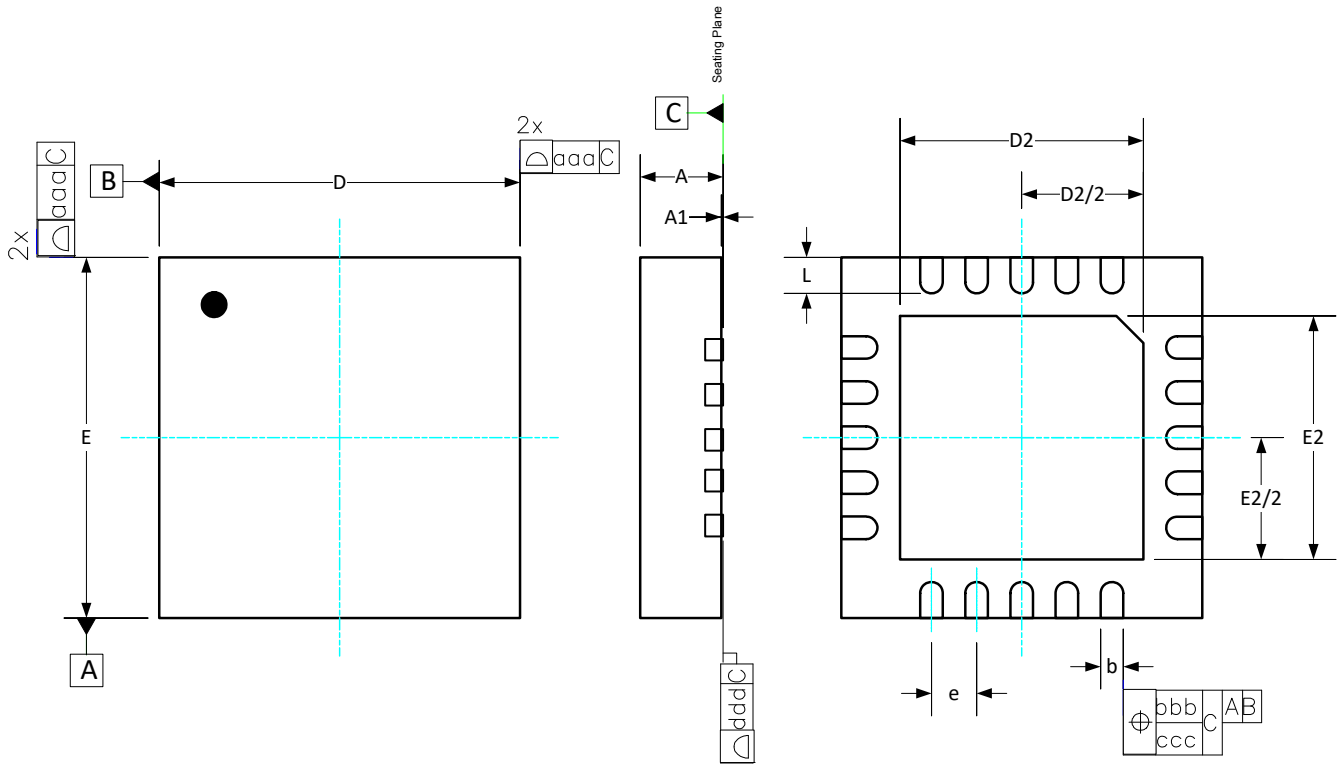


Figure 17. 20-pin QFN Package Drawing

Table 17. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	—	0.05
b	0.20	0.25	0.30
D		4.00 BSC	
D2	2.65	2.70	2.75
e		0.50 BSC	
E		4.00 BSC	
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MO-220, variation VGGD-5.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2. Land Pattern: 20-Pin QFN

Figure 18 shows the recommended land pattern details for the Si5350 in a 20-Pin QFN package. Table 18 lists the values for the dimensions shown in the illustration.

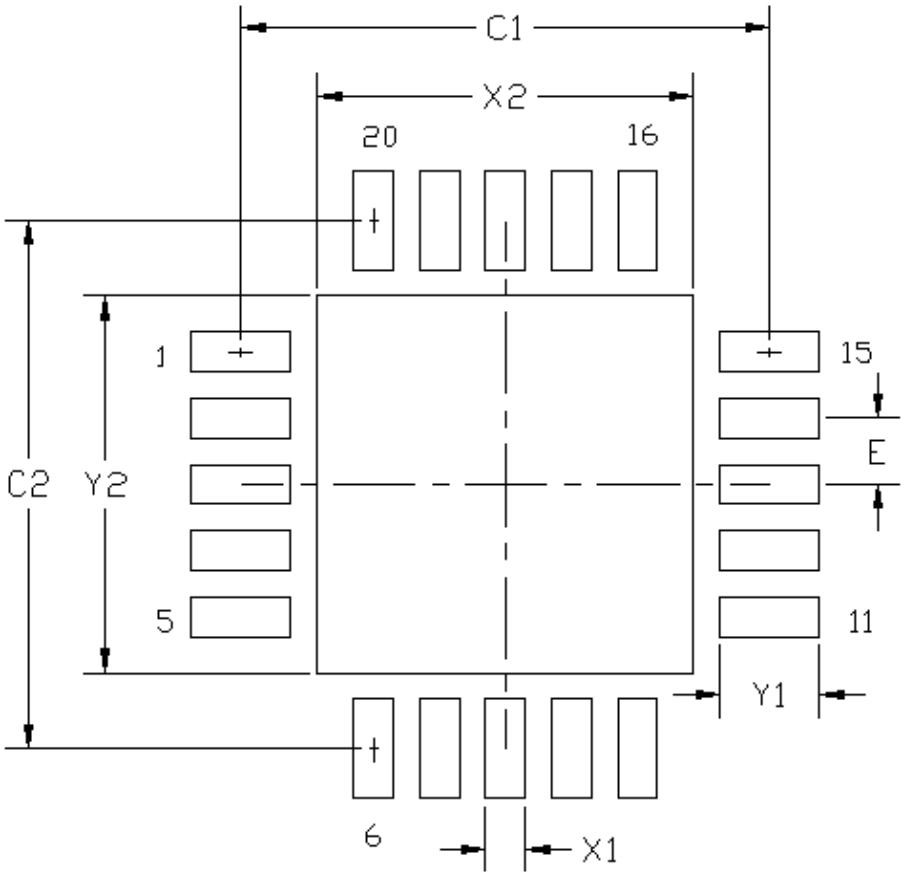


Figure 18. 20-Pin QFN Land Pattern

Table 18. PCB Land Pattern Dimensions

Symbol	Millimeters
C1	4.0
C2	4.0
E	0.50 BSC
X1	0.30
X2	2.70
Y1	0.80
Y2	2.70

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body components.

9.3. 16-Pin QFN Package Outline

Figure 19 illustrates the package details for the Si5350B-B in a 16-QFN package. Table 19 lists the values for the dimensions shown in the illustration.

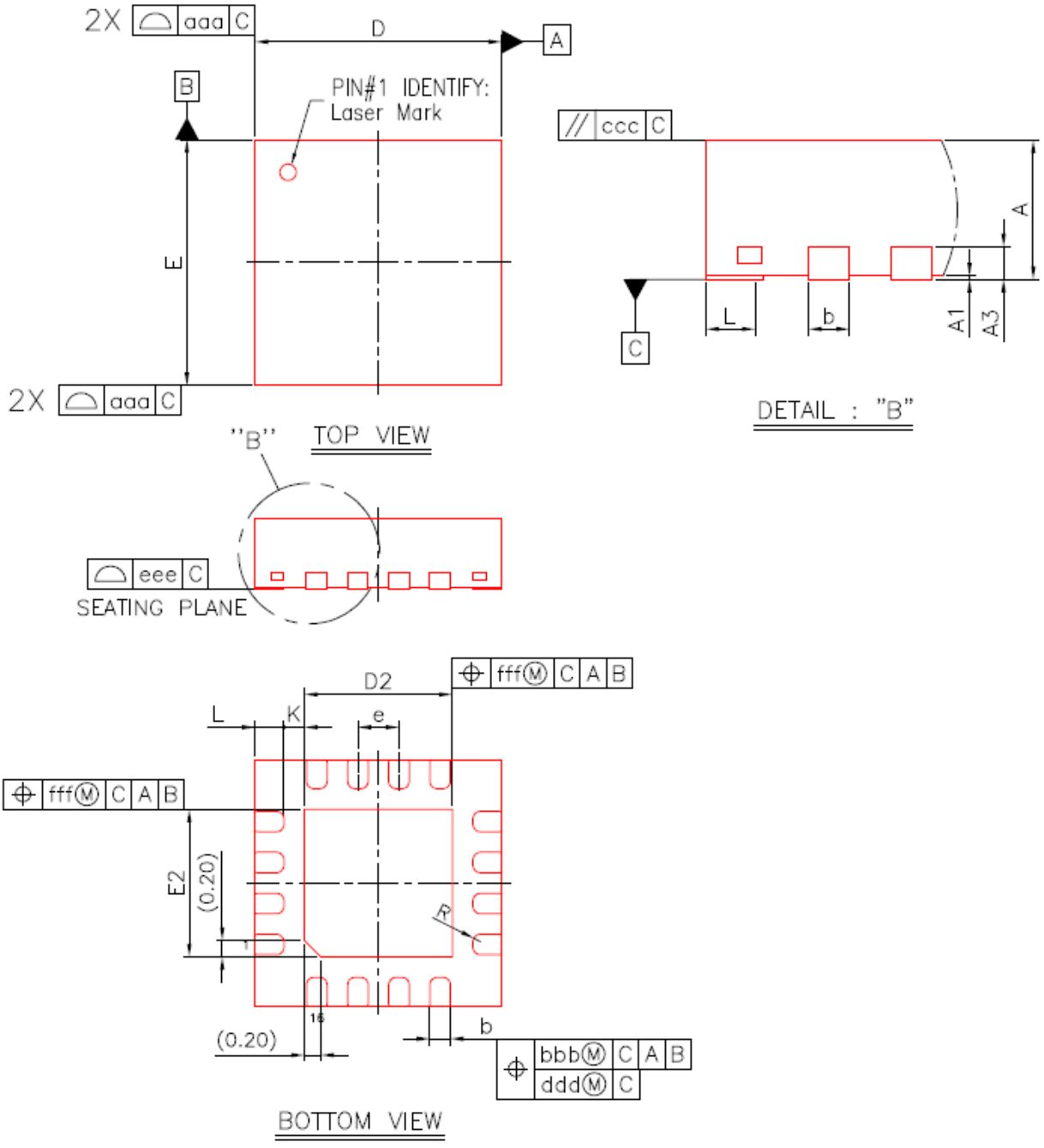


Figure 19. 16-Pin QFN Package Drawing

Table 19. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D		3.0 BSC	
D2	1.70	1.80	1.90
e		0.50 BSC	
E		3.0 BSC	
E2	1.70	1.80	1.90
L	0.25	0.35	0.45
K	0.20	—	—
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.4. Land Pattern: 16-Pin QFN

Figure 20 shows the recommended land pattern details for the Si5350 in a 16-QFN package. Table 20 lists the values for the dimensions shown in the illustration.

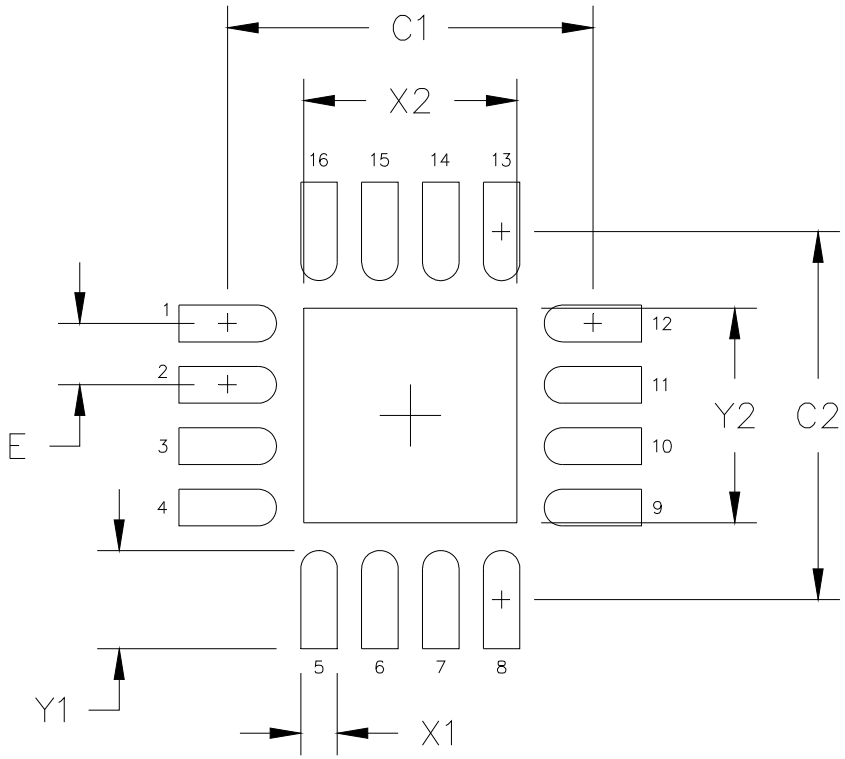


Figure 20. 16-Pin QFN Land Pattern

Table 20. PCB Land Pattern Dimensions

Symbol	Millimeters
C1	3.00
C2	3.00
E	0.50
X1	0.30
Y1	0.75
X2	1.80
Y2	1.80

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This land pattern design is based on IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
8. A 2x2 array of 0.65 mm square openings on a 0.90 mm pitch should be used for the center ground pad.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body components.
11. The above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

9.5. 10-Pin MSOP Package Outline

Figure 21 illustrates the package details for the Si5350B-B in a 10-pin MSOP package. Table 21 lists the values for the dimensions shown in the illustration.

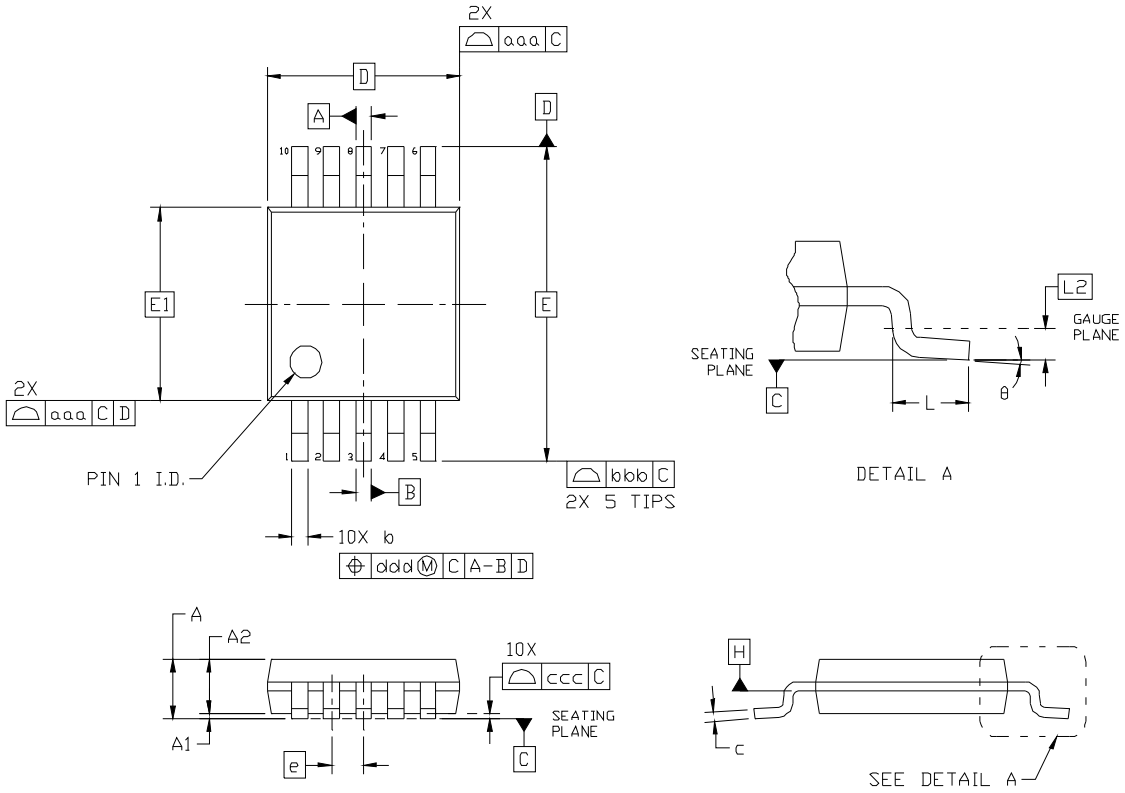


Figure 21. 10-pin MSOP Package Drawing

Table 21. 10-MSOP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
b	0.17	—	0.33
c	0.08	—	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
L	0.40	0.60	0.80
L2	0.25 BSC		
q	0	—	8
aaa	—	—	0.20
bbb	—	—	0.25
ccc	—	—	0.10
ddd	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation C
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.6. Land Pattern: 10-Pin MSOP

Figure 22 shows the recommended land pattern details for the Si5350B-B in a 10-Pin MSOP package. Table 22 lists the values for the dimensions shown in the illustration.

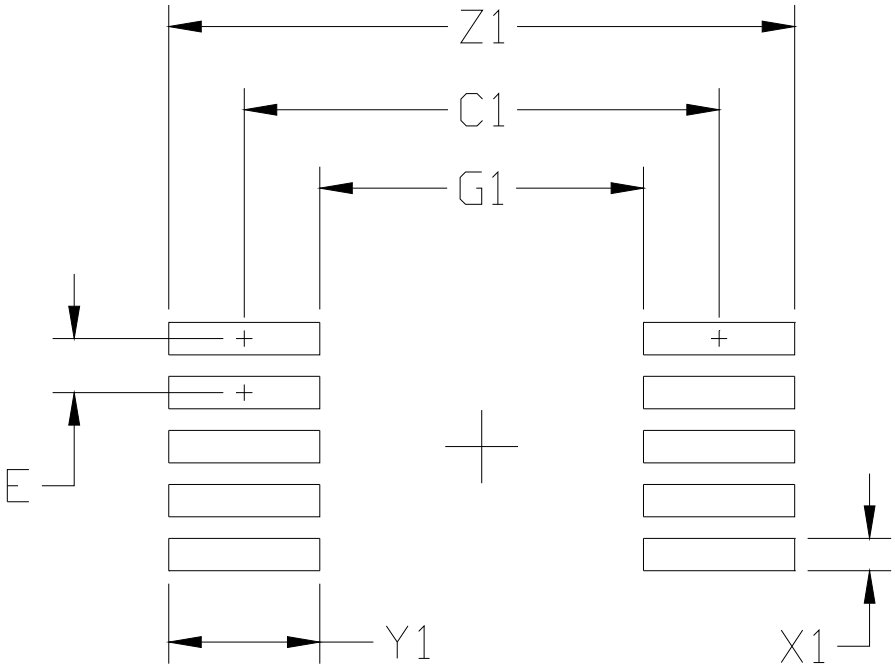


Figure 22. 10-Pin MSOP Land Pattern

Table 22. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
C1	4.40 REF	
E	0.50 BSC	
G1	3.00	—
X1	—	0.30
Y1	1.40 REF	
Z1	—	5.80

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ASME Y14.5M-1994.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body components.

10. Top Marking

10.1. 20-Pin QFN Top Marking

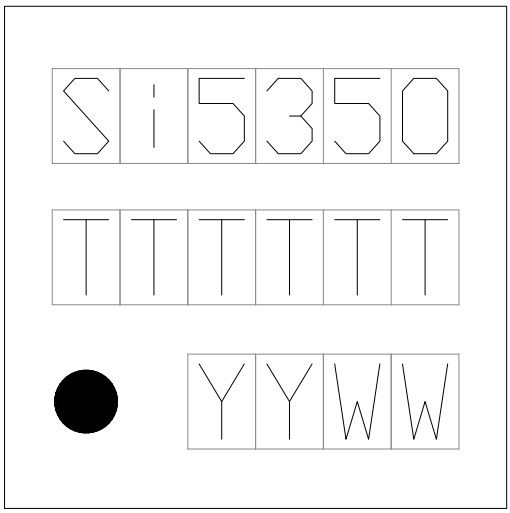


Figure 23. 20-Pin QFN Top Marking

10.2. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Filled Circle = 0.50 mm Diameter (Bottom-Left Corner)	
Font Size:	0.60 mm (24 mils)	
Line 1 Mark Format	Device Part Number	Si5350
Line 2 Mark Format:	TTTTTT = Mfg Code*	Manufacturing Code from the Assembly Purchase Order Form.
Line 3 Mark Format:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly date.
***Note:** The code shown in the “TTTTTT” line does not correspond to the orderable part number or frequency plan. It is used for package assembly quality tracking purposes only.		

10.3. 16-Pin QFN Top Marking

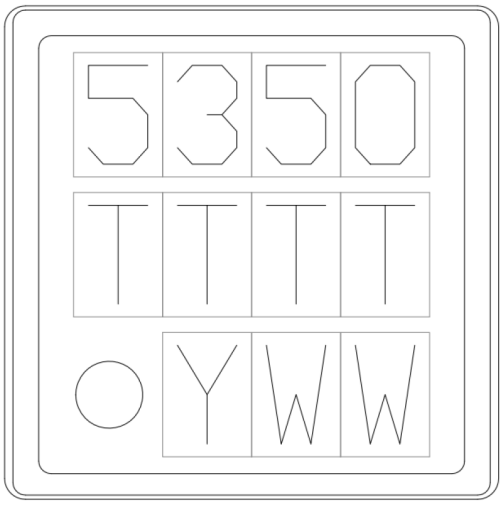


Figure 24. 16-Pin QFN Top Marking

10.4. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Circle (Bottom-Left Corner)	
Font Size:	0.60 mm (24 mils)	
Line 1 Mark Format	Device Part Number	5350
Line 2 Mark Format:	TTTT = Mfg Code*	Manufacturing Code from the Assembly Purchase Order Form.
Line 3 Mark Format:	YWW = Date Code	Assigned by the Assembly House. Y = Last digit of the current year. WW = Work week of the assembly date.
***Note:** The code shown in the "TTTT" line does not correspond to the orderable part number or frequency plan. It is used for package assembly quality tracking purposes only.		

10.5. 10-Pin MSOP Top Marking

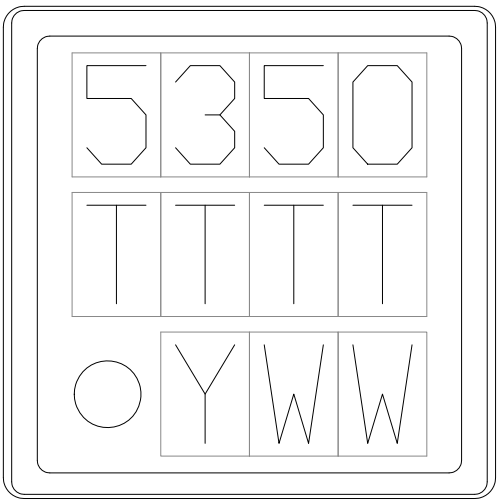


Figure 25. 10-Pin MSOP Top Marking

10.6. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Mold Dimple (Bottom-Left Corner)	
Font Size:	0.60 mm (24 mils)	
Line 1 Mark Format	Device Part Number	Si5350
Line 2 Mark Format:	TTTT = Mfg Code*	Line 2 from the “Markings” section of the Assembly Purchase Order form.
Line 3 Mark Format:	YWW = Date Code	Assigned by the Assembly House. Y = Last Digit of Current Year (Ex: 2013 = 3) WW = Work Week of Assembly Date.
***Note:** The code shown in the “TTTT” line does not correspond to the orderable part number or frequency plan. It is used for package assembly quality tracking purposes only.		

Revision History

Revision 1.2

March, 2020

- Added "1. Ordering Guide" on page 2.
- Updated "3. Electrical Specifications" on page 5.
  - Updated Tables 5, 7, 12, and 13 to include 16-QFN parameters.
  - Updated thermal characteristics tables to include Table 10 (2-Layer Board), Table 11 (4-Layer Board), and Table 12 (Junction-to-Case).
- Updated "4. Typical Application" on page 11.
  - Updated "4.3. HCSL Compatible Outputs" on page 12.
- Updated "5. Functional Description" on page 13.
- Updated "6. Configuring the Si5350B" on page 14.
  - Updated "6.2. Output Clocks (CLK0–CLK7)" on page 14.
  - Updated "6.3.3. Frequency Select (FS_0, FS_1)" on page 15.
  - Updated "6.5.5. Unused Pins" on page 19.
- Updated "7. Pin Descriptions" on page 20.
  - Added 16-QFN information.
- Updated "8. Ordering Information" on page 23.
  - Updated EVB and 16-QFN information.
- Updated "9. Packaging" on page 24.
  - Added 16-QFN information.

Revision 1.1

August, 2018

- Updated "8. Ordering Information" on page 23.
  - Changed “Blank = Bulk” to “Blank = Coil Tape” in Figure 16.

Revision 1.0

April, 2015

- Extended frequency range from 8 MHz–160 MHz to 2.5 MHz–200 MHz.
- Updated block diagrams for clarity.
- Added complete Si5350/1 family table, Table 1.
- Added top mark information.
- Added land pattern drawings.
- Added PowerUp Time, PLL Bypass mode, Table 5.
- Clarified Down Spread step sizes in Table 5.
- Updated max jitter specs (typ unchanged) in Table 7.
- Clarified power supply sequencing requirement, Section 6.5.2.

Revision 0.75

October, 2012

- Initial release.

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