Si8281/82/83/84 Data Sheet

SiC FET-Ready ISODrivers with Integrated DC-DC Converters

The Si828x family (Si8281/82/83/84) is comprised of isolated, high-current gate drivers with integrated system safety and feedback functions. These devices are ideal for driving Silicon Carbide (SiC) FETs, power MOSFETs, and IGBTs used in a wide variety of inverter and motor control applications. The Si828x isolated gate drivers utilize Skyworks' proprietary silicon isolation technology, supporting up to 5.0 kVrms withstand voltage per UL1577. This technology enables higher-performance, reduced variation with temperature and age, tighter part-to-part matching, and superior common-mode rejection compared to other isolated gate driver technologies.

In addition to the gate driver, the Si828x family integrates a dc-dc controller for simple implementation of an isolated supply for the driver side. The Si828x dc-dc controller can be ordered in two different configurations depending on what system voltage rails are available and the amount of power needed. The Si8281 and Si8283 have integrated power switches but are limited in dc-dc voltage input to the device bias. The Si8282 and Si8284 utilize an external power switch and are able to accept much higher voltage input power. User-adjustable frequency for minimizing emissions, a soft-start function for safety, and shut-down capability are available options. The device requires only minimal passive components and a miniature transformer.

The input to the device is a complementary digital input that can be utilized in several configurations. The input side of the isolation also has several control and feedback digital signals. The controller to the device receives information about the driver side power state and fault state of the device and recovers the device from faults through an active-low reset pin.

On the output side, Si828x devices provide separate pull-up and pull-down pins for the gate. A dedicated DSAT pin detects a desaturation condition and immediately shuts down the driver in a controlled manner using soft shutdown. The Si828x devices also integrate a Miller clamp to assure a strong turn-off of the power switch.

Automotive Grade is available. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Industrial Applications

- SiC/IGBT/ MOSFET gate drives
- Industrial and renewable energy inverters
- AC, Brushless, and DC motor controls
- Variable-speed motor controllers
- Isolated switch mode power supplies

Automotive Applications

- Hybrid electric and electric vehicles
- Traction inverters
- On-board chargers
- Inductive chargers
- DC-DC converters

Safety Regulatory Approvals

- UL 1577 recognized: 5000 V_{RMS} for 1 minute
- CSA approval: IEC 62368-1 (reinforced insulation)
- VDE approval: EN 62368-1 (reinforced insulation)
- CQC certification approval: GB4943.1-2011 (reinforced insulation)

KEY FEATURES

- System Safety Features
  - DESAT detection
  - FAULT feedback
  - Undervoltage Lock Out (UVLO) including 13 and 15 V for SiC FET
  - Soft shutdown on fault condition
  - Ultra-fast short circuit protection << 1 µs
  - Robust reference design for current boost, DESAT adjustment, soft shutdown tuning, and external Miller clamp transistor
- High-performance isolation technology
- High CMTI 125 kV/µs
- 30 V driver-side supply voltage
- Integrated Miller clamp
- Power ready pin
- Complementary driver control input
- Compact packages: 20 and 24-pin wide-body SOIC
- Integrated DC-DC converter
  - Feedback-controlled converter with dithering for low EMI
  - DC-DC converter efficiency of 83%
  - Shutdown, frequency, and soft-start controls
- Automotive-grade OPNs available
  - PPAP documentation support
  - IMDS and CAMDS listing support
  - AEC-Q100 Qualified
- Temp range: –40 to 125 °C

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1. Si8281/82/83/84 Ordering Guide

Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an “-A” in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 1.1. Si8281/82/83/84 Ordering Guide

Ordering Part Number (OPN)	A-Grade OPN	DC/DC Features						Package
		UVLO (V)	Shutdown	Soft Start	Frequency Control	External Switch	Isolation Rating (kVrms)	
Si8281BC-IS	Si8281BC-AS	9	No	No	No	No	3.75	WB SOIC-20
Si8281CC-IS	Si8281CC-AS	12	No	No	No	No	3.75	WB SOIC-20
Si8281DC-IS	Si8281DC-AS	13	No	No	No	No	3.75	WB SOIC-20
Si8281EC-IS	Si8281EC-AS	15	No	No	No	No	3.75	WB SOIC-20
Si8282BC-IS	Si8282BC-AS	9	No	No	No	Yes	3.75	WB SOIC-20
Si8282CC-IS	Si8282CC-AS	12	No	No	No	Yes	3.75	WB SOIC-20
Si8282DC-IS	Si8282DC-AS	13	No	No	No	Yes	3.75	WB SOIC-20
Si8282EC-IS	Si8282EC-AS	15	No	No	No	Yes	3.75	WB SOIC-20
Si8283BC-IS	Si8283BC-AS	9	Yes	Yes	Yes	No	3.75	WB SOIC-24
Si8283CC-IS	Si8283CC-AS	12	Yes	Yes	Yes	No	3.75	WB SOIC-24
Si8283DC-IS	Si8283DC-AS	13	Yes	Yes	Yes	No	3.75	WB SOIC-24
Si8283EC-IS	Si8283EC-AS	15	Yes	Yes	Yes	No	3.75	WB SOIC-24
Si8284BC-IS	Si8284BC-AS	9	Yes	Yes	Yes	Yes	3.75	WB SOIC-24
Si8284CC-IS	Si8284CC-AS	12	Yes	Yes	Yes	Yes	3.75	WB SOIC-24
Si8284DC-IS	Si8284DC-AS	13	Yes	Yes	Yes	Yes	3.75	WB SOIC-24
Si8284EC-IS	Si8284EC-AS	15	Yes	Yes	Yes	Yes	3.75	WB SOIC-24
Si8281BD-IS	Si8281BD-AS	9	No	No	No	No	5	WB SOIC-20
Si8281CD-IS	Si8281CD-AS	12	No	No	No	No	5	WB SOIC-20
Si8281DD-IS	Si8281DD-AS	13	No	No	No	No	5	WB SOIC-20
Si8281ED-IS	Si8281ED-AS	15	No	No	No	No	5	WB SOIC-20
Si8282BD-IS	Si8282BD-AS	9	No	No	No	Yes	5	WB SOIC-20
Si8282CD-IS	Si8282CD-AS	12	No	No	No	Yes	5	WB SOIC-20
Si8282DD-IS	Si8282DD-AS	13	No	No	No	Yes	5	WB SOIC-20
Si8282ED-IS	Si8282ED-AS	15	No	No	No	Yes	5	WB SOIC-20

Ordering Part Number (OPN)	A-Grade OPN	DC/DC Features						Package
		UVLO (V)	Shutdown	Soft Start	Frequency Control	External Switch	Isolation Rating (kVrms)	
Si8283BD-IS	Si8283BD-AS	9	Yes	Yes	Yes	No	5	WB SOIC-24
Si8283CD-IS	Si8283CD-AS	12	Yes	Yes	Yes	No	5	WB SOIC-24
Si8283DD-IS	Si8283DD-AS	13	Yes	Yes	Yes	No	5	WB SOIC-24
Si8283ED-IS	Si8283ED-AS	15	Yes	Yes	Yes	No	5	WB SOIC-24
Si8284BD-IS	Si8284BD-AS	9	Yes	Yes	Yes	Yes	5	WB SOIC-24
Si8284CD-IS	Si8284CD-AS	12	Yes	Yes	Yes	Yes	5	WB SOIC-24
Si8284DD-IS	Si8284DD-AS	13	Yes	Yes	Yes	Yes	5	WB SOIC-24
Si8284ED-IS	Si8284ED-AS	15	Yes	Yes	Yes	Yes	5	WB SOIC-24

Note:

1. Add an "R" at the end of the Part Number to denote Tape and Reel option.
2. All packages are RoHS-compliant with peak solder reflow temperatures of 260° C according to JEDEC industry-standard classifications.
3. A-grade OPNs are AEC-Q100 qualified.
4. “Si” and “SI” are used interchangeably.
5. Automotive-Grade devices (with an "–A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with a "–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. In the top markings of each device, the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

2. System Overview

2.1 Isolation Channel Description

The operation of an Si828x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si828x channel is shown in the figure below.

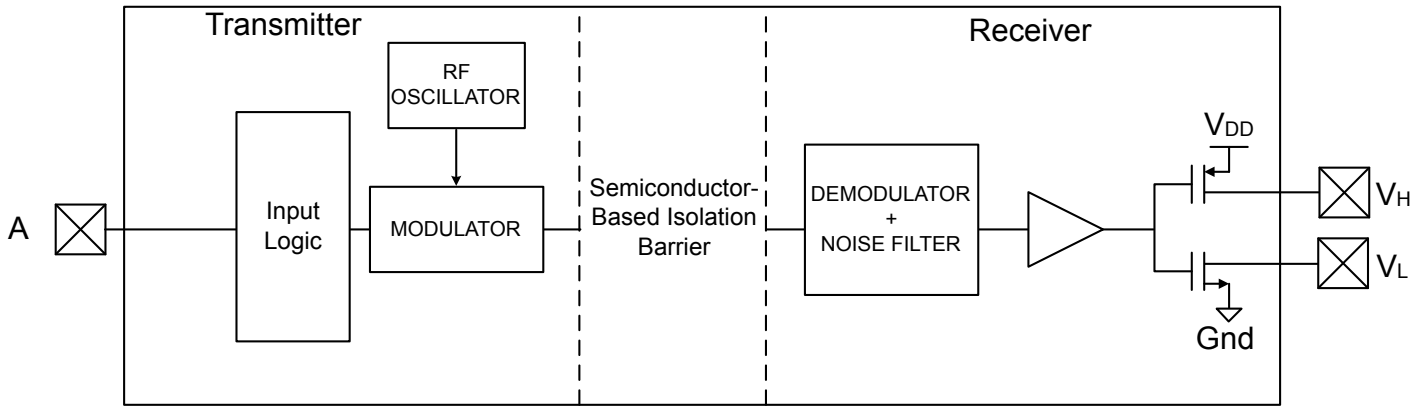


Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields.

2.2 Device Behavior

The following table shows state relationships for the Si828x inputs and outputs.

Table 2.1. Si8281/82/83/84 Truth Table

IN+	IN–	VDDA State	VDDB–VMID State	Desaturation State	VH	VL	RDY	FLTb
H	H	Powered	Powered	Undetected	Hi-Z	Pull-down	H	H
H	L	Powered	Powered	Undetected	Pull-up	Hi-Z	H	H
L	X	Powered	Powered	Undetected	Hi-Z	Pull-down	H	H
X	X	Powered	Unpowered	—	—	—	L	H
X	X	Powered	Powered	Detected	Hi-Z	Pull-down[1]	H	L

Note:

1. Driver state after soft shutdown.
2. This table is valid if RSTb is deactivated (high). For further information please refer to the **Reset (RSTb) Pin description.**

2.3 Main Features

Input

The IN+ and IN– inputs to the Si828x devices act as a complementary pair. If IN– is held low, then IN+ will act as an active-high input for driver control. Alternatively, if IN+ is held high, then IN– can be used as an active-low input for driver control. When IN– is used as the control signal, taking IN+ low will hold the output driver low.

Driver Side Output

The Si8281/82/83/84 have separate pins for gate drive high (VH) and gate drive low (VL). This makes it simple to use different gate resistors to control IGBT V_{CE} or SiC FET VDS rise and fall time.

Desaturation Detection

The Si828x provides sufficient voltage and current to drive and keep the SiC FET or IGBT in saturation during on time to minimize power dissipation and maintain high efficiency operation. However, abnormal load conditions can force the SiC FET or IGBT out of saturation and cause permanent damage to the switch.

To protect the SiC FET or IGBT during abnormal load conditions, the Si828x detects a switch desaturation condition, shuts down the driver upon detecting a fault, and provides a fault indication to the controller. These integrated features provide desaturation protection with minimum external BOM cost.

Soft Shutdown

To avoid excessive dV/dt on the SiC FET or IGBT during fault shut down, the Si828x implements a soft shut down feature to discharge the switch's gate slowly.

Fault (FLTb) Pin

FLTb is an open-drain type output. A pull-up resistor takes the pin high. When the desaturation condition is detected, the Si828x indicates the fault by bringing the FLTb pin low. FLTb stays low until the controller resets the desaturation fault by driving the RSTb pin low.

Note: This FLTb behavior is only valid when, prior to the desaturation condition being detected, there were no undervoltage lockout (UVLO) conditions.

Reset (RSTb) Pin

The RSTb pin is active low and is used to clear the desaturation condition and bring the Si828x driver back to an operational state. Even though IN+ and IN- may be toggling, the driver output will not change state until the fault condition has been reset. Both RSTb and FLTb should be high before resuming operation.

Undervoltage Lockout (UVLO)

The UVLO circuit unconditionally drives VL low when VDDB is below the lockout threshold. The Si828x is maintained in UVLO until VDDB rises above $VDDB_{UV+}$. During power down, the Si828x enters UVLO when VDDB falls below the UVLO threshold minus hysteresis (i.e., $VDDB \leq VDDB_{UV+} - VDDB_{HYS}$).

Note: UVLO voltage is evaluated between VDDB and VMID. The VSSB pin should be shorted to VMID if a negative gate bias is not utilized.

Ready (RDY) Pin

The ready pin indicates to the controller that power is available on both sides of the isolation, i.e., at VDDA and VDDB. RDY goes high when both the primary side and secondary side UVLO circuits are disengaged. If the UVLO conditions are detected on either side of the isolation barrier, the ready pin will return low. RDY is a push-pull output pin and can be floated if not used. The recommendation is to put a 10kΩ pulldown to ground on this pin to help prevent a false "Ready" indication when power supplies are below operating conditions (UVLO active).

Miller Clamp

SiC FET or IGBT power circuits are commonly connected in a half bridge configuration with the collector of the bottom IGBT tied to the emitter of the top IGBT, or, in the case of SiC FETs, to the drain and source, respectively.

As an example using IGBTs, when the upper switch turns on (while the bottom switch is in the off state), the voltage on the collector of the bottom switch flies up several hundred volts quickly (fast dV/dt). This fast dV/dt induces a current across the IGBT collector-to-gate capacitance (C_{CG}) that constitutes a positive gate voltage spike and can turn on the bottom IGBT. This behavior is called Miller parasitic turn on and can be destructive to the switch since it causes shoot-through current from the positive power rail across the two switches to ground. The Si828x Miller clamp's purpose is to clamp the gate of the switch device being driven by the Si828x to prevent switch turn on due to the collector C_{CG} coupling. SiC FET half bridge behavior is similar and the Miller clamp's purpose similar, with the effect due to the SiC FET's drain-to-gate capacitance (C_{DG}).

DC-DC Converter

The Si828x's isolated dc-dc converter uses an external transformer and low leakage/low forward voltage Schottky rectifying diodes for low cost and high operating efficiency. The PWM controller operates in closed-loop, current mode control and generates isolated output voltages. Voltage feedback is referenced between VDDB and VSSB. Although there is only one voltage feedback path, two output voltages are realized by the tight coupling of the two secondary transformer windings. Options are available for flexible input voltages and fixed or externally configured switching frequency.

3. Applications Information

The following sections detail the input and output circuits necessary for proper operation. Refer to Figure 3.1 Example Si8281/83 Application Circuit on page 8 and Figure 3.2 Example Si8282/84 Application Circuit on page 9 for recommended circuit diagrams. Diagrams display IGBTs for the application examples, but the application circuits are similar for SiC FETs.

Please note the general guidance in this table for selecting an Si828x product with integrated dc-dc converter.

	Si8281	Si8282	Si8283	Si8284
V_{IN} 5V	Yes	—	Yes	—
V_{IN} 12 V/Automotive	—	Yes	—	Yes
Switch Location	Internal	External	Internal	External
Shutdown, Soft Start, Frequency Control	No	No	Yes	Yes
Converter Switching Frequency Control	Fixed	Fixed	Variable	Variable

3.1 Recommended Application Circuits

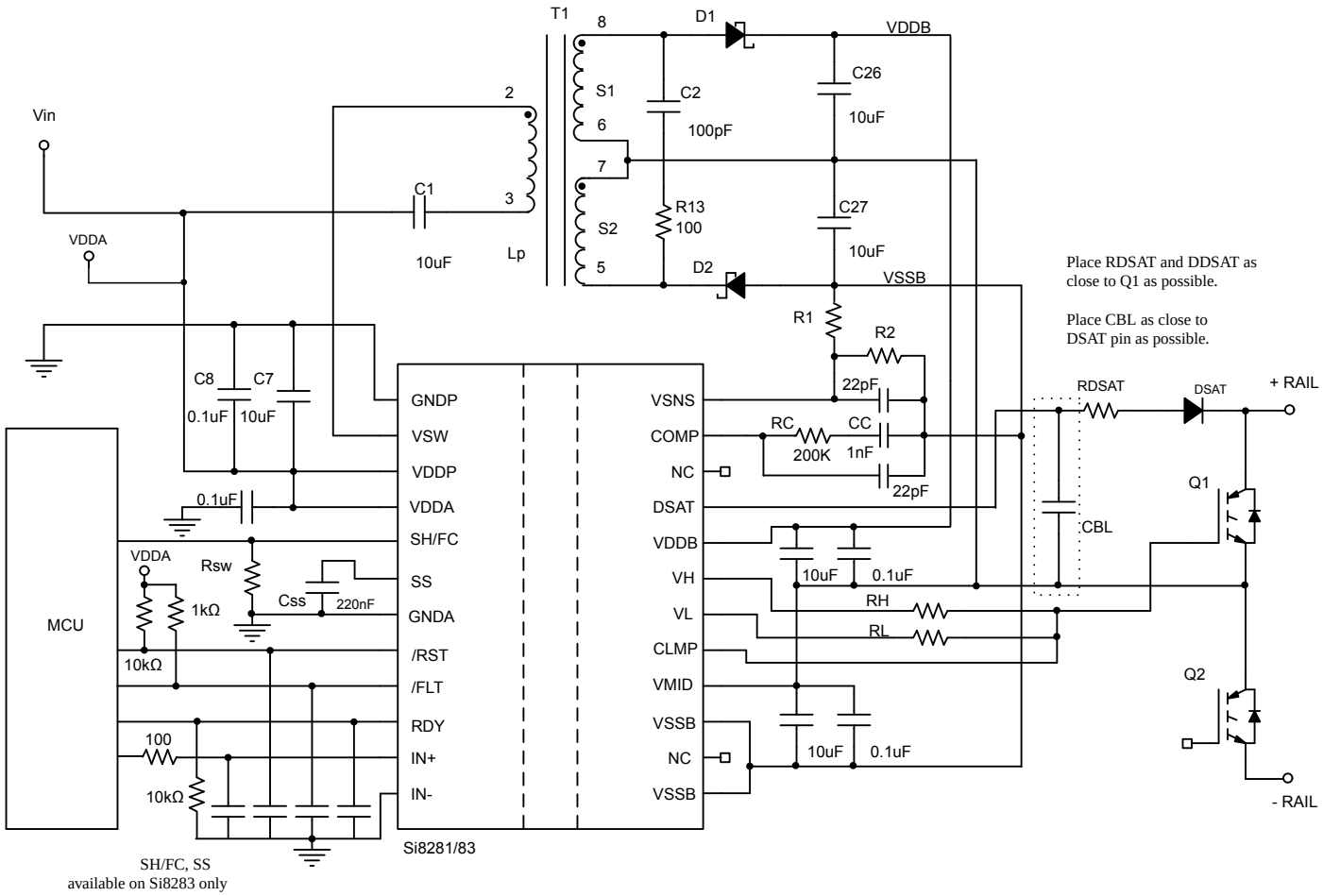


Figure 3.1. Example Si8281/83 Application Circuit

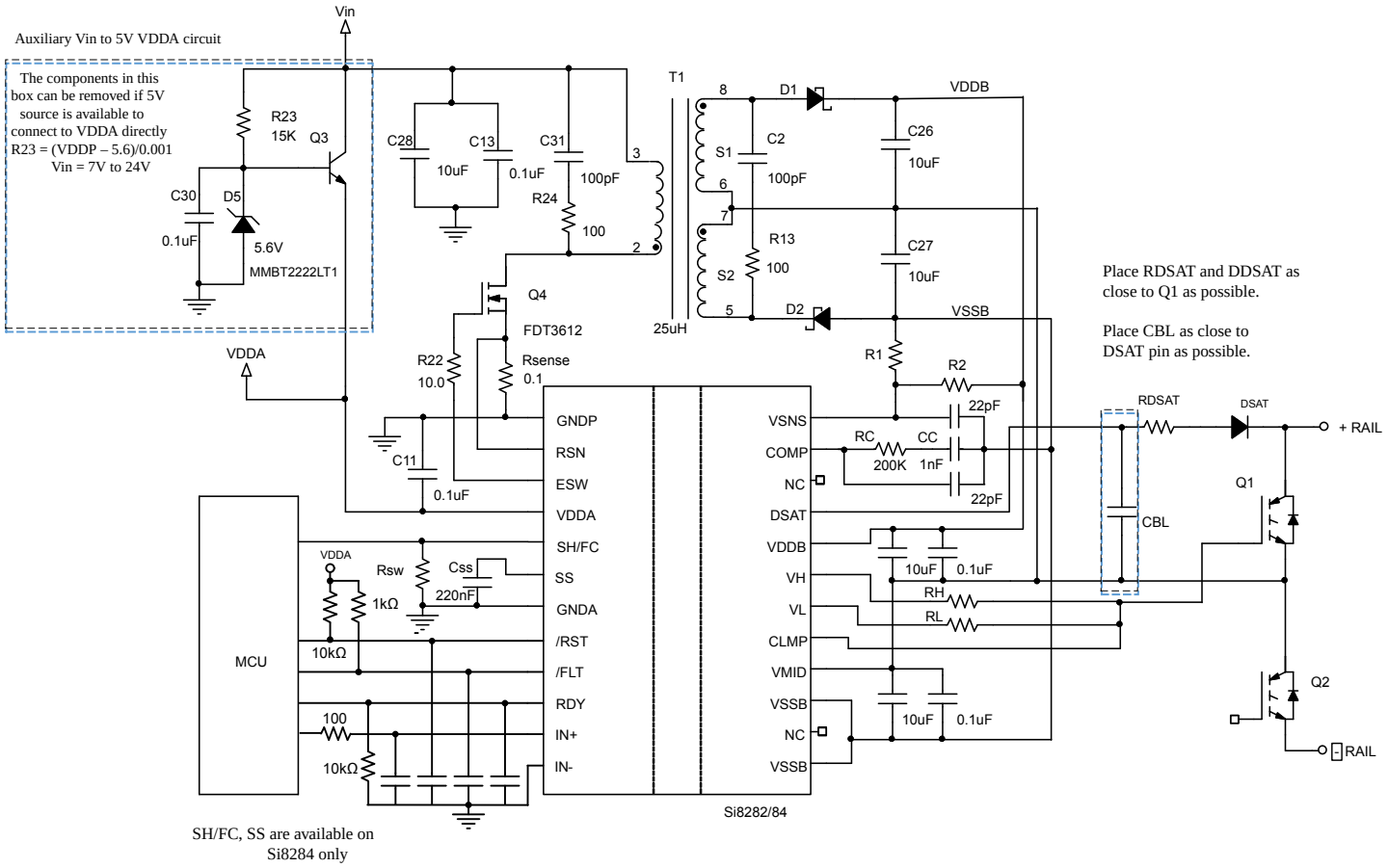


Figure 3.2. Example Si8282/84 Application Circuit

3.1.1 Power Supply Considerations

On VDDB and VSSB, each supply should have 0.1 µF and 10 µF parallel bypass capacitors. As shown in Figure 3.1 Example Si8281/83 Application Circuit on page 8 and Figure 3.2 Example Si8282/84 Application Circuit on page 9, an extra transformer winding can be implemented between VSSB and VMID to provide a negative bias to the gate drive output, if desired. Negative gate biases may help reduce switching losses. The VSSB pin should be shorted to VMID if a negative gate bias is not utilized.

3.1.2 Inputs

The Si828x has both inverting and non-inverting gate control inputs (IN– and IN+). In some topologies, one of the inputs is not used and should be connected to GNDA (IN–) or VDDA (IN+) for proper logic termination. Tying IN+ to VDDA allows active-low control of output with the IN- pin.

Inputs should be driven by CMOS level drivers. It is recommended that the MCU or input driver be located as close to the Si828x as possible to minimize PCB trace parasitics and noise coupling to the input circuit. In noisy environments, it is recommended to add a small series resistor and an approximately 56pF decoupling cap to the IN traces to attenuate glitches from electrical noise and improve input-to-output signal integrity. The resistor and capacitor values should be large enough to minimize noise but not so large that it affects PWM signals significantly.

The implementation of a differential interface circuit between the MCU and driver's input can greatly improve the noise immunity performance and prevent faulty turn on during high current switching operation.

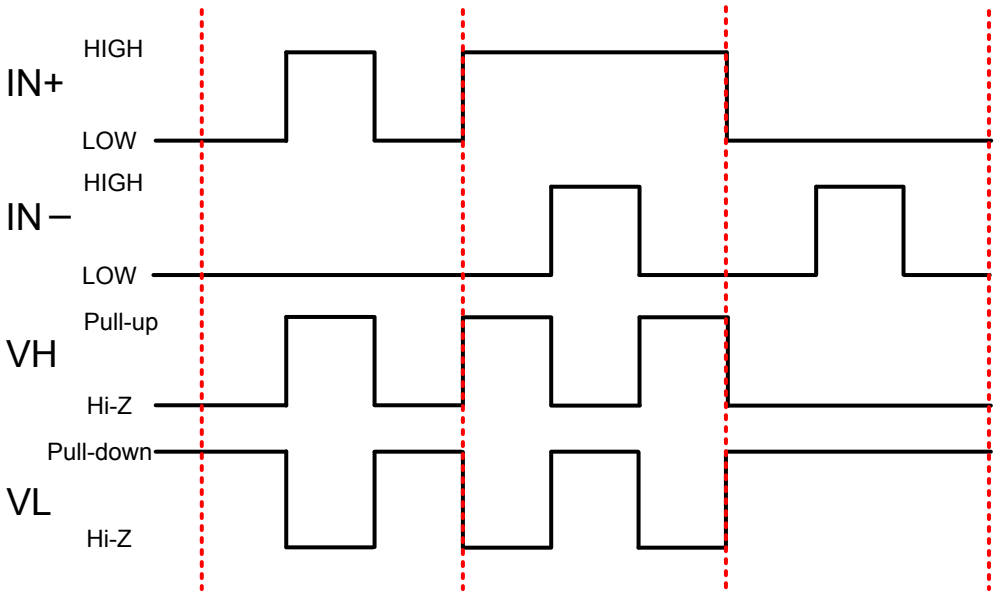


Figure 3.3. Si828x Complementary Input Diagram

3.1.3 Reset, RDY, and Fault

The Si828x family has an active high ready (RDY) push-pull output and needs a 10 kΩ pulldown resistor to prevent false ready indications during power up. The open drain fault (FLTb) output needs a pullup resistor (1 kΩ recommended) to prevent false fault indication in noisy environments; furthermore, the active low reset input (RSTb) needs a 10 kΩ pullup to help avoid false resets, particularly at startup. Fast common-mode transients in high-power circuits can inject noise and glitches into these pins due to parasitic coupling. Depending on the SiC FET or IGBT power circuit layout, additional capacitance (100 pF to 470 pF) can be included on these pins to prevent false RDY and FLTb indications as well as to prevent unintended RSTb reset of the device.

The FLTb outputs from multiple Si828x devices can be connected in an OR wiring configuration to provide a single FLTb signal to the MCU. The Si828x gate driver will shut down when a fault is detected. It then provides FLTb indication to the MCU and remains in the shutdown state until the MCU applies a reset signal to RSTb.

3.1.4 Desaturation

The Si828x provides sufficient voltage and current to drive and keep the IGBT or SiC FET in a low impedance state during the on time to minimize power dissipation and maintain high efficiency operation. However, abnormal load conditions may create excessively large load currents which may cause permanent damage. The Si828x detects this condition and safely turns off the IGBT or SiC FET.

The figure below illustrates the Si828x desaturation circuit. When the Si828x driver output is high, the internal current source is on, and this current flows from the DSAT pin to charge the CBL capacitor. The voltage on the DSAT pin is monitored by an internal comparator. Since the DSAT pin is connected to the SiC FET drain or IGBT collector through the DDSAT and a small RDSAT, its voltage is almost the same as the VCE of the IGBT or VDS of the SiC FET. If this VCE or VDS voltage does not drop below the Si828x desaturation threshold voltage within a certain time after turning on the SiC FET or IGBT (blanking period), the block will generate a fault signal. The Si828x desaturation hysteresis is fixed at 220 mV and threshold is nominally 7 V.

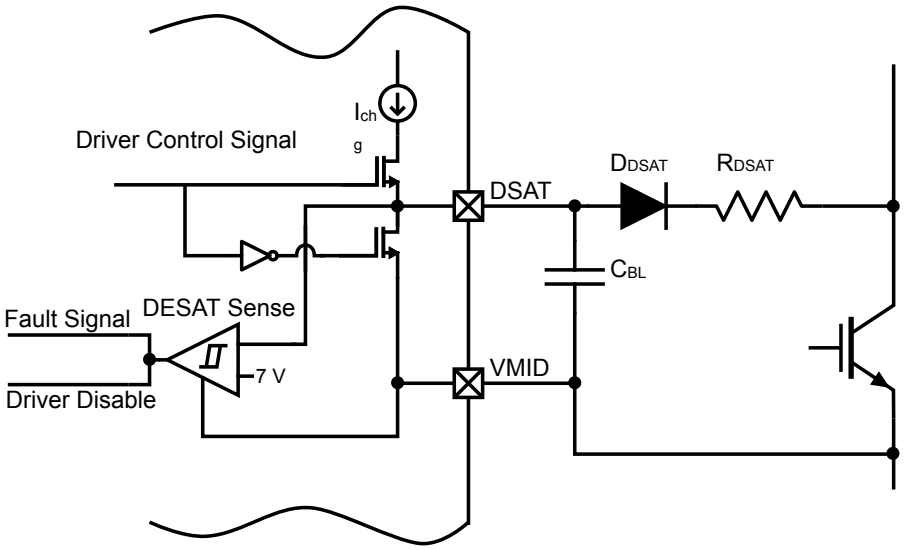


Figure 3.4. Desaturation Circuit

As an additional feature, the Si828x supports a blanking timer function to mask the turn-on transient of the external switching device and avoid unexpected fault signal generation. This function requires an external blanking capacitor, C_{BL}, between the DSAT and VMID pins. The Si828x includes current source (I_{Chg}) to charge the C_{BL}. This current source, the value of the external C_{BL}, and the programmed fault threshold, determine the blanking time ($t_{Blanking}$).

$$t_{Blanking} = C_{BL} \times \frac{V_{DESAT}}{I_{chg}}$$

An internal NMOS switch is implemented between DSAT and VMID to discharge the external blanking capacitor, C_{BL}, and reset the blanking timer. The current limiting R_{DSAT} resistor protects the DSAT pin from large current flow toward the IGBT collector during the IGBT's body diode freewheeling period (with possible large collector's negative voltage, relative to IGBT's emitter).

The desaturation sensing circuit consists of the blanking capacitor (typically 390 pF for IGBTs and 220pF-270pF for SiC FETs), 100 Ω current limiting resistor, and DSAT diode. These components provide current and voltage protection for the Si828x desaturation (DSAT) pin. It is critical to place the resistor and diode as close to the switch as possible and the capacitor as close to the DSAT pin as possible. On the layout, ensure that the loop formed between these components and the switch is minimized for optimal desaturation detection.

High-frequency oscillation can occur at the driver's output when the following conditions are met: (1) input signals set driver's output to high state, (2) the voltage across the switching device is constantly high above VDESAT, (3) the RSTb is held low. The oscillation is due to the continuous and simultaneous DESAT detection and reset cycles. The oscillation frequency in this DESAT/Reset cycle is in the MHz range and can heat up and damage the Si828x.

To avoid this condition, it is recommended to implement the following DESAT fault reset sequence:

1. Fault detected (FLTb goes low).
2. Set inputs to achieve low output state.
3. Bring RSTb low (minimum 350 ns) to clear the DESAT fault. Refer to Figure 4.7 Device Reaction to Desaturation Event on page 26.
4. Verify fault cleared (FLTb high).
5. Run diagnostic to identify system fault condition 6. Resume operation when it is safe.

3.1.4.1 Soft Shutdown

When soft shutdown is activated, the high-power driver goes inactive, and a weak pull-down via VH and external RH discharges the gate until the gate voltage level is reduced to the VSSB + 2 V level. The high-power driver is then turned on to clamp the SiC FET or IGBT gate voltage to VSSB.

After the soft shut down, the Si828x driver output voltage is clamped low to keep the SiC FET or IGBT in the off state.

3.1.5 Driver Outputs

The Si828x has VH and VL gate drive outputs. They work with external RH and RL resistors to limit output gate current. The value of these resistors can be adjusted to independently control SiC FET drain or IGBT collector voltage rise and fall time.

The CLMP output should be connected to the gate of the SiC FET or IGBT directly to provide clamping action between the gate and VSSB pin. This clamping action dissipates the switch's Miller effect current to secure the switch in the off-state. Negative VSSB provides further help to ensure the gate voltage stays below the switch's Vth during the off state.

3.1.6 Miller Clamp

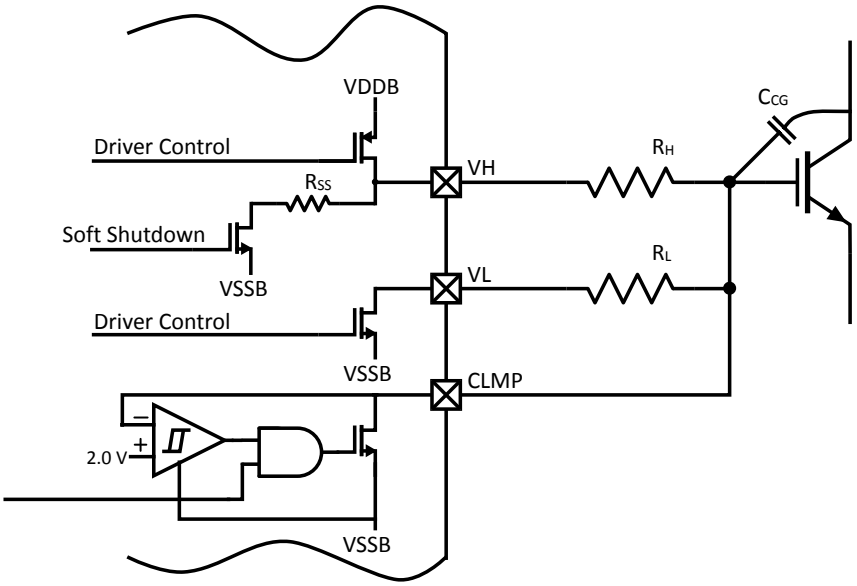


Figure 3.5. Miller Clamp Device (IGBT Example Shown)

The Miller clamp device is engaged after the main driver has been on (VL) and pulled the SiC FET or IGBT gate voltage close to VSSB, such that one can consider the switch being already off. This timing prevents the Miller clamp from interfering with the driver's operation. The engaging of the Miller Clamp is done by comparing the switch gate voltage with a 2.0 V reference (relative to VSSB) before turning on the Miller clamp NMOS.

3.1.7 Additional Adjustments for the Si828x

Additional adjustments of the desaturation detection, soft shutdown, gate current drive, and Miller clamp are possible using external components. Please refer to AN1288: Si828x External Enhancement Circuits for further information.

3.2 DC-DC Converter Application Information

The dc-dc controller modulates a pair of internal, primary-side power switches (see Figure 3.7 Si8281/83 Block Diagram: 3 to 5 V Input to Split Voltage Output on page 16) to generate an isolated voltage at external diodes D1 and D2. Divider resistors, R1 and R2, generate proper 1.05 V for the VSNS pin. Closed-loop feedback is provided by an internal compensated error amplifier, which compares the voltage at the VSNS pin to an internal voltage reference. The resulting error voltage is fed back across the isolation barrier via an internal feedback path to the controller, thus completing the control loop.

For input supply voltages higher than 5 V, an external FET Q2 is modulated by a driver pin ESW as shown in Figure 3.8 Si8282/84 Block Diagram: >5.5 V Input to Split Voltage Output on page 17. A shunt resistor-based voltage sense pin, RSN, provides current sensing capability to the controller.

The input side Vin power supply must be able to support the Si828x VDDB-VSSB static load current (approximately 9 mA), the output drive load requirement, and the dc-dc power dissipation (loss). The driver power requirement is dependent on the IGBT gate charge and the driver switching frequency. Below are the equations to calculate the Vin power requirement.

$$Pvin = \frac{\left(9 \times 10^{-3} \times (VDDB + VSSB) + Qg \times Fsw\right)}{\eta}$$

where:

Qg = IGBT total gate charge

Fsw = driver switching frequency

η = dc-dc efficiency (approximately 78%)

Additional part number features include an externally-triggered shutdown of the converter functionality using the SH pin and a programmable soft start configured by a capacitor connected to the SS pin. The resistor value on pin SH/FC and the capacitor value on pin SS are used during power-up to set the dc-dc switching frequency. Note that pin SH/FC and SS pins are available on the Si8283 and Si8284 only. The Si828x can be used with a low-voltage power rail or a high-voltage power rail. These features and configurations are explained in more detail in other sections.

Additional detail on dc-dc applications including key component selection is available in the following application notes:

- AN901: Design Guide for Isolated DC/DC Using the Si884xx, Si886xx, or Si8282/84
- AN973: Design Guide for Si8281/83 Isolated DC-DC with Internal Switch

3.2.1 External Transformer Driver

The dc-dc controller has internal switches (VSW) for driving the transformer with up to a 5.5 V, 2 W power supply. For higher voltages on the primary side, higher power, or higher efficiency, a driver output (ESW) is provided on the Si8282 and Si8284 that can switch an external NMOS power transistor for driving the transformer. When this configuration is used, a shunt resistor based voltage sense pin (RSN) provides current sensing to the controller.

3.2.2 Output Voltage Control

The isolated output voltage, VOUT (VDDB–VSSB), is sensed by a resistor divider that provides feedback to the controller through the VSNS pin. The voltage error is encoded and transmitted back to the primary side controller across the isolation barrier, which in turn changes the duty cycle of the transformer driver. The equation for VOUT is as follows:

$$VOUT = VSNS \times \left(1 + \frac{R1}{R2}\right)$$

The VDDB-VSSB voltage split depends on the ratio of the two secondary windings and can be calculated as follows:

$$VDDB - VMID = VOUT \times \left(\frac{S1}{S1 \times S2}\right)$$

$$VSSB - VMID = VOUT \times \left(\frac{S2}{S1 + S2}\right)$$

3.2.3 Compensation

The dc-dc converter operates in current mode control. The loop is compensated by connecting an external resistor in series with a capacitor from the COMP pin to VSSB. The compensation network, RCOMP, and CCOMP are set to 200 kΩ and 1 nF for most Si828x applications.

3.2.4 Thermal Protection

A thermal shutdown circuit is implemented to protect the system from over-temperature events.

3.2.5 Cycle Skipping (Si8282 and Si8284 Only)

Cycle skipping is included to reduce switching power losses at light loads. This feature is transparent to the user and is activated automatically at light loads.

3.2.6 Shutdown (Si8283 and Si8284 Only)

This feature allows shut down of the dc-dc converter by asserting SH/FC high. This pin normally has a resistor to ground. The resistor value and the value of the capacitor on the SS pin determine the dc-dc switching frequency. You may connect an MCU GPIO pin to the SH/FC pin to control the shutdown function. This pin should be in a high-impedance state during startup to avoid interfering with the internal frequency calculation circuit. During normal operation, this pin should be held in a high-impedance state, and only taken high to assert dc-dc shutdown.

3.2.7 DC-DC Startup and Soft Start

The dc-dc controller has an internal timer that controls the power conversion start-up to limit inrush current. The soft start period (t_{SS}) is the duration of time that the Si828x dc-dc converter will try to ramp up the output voltage while operating at a reduced current limit which is achieved by reducing the value of ILIM (Si8281 and Si8283) or V_{th_RSN} (Si8282 and Si8284). The soft start period t_{SS} is followed by 40 ms where the converter is fully on.

There is also a programmable Soft Start option (for the Si8283 and Si8284 only) where users can program t_{SS} with an external capacitor connected to the SS pin. For the Si8281 and Si8282, t_{SS} = 40 ms. The equations for setting the soft start period for the Si8283 and Si8284 are as follows:

$$t_{SS} = 200000 \times C_{SS}$$

or

$$C_{SS} = \frac{t_{SS}}{200000}$$

3.2.7.1 Startup Fault Behavior

If the output voltage fails to reach $VDDB_{UV+}$ within the 40 ms fully-on period following soft start, the Si828x will terminate the dc-dc startup cycle and wait for t_{RDFE} before initiating a new startup cycle. The RDY pin will remain low during startup if the output voltage fails to exceed $VDDB_{UV+}$.

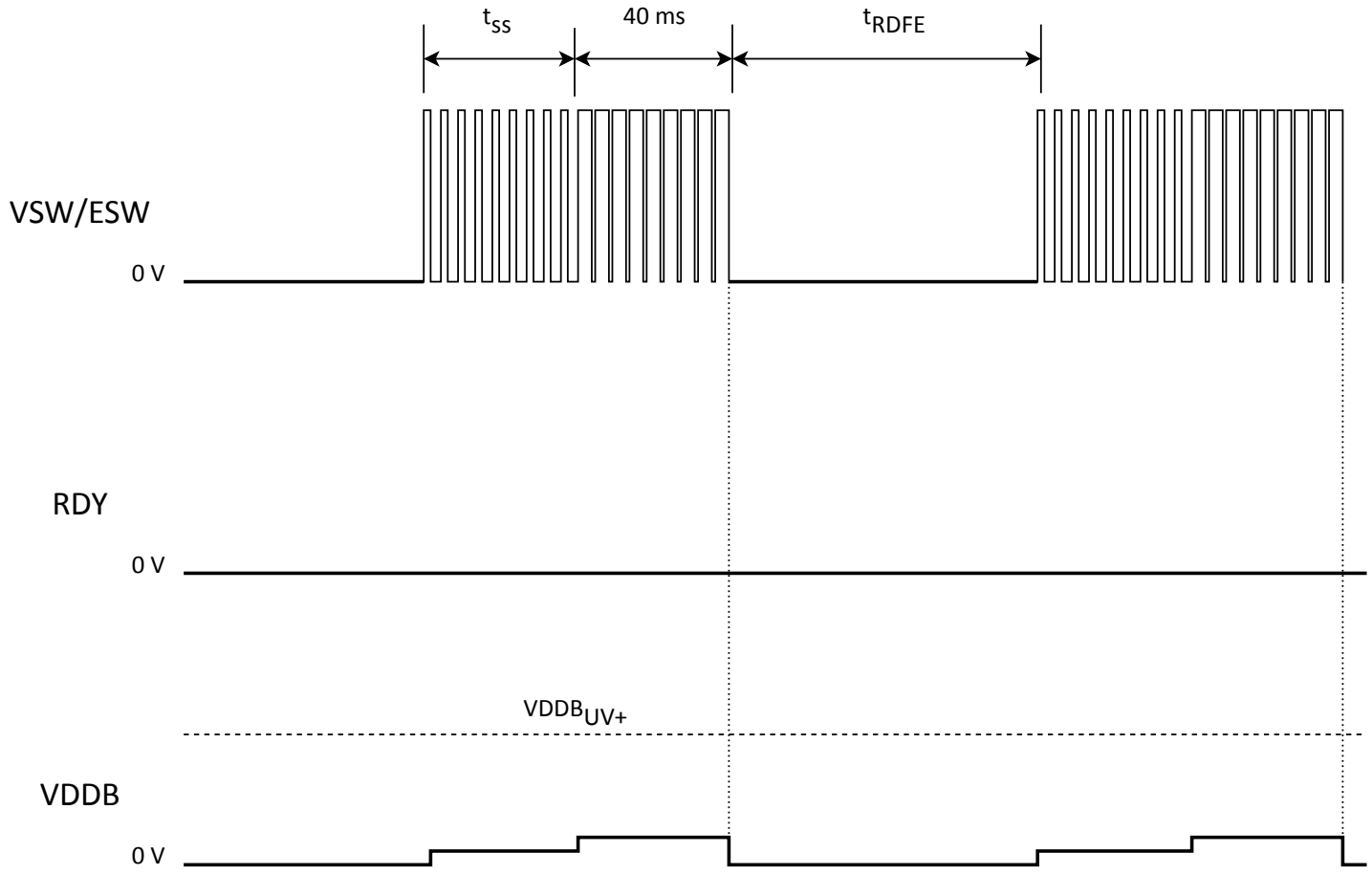


Figure 3.6. DC-DC Fault Detection, Shutdown, and Retry Behavior

3.2.8 Programmable Frequency (Si8283 and Si8284 Only)

The frequency of the PWM modulator is set to a default of 250 kHz for Si828x. Users can program their desired frequency within a given band of 200 kHz to 800 kHz by controlling the time constant of an external RC connected to the SH_FC and SS pins.

The equations for setting f_{SW} or R_{SW} are as follows:

$$f_{SW} = \frac{1025.5}{(R_{SW} \times C_{SS})}$$

or

$$R_{SW} = \frac{1025.5}{(f_{SW} \times C_{SS})}$$

The following are the recommended steps for calculating C_{SS} and R_{SW}:

1. Select the maximum soft start duration (typically 40 ms).
2. Calculate Css using Equation A.
3. Select the dc-dc switching frequency.
4. Calculate R_{SW} using the above equation.

3.2.9 Si8281/83 Converter (Internal Switch) Configuration

The low supply voltage configuration is used when 3.0 V to 5.5 V supply rails are available. All product options of the Si8281 and Si8283 are intended for this configuration. The output voltage is rated for +15 V / –9 V.

An advantage of Si828x devices over other converters that use this same topology is that the output voltage is sensed on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the dc-dc to operate with superior line and load regulation while reducing external components and increasing lifetime reliability.

In a typical isolated gate driver application, the dc-dc powers the Si8281 and Si8283 VDDB and VSSB as shown in the figure below. The Si8281 and Si8283 dc-dc circuit in the figure below can deliver up to 2 W of output power for V_{in} = 5 V and 1 W for V_{in} = 3.3 V. The dc-dc requires an input capacitor, C_2, blocking capacitor, C_1, transformer, T_1, rectifying diodes, D_1 and D_2, and output capacitors, C_{26}, and C_{27}. Resistors R_1 and R_2 divide the output voltage to match the internal reference of the error amplifier. The ratio of the two secondary windings, S1 and S2, splits the output voltage into two portions. The positive VDDB and the negative VSSB with common reference to VMID (IGBT emitter or SiC source).

$$VDDB = VOUT \times \left(\frac{S1}{S1 + S2}\right)$$

$$VSSB = -VOUT \times \left(\frac{S2}{S1 + S2}\right)$$

Type 1 loop compensation made by RCOMP and CCOMP are required at the COMP pin. The combination of RCOMP = 200 kΩ and CCOMP = 1 nF satisfies most Si8281 and Si8283 dc-dc applications. Though it is not necessary for normal operation, we recommend that an RC snubber (refer to AN973: Design Guide for Si8281/83Isolated DC-DC with Internal Switch for details) be placed in parallel with the secondary winding to minimize radiated emissions.

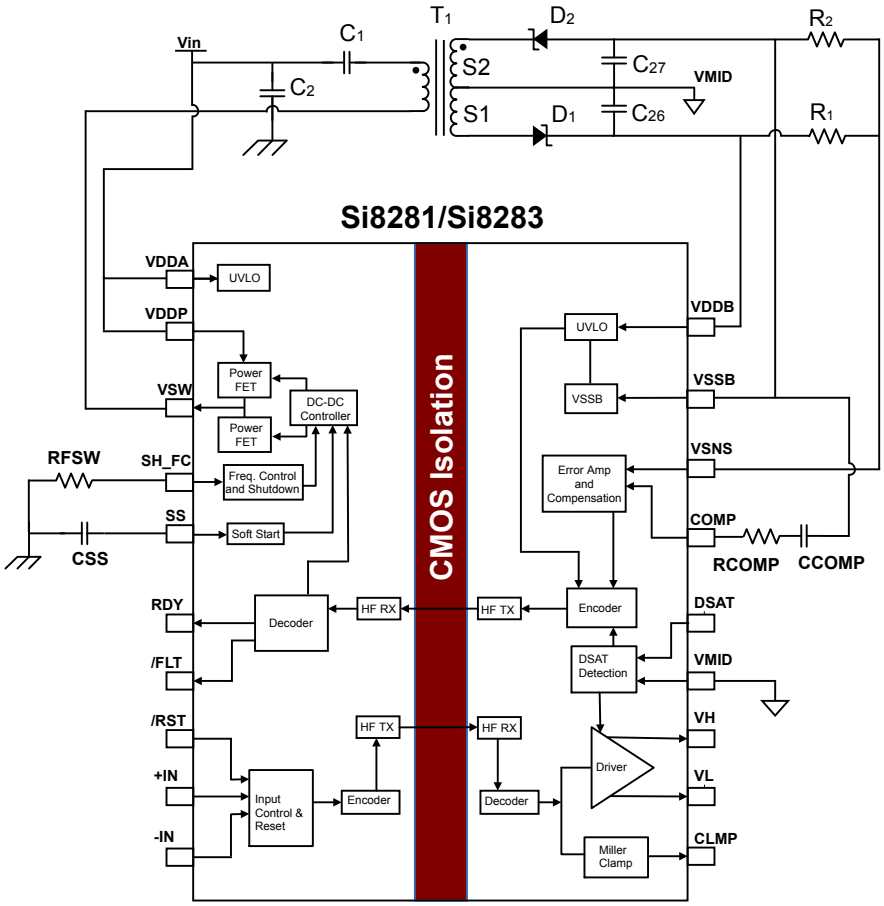


Figure 3.7. Si8281/83 Block Diagram: 3 to 5 V Input to Split Voltage Output

3.2.10 Si8282/84 Converter (External Switch) Configuration

The high supply voltage configuration is used when a higher voltage power supply rail (up to 24 V) is available. All product options of the Si8282 and Si8284 are intended for this configuration. The dc-dc converter uses the isolated flyback topology. With this topology, the switch and sense resistor are external, allowing higher switching voltages.

An advantage of Si828x devices over other converters that use this same topology is that the output voltage is sensed on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the dc-dc to operate with superior line and load regulation while reducing external components and increasing lifetime reliability.

The figure below shows the block diagram of an Si828x with external components. The Si8284 product option has externally controlled switching frequency and soft start. The dc-dc requires input capacitor C_{28}, transformer T_1, switch Q_4, sense resistor R_{sense}, rectifying diodes D_1 and D_2, and output capacitors C_{26} and C_{27}. To supply VDDA, Q_3 transistor is biased by R_{23}, 5.6 V Zener diode D_5 and filtered by C_{30} and C_{11}. External frequency and soft start behavior is set by CSS and RFSW. Resistors R_1 and R_2 divide the output voltage to match the internal reference of the error amplifier. The ratio of the two secondary windings splits the output voltage into two portions. The positive VDDB and the negative VSSB with common reference to VMID (IGBT Emitter).

$$VDDB = VOUT \times \left(\frac{S1}{S1 + S2}\right)$$

$$VSSB = -VOUT \times \left(\frac{S2}{S1 + S2}\right)$$

Type 1 loop compensation made by RCOMP and CCOMP are required at the COMP pin. The combination of RCOMP = 49.9 kΩ and CCOMP = 1.5 nF satisfies most Si8282 and Si8284 dc-dc applications. Though it is not necessary for normal operation, we recommend to use RC snubbers (refer to AN901: Design Guide for Isolated DC/DC Using the Si884xx, Si886xx, or Si8282/84 for details) on both primary and secondary windings to minimize high-frequency emissions.

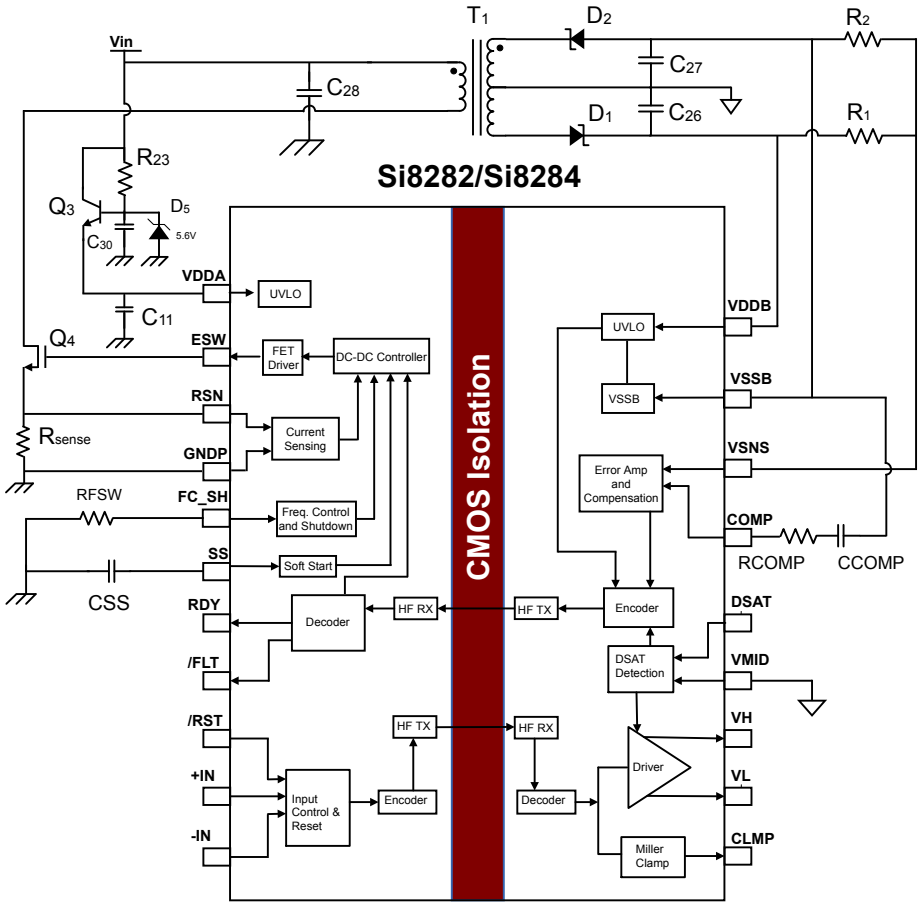


Figure 3.8. Si8282/84 Block Diagram: >5.5 V Input to Split Voltage Output

3.2.11 Transformer Design

The internal switch dc-dc (Si8281, Si8283) and external switch dc-dc (Si8282, Si8284) operate in different topologies and, thus, require different transformer designs. The table below provides a list of transformers and their parametric characteristics that have been validated to work with Si828x products. It is recommended that users order the transformers from the vendors per the part numbers given below.

To manufacture transformers from your preferred suppliers that may not be listed below, please specify to supplier the parametric characteristics as specified in the table below for a given input voltage and isolation rating.

Table 3.1. Si828x Recommended Transformers

Tranformer Supplier	Ordering Part #	Input Voltage	Output Voltage	Turns Ratio P:S	Leakage Inductance	Primary Inductance	Primary Resistance	Isolation Rating
UMEC[2] (http://www.umec-usa.com)	UTB02241s	4.5 – 5.5V	-10.0 – 14V	1 : 7 : 5	100 nH max	2.5 µH ±5%	0.05 Ω max	5 kVrms
UMEC[2] (http://www.umec-usa.com)	UTB02253s	7 – 24V	-9.0 – 15V	1 : 2 : 1.21	200 nH max	25 µH ±5%	0.225 Ω max	5 kVrms
Coilcraft[1, 2] (http://www.coilcraft.com)	TA7788-AL	7 – 24V	-9.0 – 15V	1 : 1.25 : 0.75	554 nH max	25 µH ±5%	0.49 Ω max	5 kVrms
Mentech [1, 3] (http://www.mnc-tek.com)	TTER09-1174SG	8 – 24V	-4.0 – 15V	16 : 20 : 5	5 µH max	20 µH ±5%	0.7 Ω max	5 kVrms
Mentech [1, 3] (http://www.mnc-tek.com)	TTER09-1175SG	7 – 20V	-4.0 – 15V	17 : 11 : 3	2.5 µH max	15 µH ±5%	0.6 Ω max	5 kVrms
Mentech [1, 3] (http://www.mnc-tek.com)	TTER09-1204SG	8 – 24V	6.5V AUX; -4.0 – 15V; -4.0 – 15V	17 : 5 : 11 : 3 : 11 : 3	2 µH max	20 µH ±5%	0.15 Ω max	5 kVrms

Note:

1. AEC-Q200 qualified.
2. For reference design details, see AN973: Design Guide for Si8281/83 Isolated DC-DC with Internal Switch
3. .For reference design details, see AN901: Design Guide for Isolated DC/DCUsing the Si884xx, Si886xx, or Si8282/84

3.3 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the supply lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si828x as close as possible to the device it is driving. In addition, the supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and power planes for power devices and small signal components provides the best overall noise performance.

4. Electrical Specifications

Table 4.1. Electrical Specifications

V_{IN} = 24 V; V_{DDA} = 4.3 V (See Figure 3) for all Si8282/84; V_{DDA} = V_{DDP} = 3.0 to 5.0 V (See Figure 2) for all Si8281/83; Driver supply voltage = VDDB-VSSB; T_A = –40 to +125 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DC Parameters						
Input Supply Voltage	VDDA		3.0	—	5.5	V
Power Input Voltage	VDDP		3.0	—	5.5	V
Driver Supply Voltage	(VDDB – VSSB)	Si828xBx	10.0	—	30	V
		Si828xCx	13.2	—	30	V
		Si828xDx	14.0	—	30	V
		Si828xEx	16.0	—	30	V
	(VMID – VSSB)		0	—	15	V
Input Supply Quiescent Current	IDDA(Q)		—	6.8	7.5	mA
Input Supply Active Current	IDDA	f = 10 kHz	—	10.5	—	mA
Output Supply Quiescent Current	IDDB(Q)		—	8.7	10.8	mA
DC-DC Converter						
Switching Frequency Si8281, Si8282	FSW		—	250	—	kHz
Switching Frequency Si8283, Si8284	FSW	RFSW = 23.3 kΩ FSW = 1025.5/(RFSW x CSS) CSS = 220 nF (1% tolerance on BOM)	180	200	220	kHz
		RFSW = 9.3 kΩ FSW = 1025.5/(RFSW x CSS) CSS = 220 nF (1% tolerance on BOM)	450	500	550	kHz
		RFSW = 5.18 kΩ CSS = 220 nF	810	900	990	kHz
VSNS Voltage	VSNS	ILOAD = 0 A	1.002	1.05	1.097	V
VSNS Current Offset	I_{offset}		–500	—	500	nA
Output Voltage Accuracy		ILOAD = 0 mA	–5	—	+5	%
Line Regulation	ΔVOUT(line)/ ΔVDDP	POUT = 1 W VDDP varies from 4.5 to 5.5 V (Si8281/83) VDDP varies from 8 to 24 V (Si8282/84)	—	1	—	mV/V
Load Regulation	ΔVOUT(load)/ VOUT	POUT = 0.25 to 2 W VDDP = 12 V	—	0.1	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Voltage Ripple Si8281, Si8283 Si8282, Si8284		ILOAD = 100 mA	—	100	—	mV p-p
Turn-on overshoot	ΔVOUT(start)	CIN = COUT = 0.1 µF in parallel with 10 µF ILOAD = 0 A	—	2	—	%
Continuous Output Current Si8281, Si8283 5.0 V to +15 V / –9 V split rails 3.3 V to +15 V / –9 V split rails Si8282, Si8284 24 V to +15 V / –9 V split rails	ILOAD(max)	—	—	 84 84 84	—	mA
Cycle-by-Cycle Average Current Limit Si8281, Si8283	ILIM	Output short circuited	—	3	—	A
RSN Overload Threshold Si8282, Si8284	V_{th_RSN}	VDDP = 12 V Rsns = 0.1 Ω	—	115	—	mV
No-Load Supply Current IDDP Si8281, Si8283	IDDPQ_DCDC	VDDP = VDDA = 5 V	—	30	—	mA
No-Load Supply Current IDDA Si8281, Si8283	IDDAQ_DCDC	VDDP = VDDA = 5 V	—	5.7	—	mA
No-Load Supply Current IDDP Si8282, Si8284	IDDPQ_DCDC	VIN = 24 V	—	0.8	—	mA
No-Load Supply Current IDDA Si8282, Si8284	IDDAQ_DCDC	VIN = 24 V	—	5.8	—	mA
Efficiency Si8281, Si8283 Si8282, Si8284	η		—	 78 83	—	%
Soft Start Time, Full Load Si8281, Si8282 Si8283, Si8284	t_{SS}		—	 25 50	—	ms
Restart Delay from Fault Event	t_{RDFE}		—	83	—	ms
Drive Parameters						
High Drive Transistor RDS(ON)	R_{OH}		—	2.48	—	Ω
Low Drive Transistor RDS(ON)	R_{OL}		—	0.86	—	Ω
Internal Soft Shutdown Impedance	R_{SS}		—	60	—	Ω

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
High Drive Peak Output Current[1, 2]	I_{OH}	VDDB = 15 V VSSB = -4 V CL = 220 nF Pulse = 3 µs	2.0	2.7	—	A
Low Drive Peak Output Current[1, 2]	I_{OL}		4.1	5.5	—	A
UVLO Parameters						
UVLO Threshold +	$VDDA_{UV+}$		2.4	2.7	3.0	
UVLO Threshold –	$VDDA_{UV–}$		2.3	2.6	2.9	
UVLO Lockout Hysteresis– (Input Side)	$VDDA_{HYS}$		—	100	—	mV
UVLO Threshold + (Driver Side) 9 V Threshold (Si828xB) 12 V Threshold (Si828xC) 13 V Threshold (Si828xD) 15 V Threshold (Si828xE)	$VDDB_{UV+}$	$VDDB_{UV+}$ is VDDB referenced to VMID	 8.0 10.8 11.6 13.6	 9.0 12.0 12.8 14.8	 10.0 13.2 14.0 16.0	 V V
UVLO Threshold – (Driver Side) 9 V Threshold (Si828xB) 12 V Threshold (Si828xC) 13 V Threshold (Si828xD) 15 V Threshold (Si828xE)	$VDDB_{UV–}$	$VDDB_{UV-}$ is VDDB referenced to VMID	 7.0 9.8 10.8 12.8	 8.0 11.0 12.0 14.0	 9.0 12.2 13.2 15.2	 V V
UVLO Lockout Hysteresis (Driver Side) 9 V/12 V Thresholds (Si828xB/Si828xC) 13 V/15 V Thresholds (Si828xD/ Si828xE)	$VDDB_{HYS}$		 — —	 1 0.75	 — —	 V
UVLO+ to RDY High Delay	$t_{UVLO+ \text{ to RDY}}$		—	—	100	µs
UVLO+ to V_X Active Delay	t_{UVLO+} to Vx_Active		—	—	100	µs
UVLO– to RDY Low Delay	$t_{UVLO– \text{ to RDY}}$		—	—	0.79	µs
UVLO- to Output OFF Delay	$t_{UVLO– \text{ to Output_OFF}}$		—	—	0.79	µs
Desaturation Detector Parameters						
DESAT Threshold	VDESAT	VDDB – VSSB > VDDBUV+	6.25	6.9	7.4	V
C_{BI} charging current	I_{Chg}		—	1	—	mA
DESAT Sense to 90% VH Delay	$t_{DESAT(90\%)}$	RH = RL = 10 Ω CL = 10 nF	—	270	350	ns
DESAT Sense to 10% VH Delay	$t_{DESAT(10\%)}$	RH = RL = 10 Ω CL = 10 nF	—	1.8	2.3	µs
DESAT Sense to FLTb Low Delay	$t_{DESAT \text{ to FLTb}}$		—	220	300	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Reset to FLTb High Delay	$t_{RST\ to\ FLTb}$		—	270	350	ns
Reset Pulse Width	t_{RSTb}		350	—	—	ns
Miller Clamp Parameters						
Clamp Pin Threshold Voltage	V_t Clamp		—	2.0	—	V
Miller Clamp Transistor RDS (ON)	R_{MC}		—	1.07	—	Ω
Clamp Low Level Sinking Current[1, 2]	I_{CL}	VCLMP = VSSB + 6.0	3.0	3.4	—	A
Digital Parameters						
Logic High Input Threshold	VIH		2.0	—	—	V
Logic Low Input Threshold	VIL		—	—	0.8	V
Input Hysteresis	VIHYST		—	440	—	mV
High Level Output Voltage (RDY pin only)	VOH	IO = –4 mA	VDDA – 0.4	—	—	V
Low Level Output Voltage (RDY pin only)	VOL	IO = 4 mA	—	—	0.4	V
Open-Drain Low Level Output Voltage (FLTb pin only)		VDDA = 5 V, 5 kΩ pull-up resistor	—	—	200	mV
AC Switching Parameters						
Propagation Delay (Low-to-High)	t_{PLH}	CL = 200 pF	30	40	50	ns
Propagation Delay (High-to-Low)	t_{PHL}	CL = 200 pF	30	40	50	ns
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$ for a single device	—	1	5	ns
Propagation Delay Difference[2]	PDD	$t_{PHLMAX} - t_{PLHMIN}$	–1	—	25	ns
Rise Time[2] (10% to 90%)	t_R	CL = 200 pF	—	5.5	15	ns
Fall Time[2] (90% to 10%)	t_F	CL = 200 pF	—	8.5	20	ns
Common Mode Transient Immunity		Output = low or high (VCM = 1500 V)	125	—	—	kV/µs

1. When performing this test, it is recommended that the DUT be soldered to avoid socket and trace inductances, which may cause overstress conditions.
2. Guaranteed by characterization.

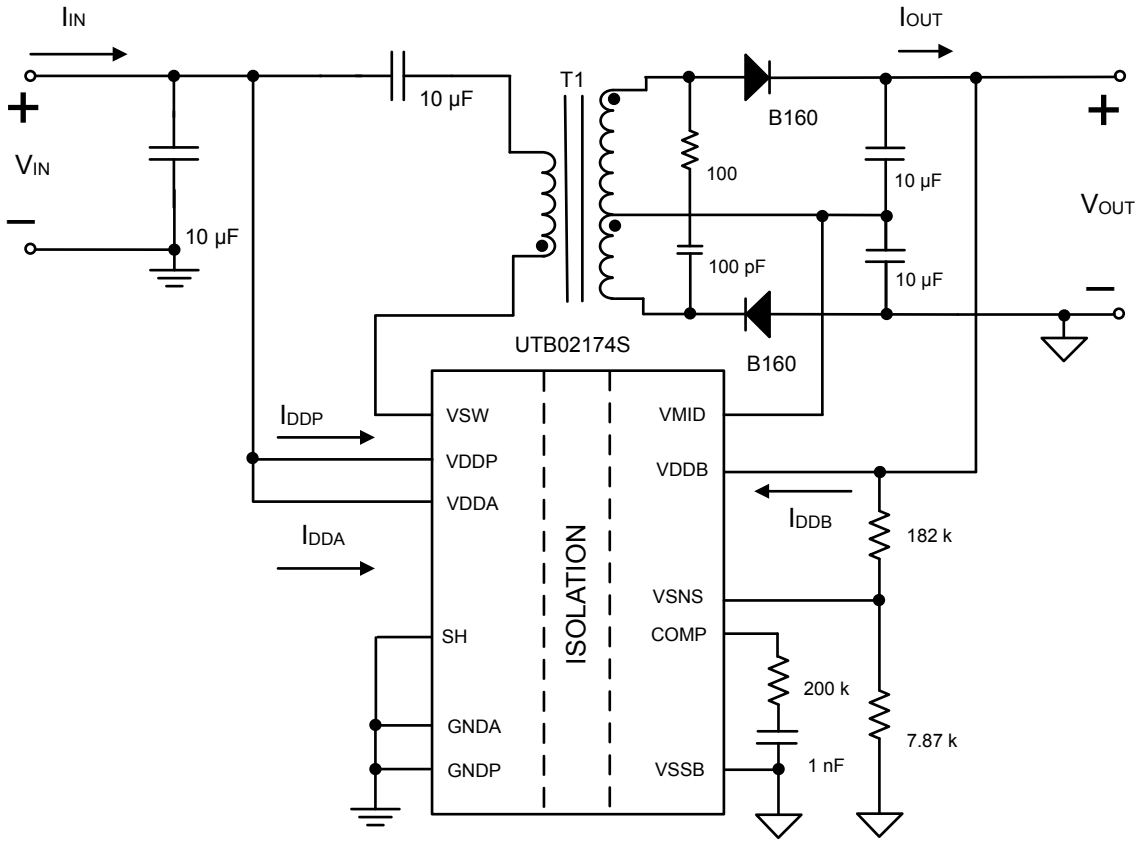


Figure 4.1. Si8281, Si8283 Measurement Circuit for Converter Efficiency and Regulation

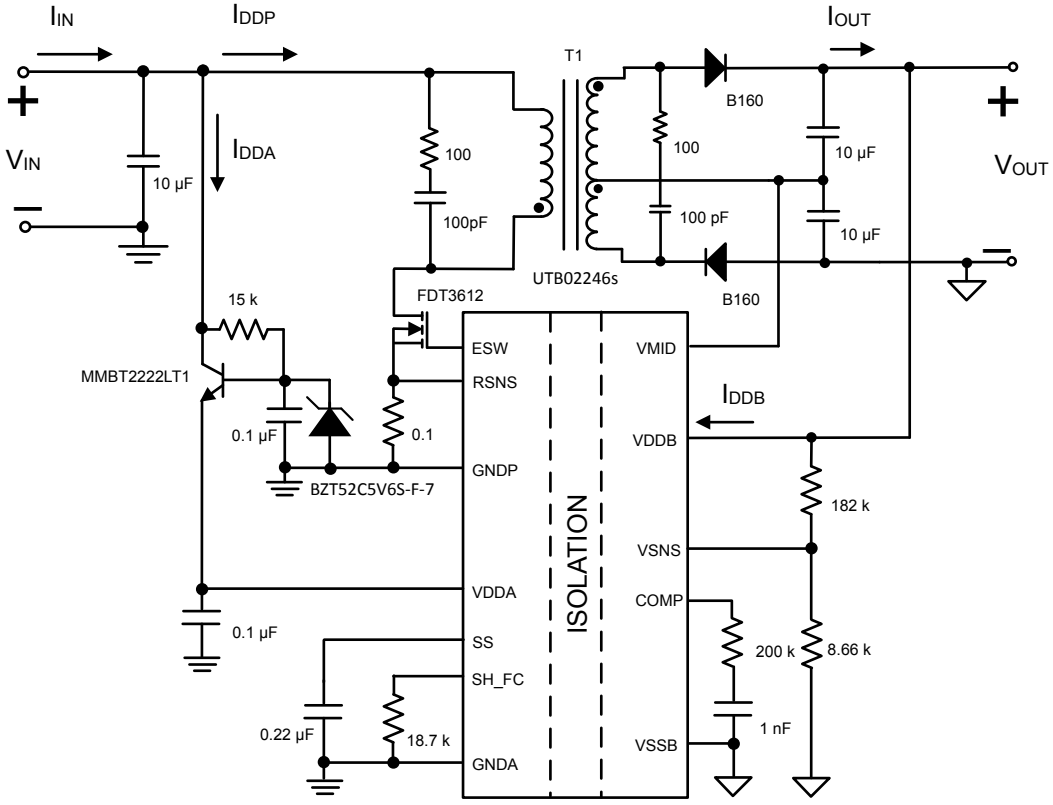


Figure 4.2. Si8282, Si8284 Measurement Circuit for Converter Efficiency and Regulation

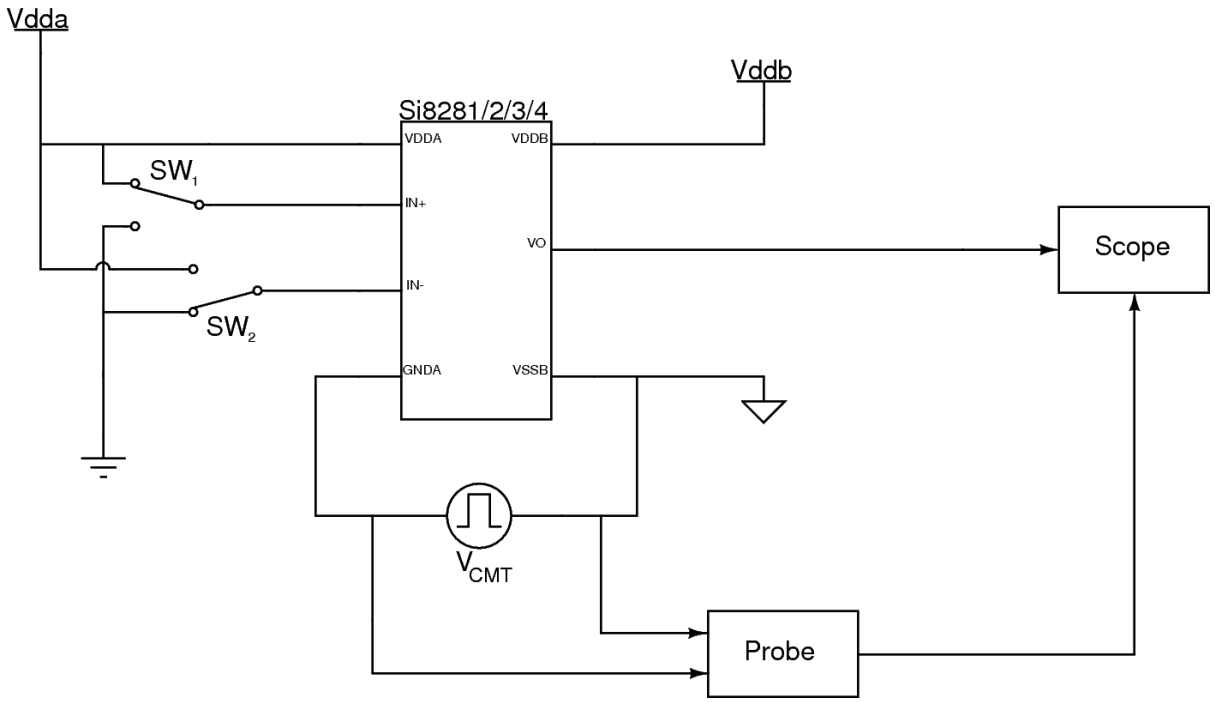


Figure 4.3. Common-Mode Transient Immunity Characterization Circuit

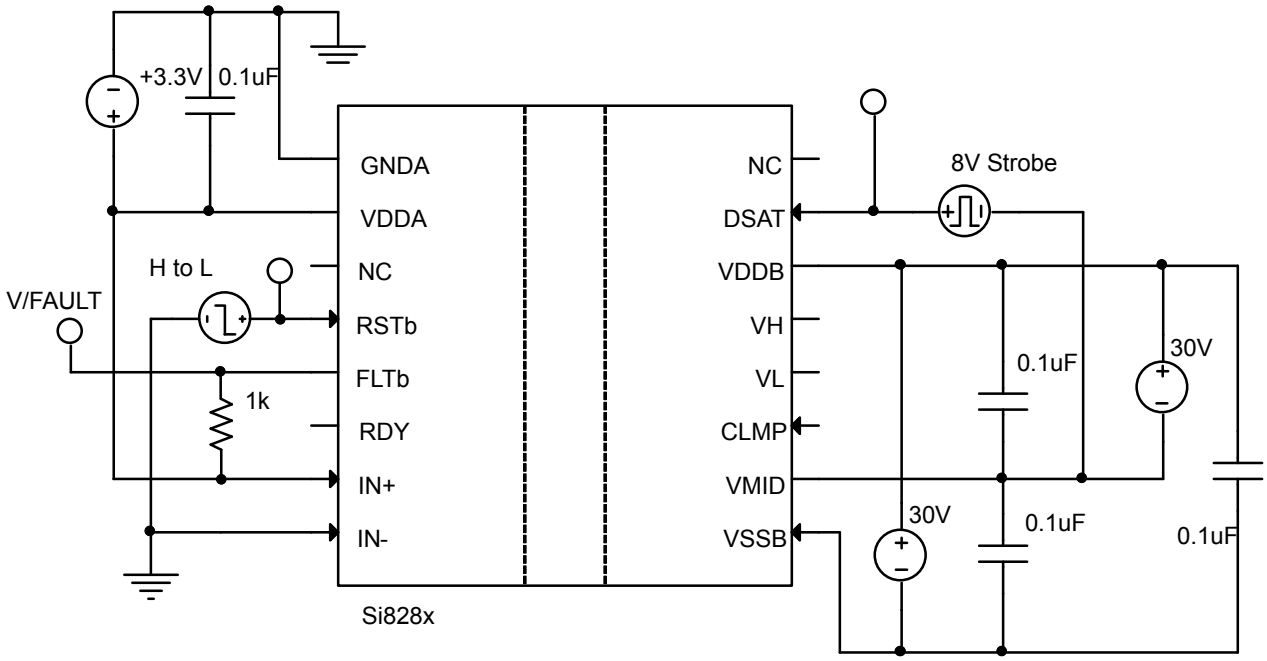


Figure 4.4. Si828x RSTb FLTb CLEAR Test Circuit

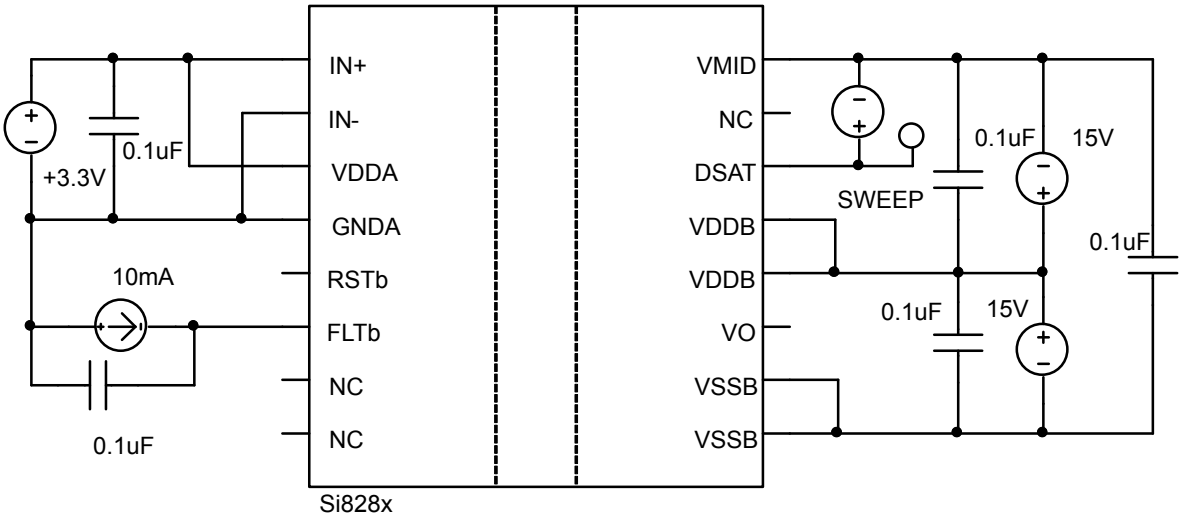


Figure 4.5. Si828x DSAT Threshold Test Circuit

Table 4.2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	+150	°C
Operating Temperature	T_A	–40	+125	°C
Junction Temperature	T_J	—	+140	°C
Peak Output Current (t_{PW} = 10 µs)	I_{OPK}	—	4.0	A
Input Side Supply Voltage	VDDA - GNDA	-0.5	6	V
Output Side Supply Voltage	VDDB - VSSB	–0.5	36	V
Output Voltage	VH/VL	–0.5	36	V
Input Power Dissipation	P_I	—	100	mW
Output Power Dissipation	P_O	—	800	mW
Total Power Dissipation (All Packages Limited by Thermal Derating Curve)	P_T	—	900	mW
Lead Solder Temperature (10 s)		—	260	°C

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.1 Timing Diagrams

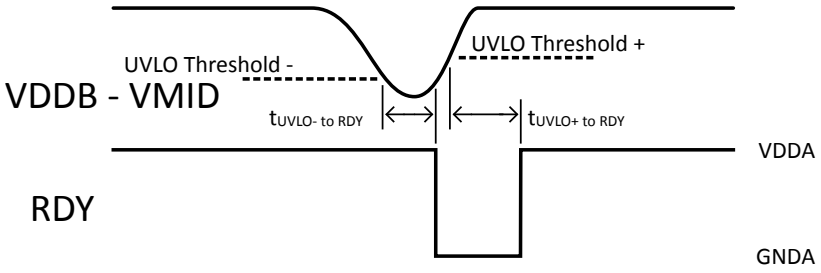


Figure 4.6. UVLO Condition to RDY Output

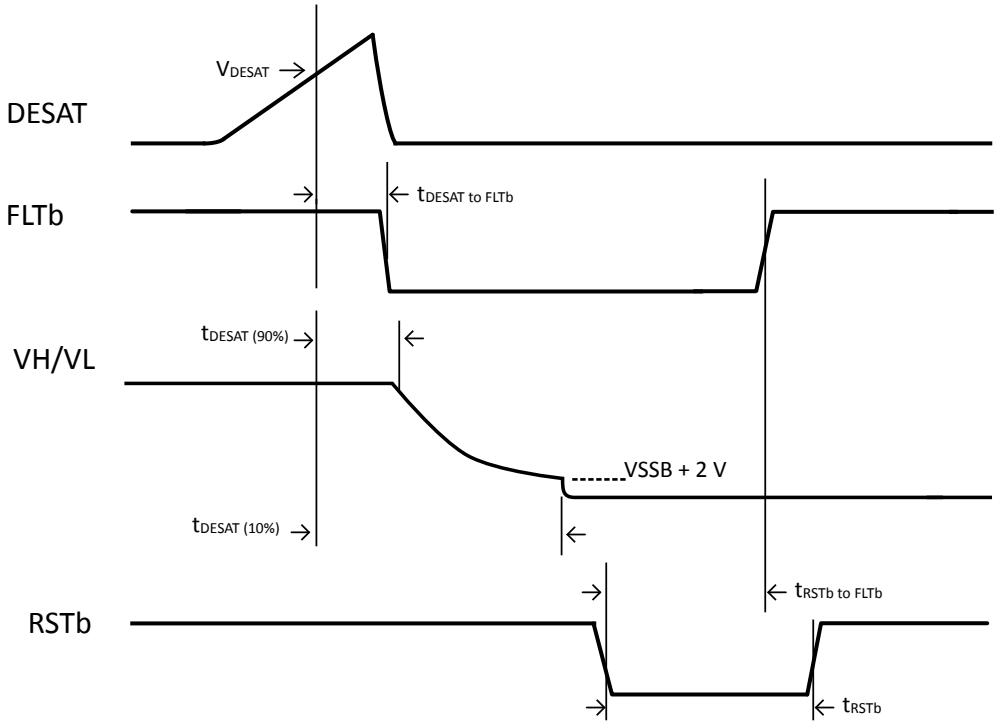
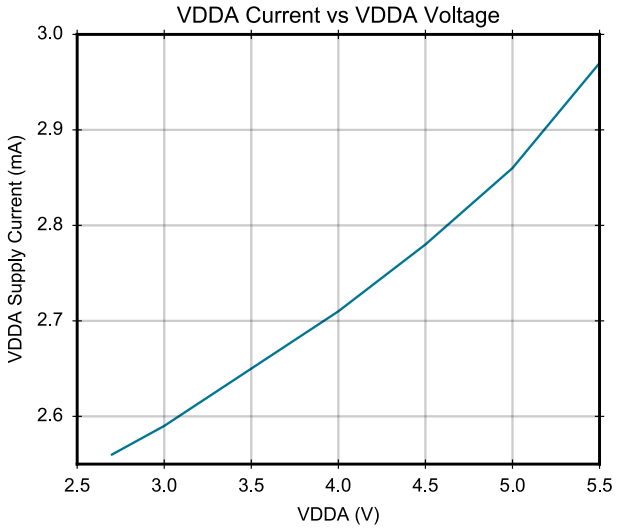
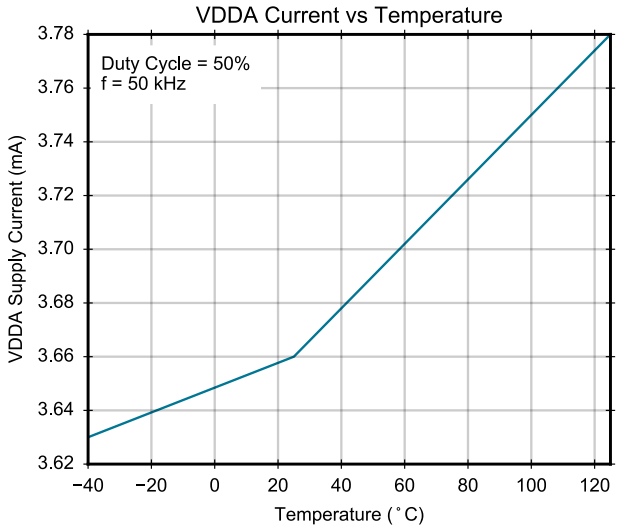
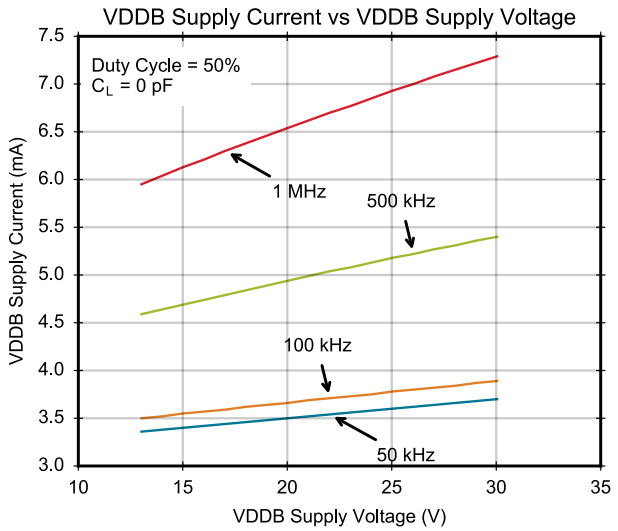


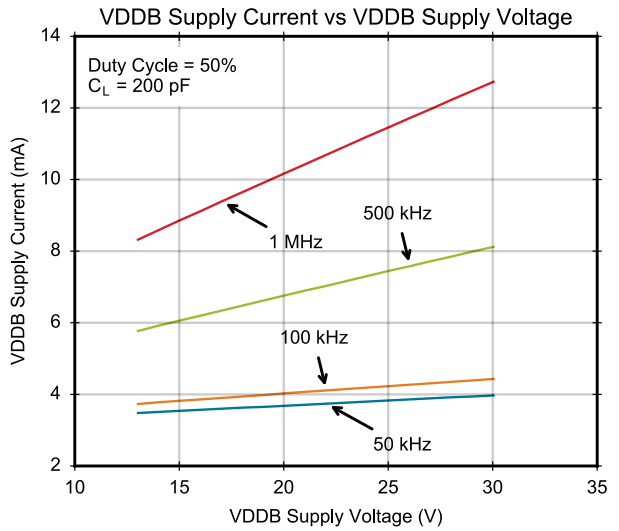
Figure 4.7. Device Reaction to Desaturation Event

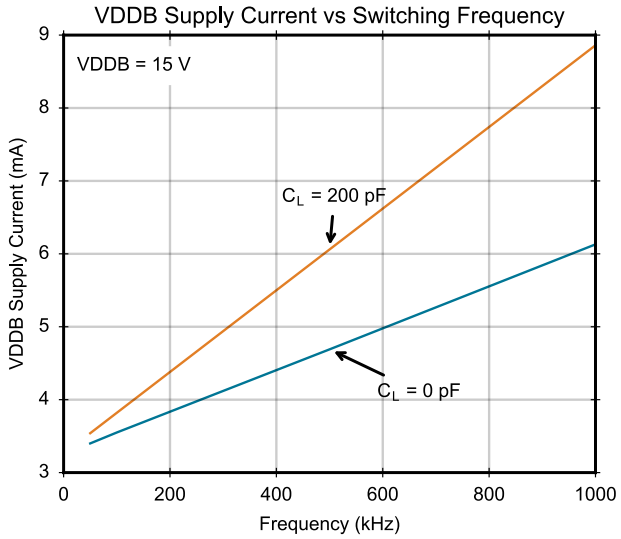
4.2 Typical Operating Characteristics

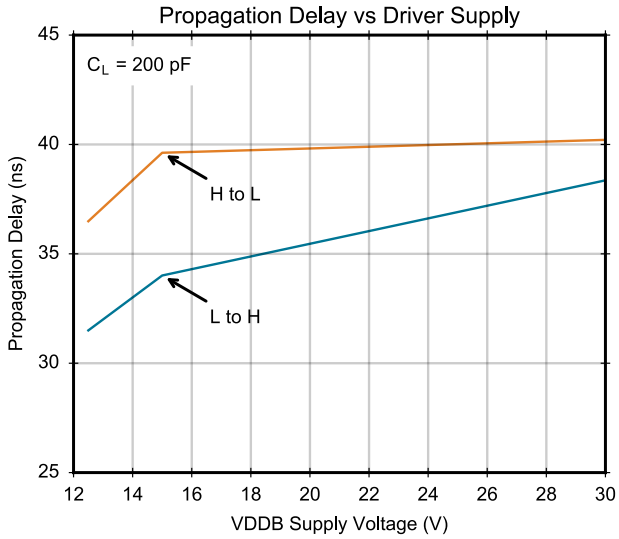


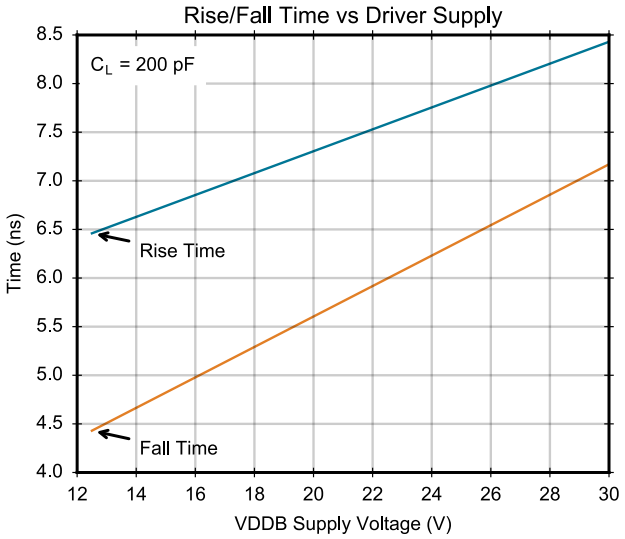


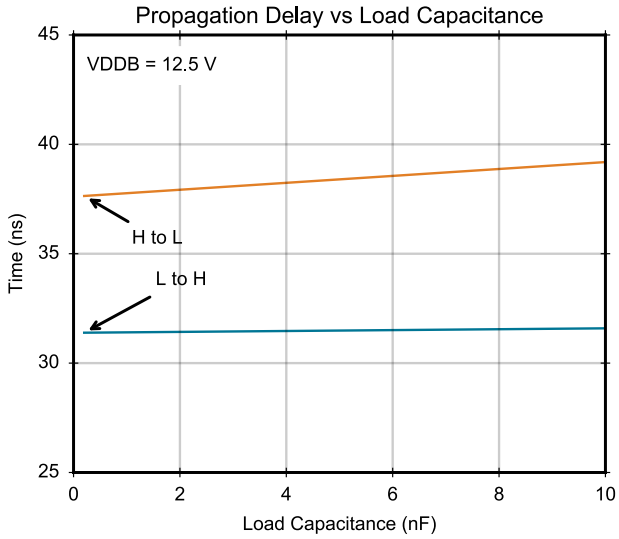


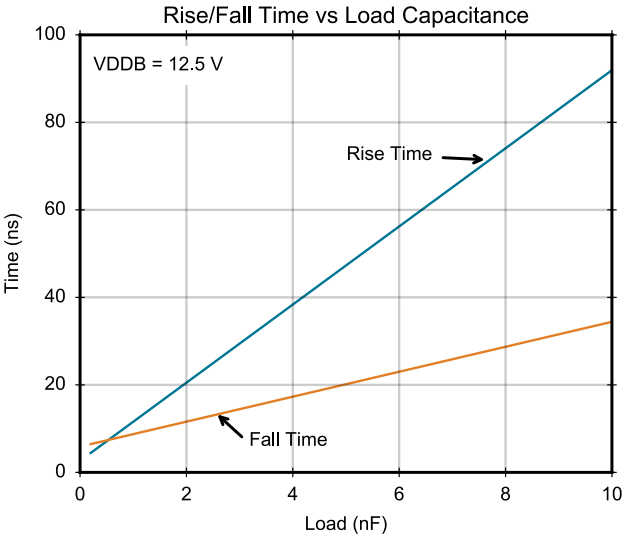


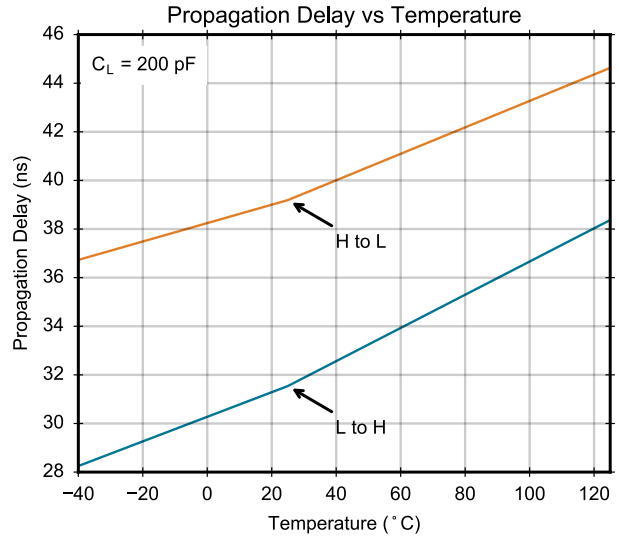

VDDB Supply Current vs Switching Frequency
VDDB = 15 V
C_L = 200 pF
C_L = 0 pF
VDDB Supply Current (mA)
Frequency (kHz)
9
8
7
6
5
4
3
0
200
400
600
800
1000

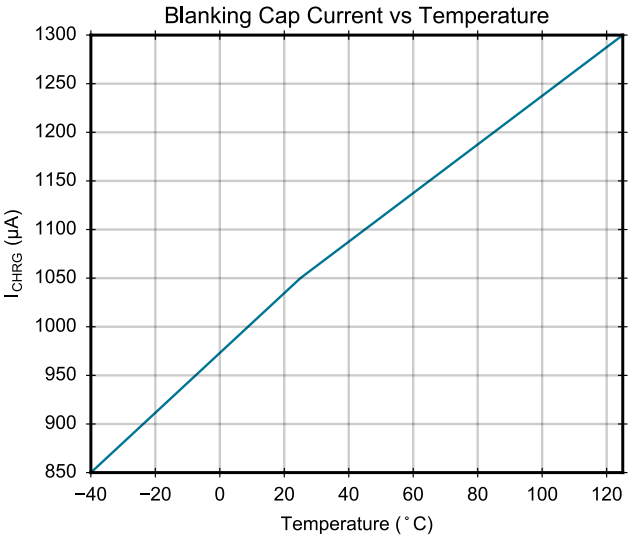

Propagation Delay vs Driver Supply
C_L = 200 pF
H to L
L to H
Propagation Delay (ns)
VDDB Supply Voltage (V)
45
40
35
30
25
12
14
16
18
20
22
24
26
28
30

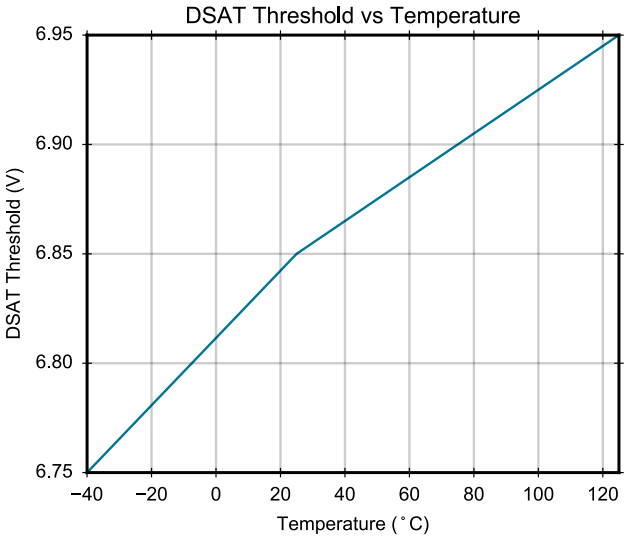

Rise/Fall Time vs Driver Supply
C_L = 200 pF
Rise Time
Fall Time
Time (ns)
VDDB Supply Voltage (V)
8.5
8.0
7.5
7.0
6.5
6.0
5.5
5.0
4.5
4.0
12
14
16
18
20
22
24
26
28
30

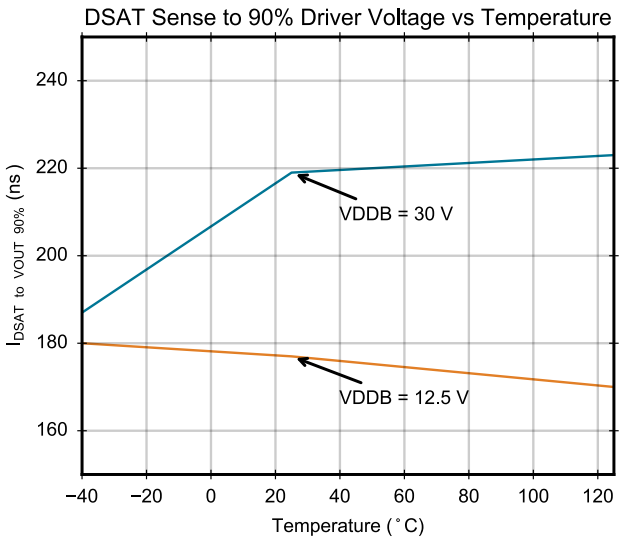

Propagation Delay vs Load Capacitance
VDDB = 12.5 V
H to L
L to H
Time (ns)
Load Capacitance (nF)
45
40
35
30
25
0
2
4
6
8
10

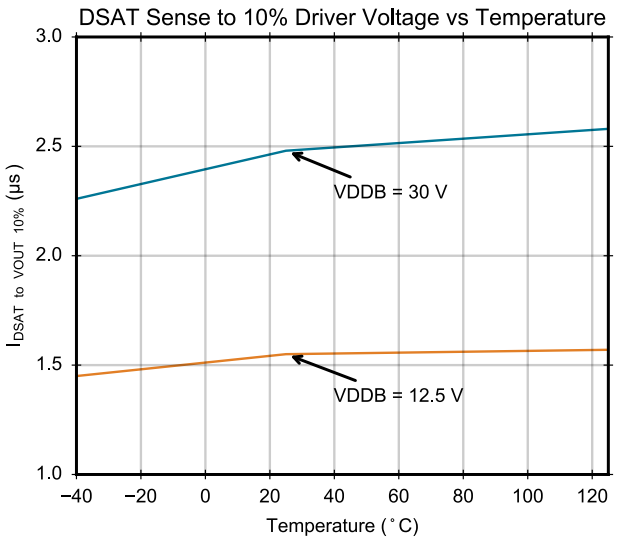

Rise/Fall Time vs Load Capacitance
VDDB = 12.5 V
Rise Time
Fall Time
Time (ns)
Load (nF)
100
80
60
40
20
0
0
2
4
6
8
10

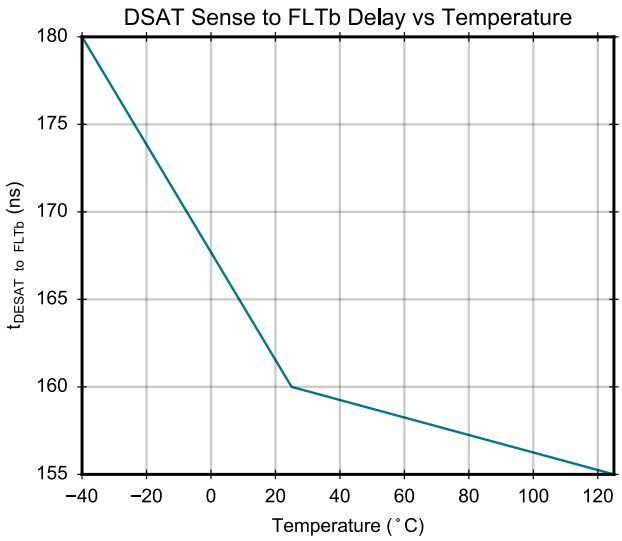

Propagation Delay vs Temperature
C_L = 200 pF
H to L
L to H
Propagation Delay (ns)
Temperature (˚C)
46
44
42
40
38
36
34
32
30
28
−40
−20
0
20
40
60
80
100
120

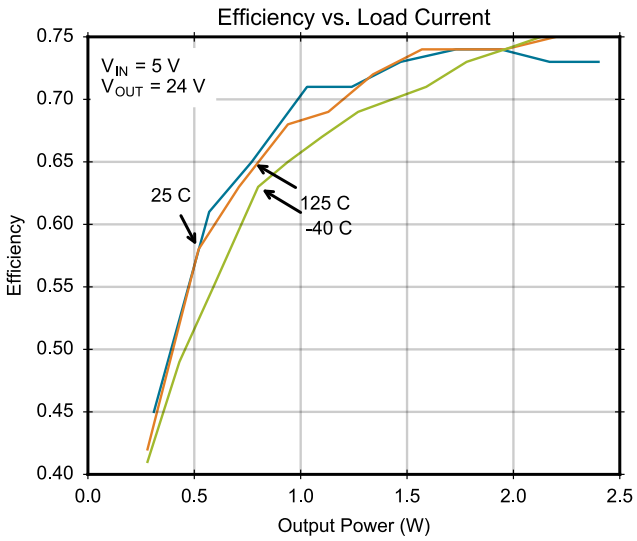

Blanking Cap Current vs Temperature
I_{CHRG} (µA)
1300
1250
1200
1150
1100
1050
1000
950
900
850
−40 −20 0 20 40 60 80 100 120
Temperature (˚C)

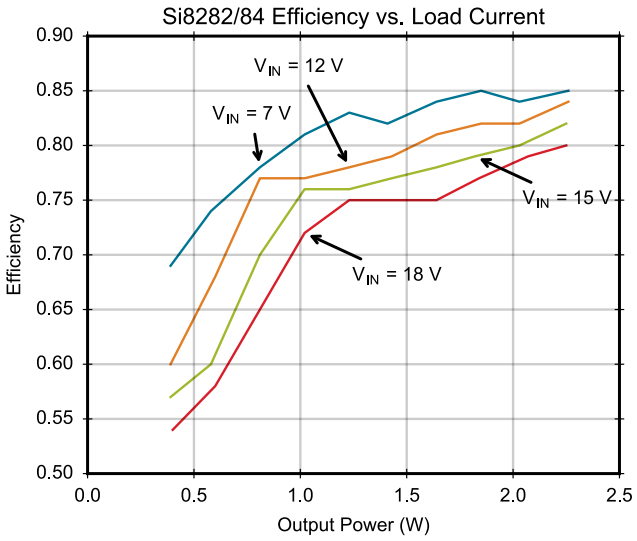

DSAT Threshold vs Temperature
DSAT Threshold (V)
6.95
6.90
6.85
6.80
6.75
−40 −20 0 20 40 60 80 100 120
Temperature (˚C)

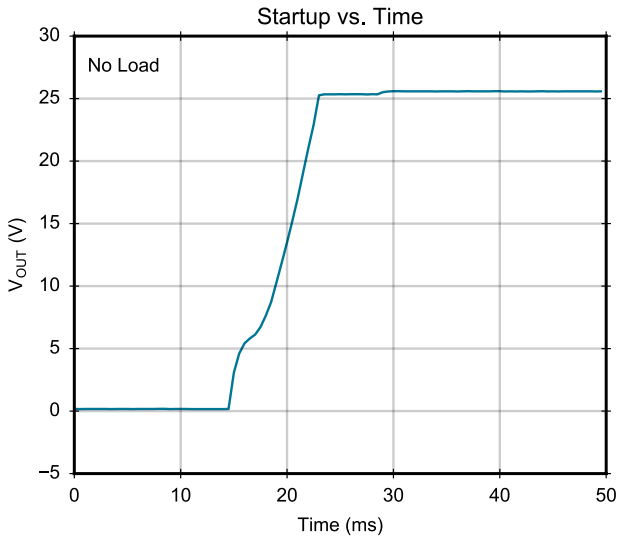

DSAT Sense to 90% Driver Voltage vs Temperature
$t_{DSAT\ to\ VOUT\ 90\%}$ (ns)
240
220
200
180
160
VDDB = 30 V
VDDB = 12.5 V
−40 −20 0 20 40 60 80 100 120
Temperature (˚C)

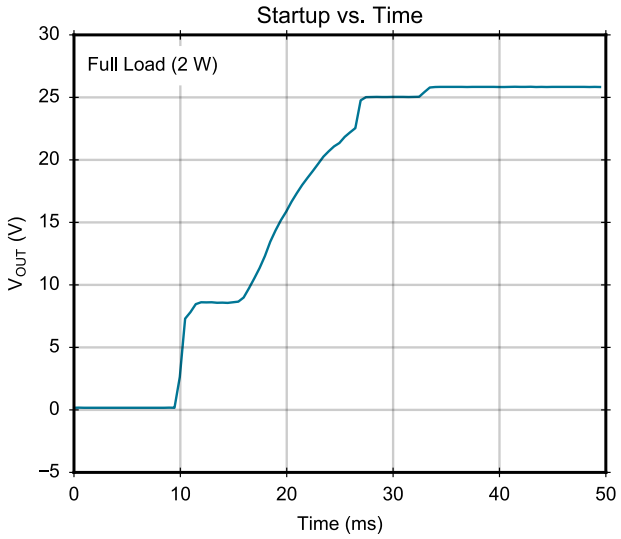

DSAT Sense to 10% Driver Voltage vs Temperature
$t_{DSAT\ to\ VOUT\ 10\%}$ (µs)
3.0
2.5
2.0
1.5
1.0
VDDB = 30 V
VDDB = 12.5 V
−40 −20 0 20 40 60 80 100 120
Temperature (˚C)

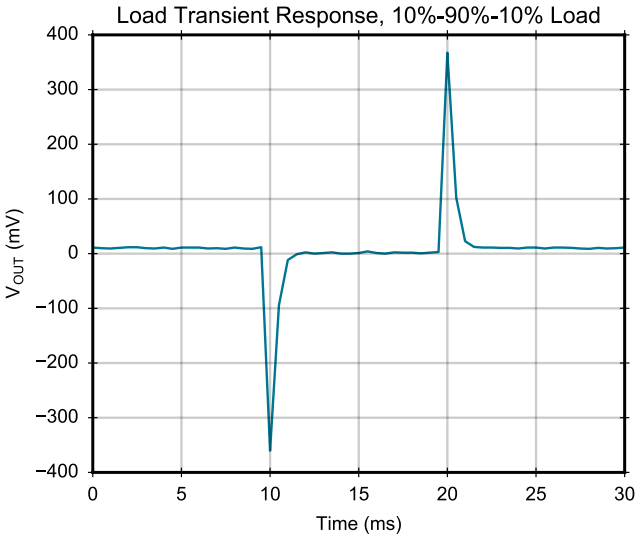

DSAT Sense to FLTb Delay vs Temperature
$t_{DESAT\ to\ FLTb}$ (ns)
180
175
170
165
160
155
−40 −20 0 20 40 60 80 100 120
Temperature (˚C)


Efficiency vs. Load Current
V_{IN} = 5 V
V_{OUT} = 24 V
25 C
125 C
-40 C
Efficiency
0.75
0.70
0.65
0.60
0.55
0.50
0.45
0.40
0.0 0.5 1.0 1.5 2.0 2.5
Output Power (W)


Si8282/84 Efficiency vs. Load Current
Efficiency
Output Power (W)
V_{IN} = 12 V
V_{IN} = 7 V
V_{IN} = 15 V
V_{IN} = 18 V
0.90
0.85
0.80
0.75
0.70
0.65
0.60
0.55
0.50
0.0
0.5
1.0
1.5
2.0
2.5


Startup vs. Time
No Load
V_{OUT} (V)
Time (ms)
30
25
20
15
10
5
0
−5
0
10
20
30
40
50


Startup vs. Time
Full Load (2 W)
V_{OUT} (V)
Time (ms)
30
25
20
15
10
5
0
−5
0
10
20
30
40
50


Load Transient Response, 10%-90%-10% Load
V_{OUT} (mV)
Time (ms)
400
300
200
100
0
−100
−200
−300
−400
0
5
10
15
20
25
30

4.3 Regulatory Information

Table 4.3. Regulatory Information (Pending)[1, 2]

CSA
The Si828x is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si828x is supported according to EN62368-1. For more details, see File 5028467.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si828x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage (V_{ISO}) for basic protection.
CQC
The Si828x is certified under GB4943.1-2011.
Rated up to 250 V_{RMS} reinforced insulation working voltage, at 5000 meters.
Note: 1. Regulatory Certifications apply to 3.75 and 5.0 kV_{RMS} rated devices, which are production tested to 4.5 and 6.0 kV_{RMS} for 1 sec, respectively. 2. For more information, see Section 1. Si8281/82/83/84 Ordering Guide.

Table 4.4. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			WB SOIC	
Nominal External Air Gap (Clearance)[1]	CLR		8.0	mm
Nominal External Tracking (Creepage)	CRP		8.0	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.016	mm
Tracking Resistance	PTI or CTI	IEC60112	600	V
Erosion Depth	ED		0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1	pF

Note:

1. The values in this table correspond to the nominal creepage and clearance values as detailed in 6.1 Package Outline: 20-Pin Wide Body SOIC and 6.3 Package Outline: 24-Pin Wide Body SOIC. VDE certifies the clearance and creepage limits as 8.5 mm minimum for the WB SOIC. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 7.6 mm minimum for the WB SOIC package.
2. To determine resistance and capacitance, the Si828x is converted into a 2-terminal device. All pins on input side are shorted together to form the first terminal, and similarly, all pins on the output side are shorted together to form the second terminal. The parameters are then measured between these two terminals.

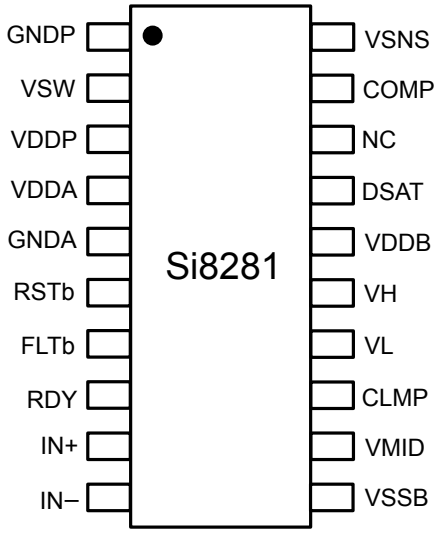
Table 4.5. IEC 60664-1 Ratings

Parameter	Test Condition	Specification
		WB SOIC
Basic Isolation Group	Material Group	I
Overvoltage Category	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 600 V_{RMS}	I-III

Table 4.6. Thermal Characteristics

Parameter	Symbol	Typ		Unit
		WB SOIC-20	WB SOIC-24	
IC Junction-to-Air Thermal Resistance	θ_{JA}	74	74	°C/W

5. Pin Descriptions



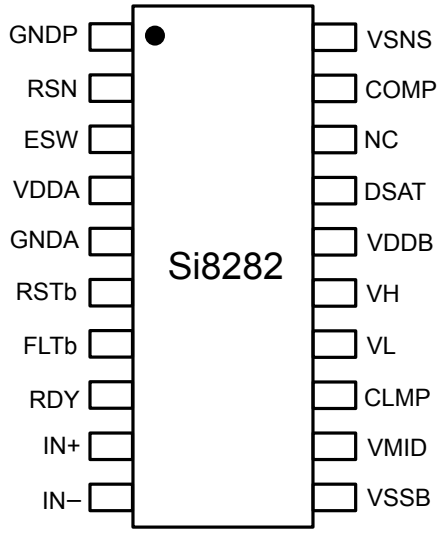


Table 5.1. Si8281/82 Pin Descriptions

Name	Si8281 Pin #	Si8282 Pin #	Description
GNDP	1	1	Power stage ground
VSW	2	—	Power stage internal switch
RSN	—	2	Power stage current sense
VDDP	3	—	Power stage supply
ESW	—	3	Power stage external switch drive
VDDA	4	4	Input side low voltage power supply
GNDA	5	5	Input side low voltage ground
RSTb	6	6	Reset fault condition
FLTb	7	7	Fault condition signal
RDY	8	8	UVLO ready signal
IN+	9	9	Driver control plus
IN–	10	10	Driver control minus
VSSB	11	11	Output side low voltage power supply
VMID	12	12	Drain reference for driven switch
CLMP	13	13	Miller clamp
VL	14	14	Low gate drive
VH	15	15	High gate drive
VDDB	16	16	Output side low voltage power supply
DSAT	17	17	Desaturation detection input
NC[1]	18	18	No connect
COMP	19	19	dc/dc compensation
VSNS	20	20	dc/dc voltage feedback

Name	Si8281 Pin #	Si8282 Pin #	Description

Note:

1. No Connect. These pins may be internally connected. For optimal performance and safety, these pins must be connected to their respective grounds: GNDA for input side and VSSB for output side.

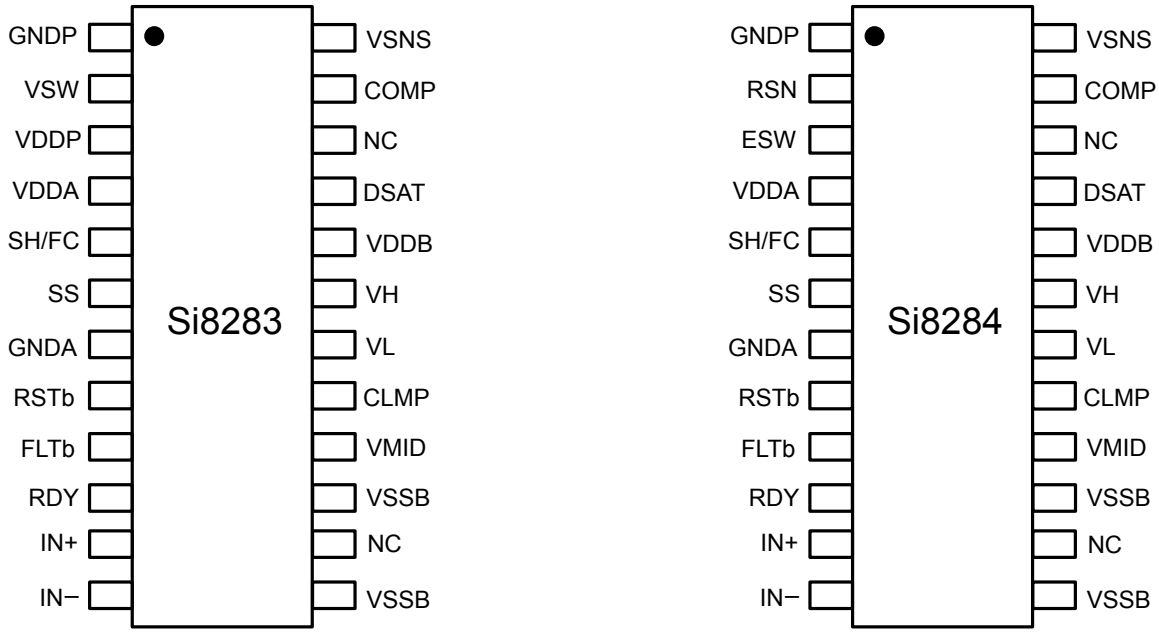


Table 5.2. Si8283/84 Pin Descriptions

Name	Si8283 Pin #	Si8284 Pin #	Description
GNDP	1	1	Power stage ground
VSW	2	—	Power stage internal switch
RSN	—	2	Power stage current sense
VDDP	3	—	Power stage supply
ESW	—	3	Power stage external switch drive
VDDA	4	4	Input side low voltage power supply
SH/FC	5	5	Shutdown and Switch frequency control
SS	6	6	Soft startup control
GNDA	7	7	Input side low voltage ground
RSTb	8	8	Reset fault condition
FLTb	9	9	Fault condition signal
RDY	10	10	UVLO ready signal
IN+	11	11	Driver control plus
IN–	12	12	Driver control minus
VSSB	13, 15	13, 15	Output side low voltage power supply
VMID	16	16	Drain reference for driven switch
CLMP	17	17	Miller clamp
VL	18	18	Low gate drive
VH	19	19	High gate drive
VDDB	20	20	Output side low voltage power supply
DSAT	21	21	Desaturation detection input

Name	Si8283 Pin #	Si8284 Pin #	Description
NC[1]	14, 22	14, 22	No connect
COMP	23	23	dc/dc compensation
VSNS	24	24	dc/dc voltage feedback

Note:

1. No Connect. These pins may be internally connected. For optimal performance and safety, these pins must be connected to their respective grounds: GNDA for input side and VSSB for output side.

6. Packaging

6.1 Package Outline: 20-Pin Wide Body SOIC

The figure below illustrates the package details for the Si8281/82 in a 20-Pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

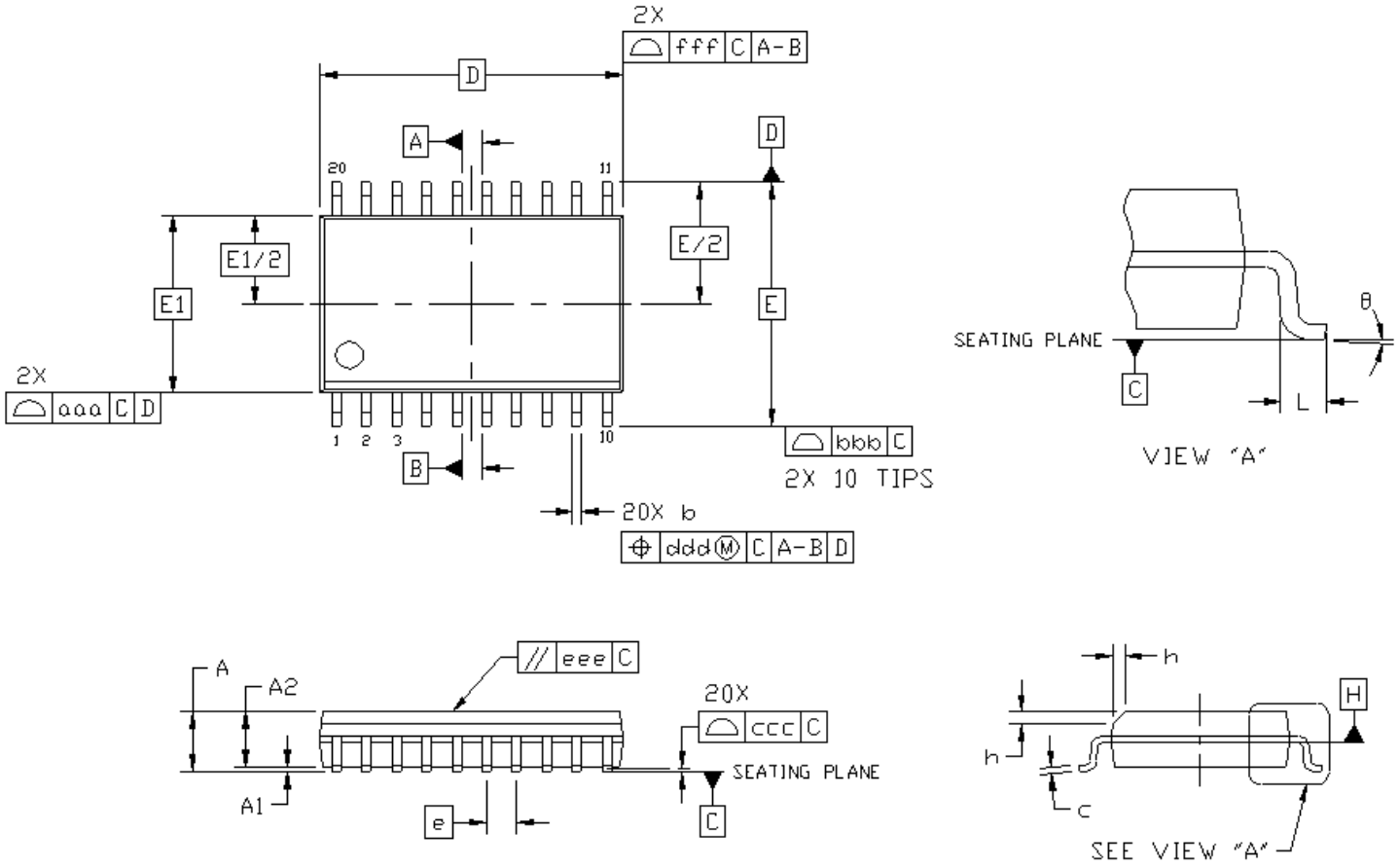


Figure 6.1. 20-Pin Wide Body SOIC

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	12.80 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°

Symbol	Millimeters	
	Min	Max
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AC.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

6.2 Land Pattern: 20-Pin Wide Body SOIC

The figure below illustrates the recommended land pattern details for the Si8281/2 in a 20-Pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

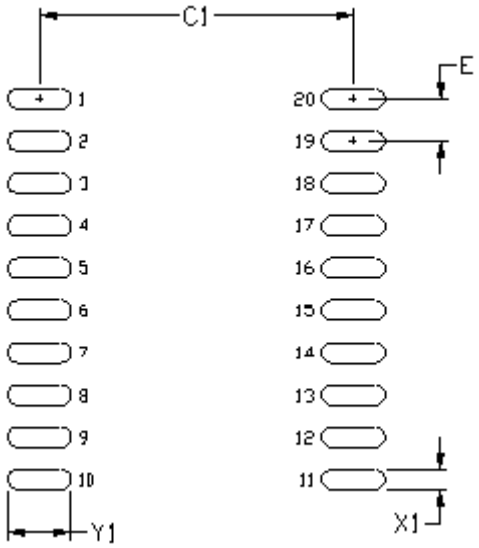


Figure 6.2. PCB Land Pattern: 20-Pin Wide Body SOIC

Table 6.1. 20-Pin Wide Body SOIC Land Pattern Dimensions[1, 2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Note:

1. This Land Pattern Design is based on IPC-7351 design guidelines for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

6.3 Package Outline: 24-Pin Wide Body SOIC

The figure below illustrates the package details for the Si8283/4 in a 24-Pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

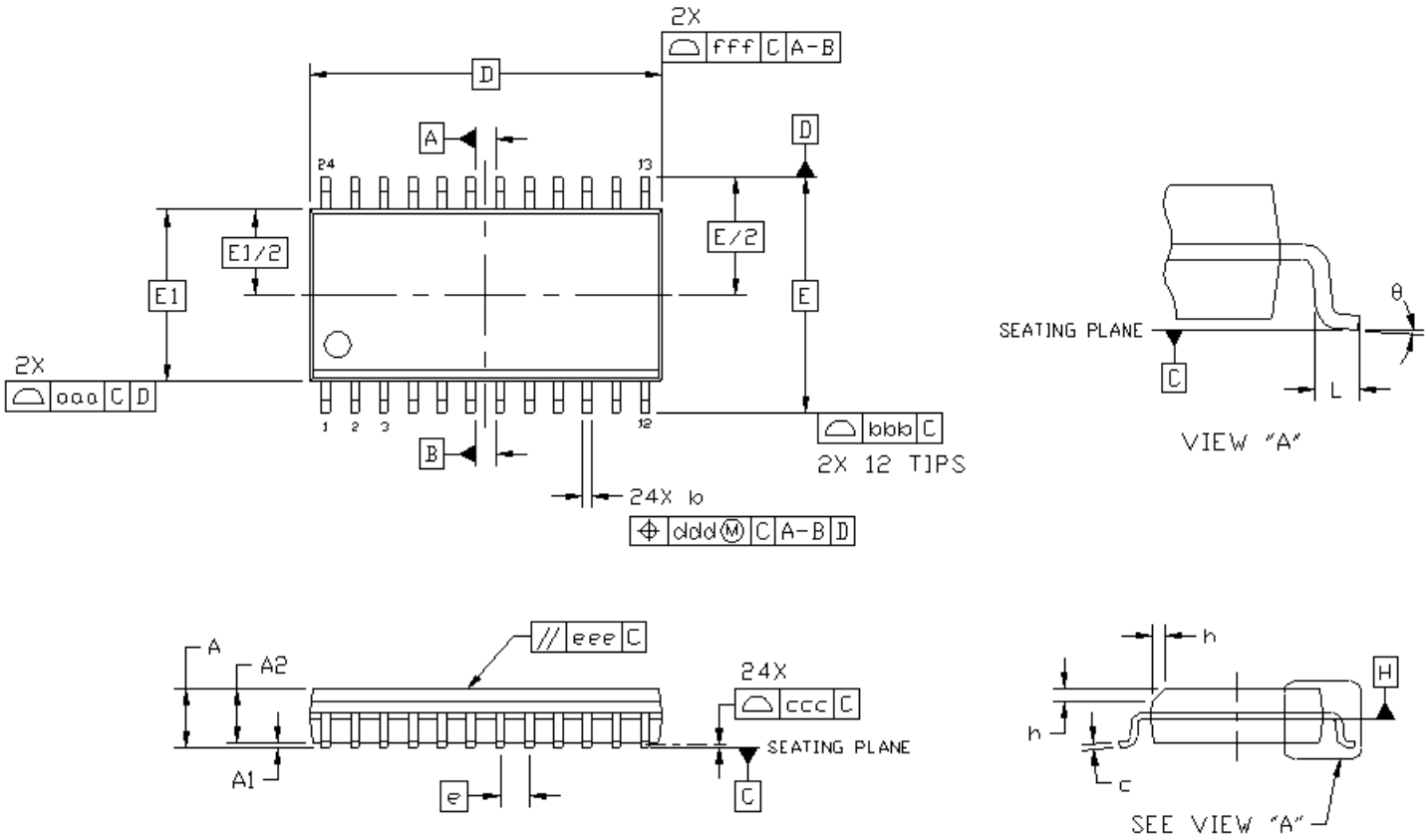


Figure 6.3. 24-Pin Wide Body SOIC

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	15.40 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10

Symbol	Millimeters	
	Min	Max
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AD.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

6.4 Land Pattern: 24-Pin Wide Body SOIC

The figure below illustrates the recommended land pattern details for the Si8283/4 in a 24-Pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

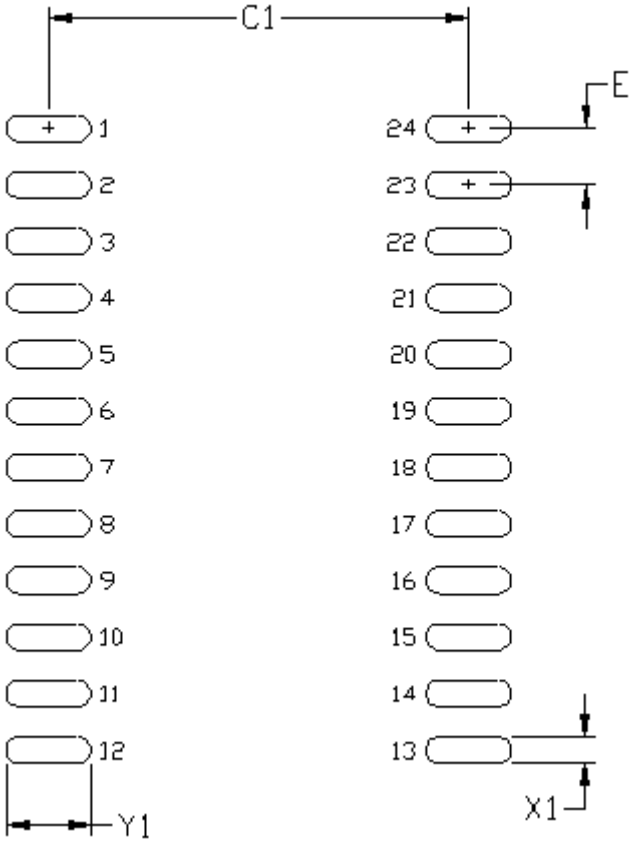


Figure 6.4. PCB Land Pattern: 24-Pin Wide Body SOIC

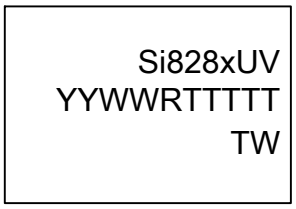
Table 6.2. 24-Pin Wide Body SOIC Land Pattern Dimensions[1, 2]

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

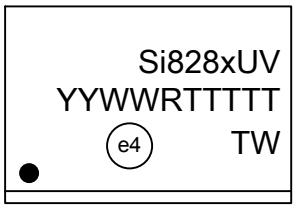
Note:

1. This Land Pattern Design is based on IPC-7351 design guidelines for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

6.5 Top Marking: 20-Pin and 24-Pin Wide Body SOIC



Si8281/82 Top Marking



Si8283/84 Top Marking

Table 6.3. Si8281/2/3/4 Top Marking Explanation

Line 1 Marking:	Customer Part Number	Si8281, Si8282, Si8283, Si8284 = ISOdriver U = UVLO level: B = 9 V; C = 12 V; D = 13 V; E = 15 V V = Isolation rating: C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	RTTTTT = Mfg Code	Manufacturing code “R” indicates revision
Line 3 Marking:	Circle = 43 mils Diameter TW	"e4" = Pb-Free Symbol Country of Origin

7. Revision History

Revision 206406A

October, 2022

- Updated revision number from decimal format to Agile-generated revision number.
- Updated "Soft Start (Si8283 and Si8284 Only)" to "3.2.7 DC-DC Startup and Soft Start".
- Added 3.2.7.1 Startup Fault Behavior.

Revision 2.1

July, 2021

- Corrected DCDC Test Conditions (for line regulation, load regulation), added "RSN Overload Threshold" spec, changed "restart delay from fault event" to 83ms, fixed cosmetic issues--all in Table 4.1 Electrical Specifications on page 19.

Revision 2.0

April, 2021

- Restructured and updated Product Overview and Applications Information sections
- Updated numerous Electrical specifications in Table 4.1 Electrical Specifications on page 19 and Table 4.2 Absolute Maximum Ratings[1] on page 25
- Clarified timing diagrams in Section 4.1 Timing Diagrams
- Updated Regulatory Information in Table 4.3 Regulatory Information (Pending)[1, 2] on page 31
- Updated Table 3.1 Si828x Recommended Transformers on page 18
- Updated Table 4.7 IEC60747-17 Safety Limiting Values, Table 4.6 Thermal Characteristics on page 32, and Figure 4.8 WB SOIC20/24 Thermal Derating Curve.

Revision 1.1

August, 2018

- Corrected typo for minimum VDDA and VDDB in Table 4.1 Electrical Specifications on page 19 to match the max UVLO values stated in the same table.

Revision 1.0

March, 2018

- Updated Safety Regulatory Approvals section on page 1, and Tables 4.3, 4.4, and 4.6 to conform with isolation component standard terminology.
- Removed references to IEC 60747-5-5 throughout the document and replaced with VDE 0884.
- Updated Table 2.2, Recommended Transformers.
- Updated Thermal Derating Curve, Figure 4.6.

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