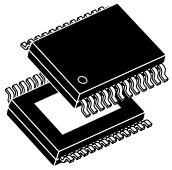
# LNBH23

## LNBs supply and control IC with step-up and I²C interface

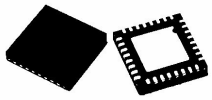
**Datasheet – production data**

## Features

- Complete interface between LNB and I²C bus
- Built-in DC-DC converter for single 12 V supply operation and high efficiency (typ. 93% @ 0.75 A), with integrated NMOS
- Selectable output current limit by external resistor
- Compliant with main satellite receiver systems specifications
- New accurate built-in 22 kHz tone generator suits widely accepted standards (patent pending)
- Fast oscillator start-up facilitates DiSEqC™ encoding
- Built-in 22 kHz tone detector supports bi-directional DiSEqC™ 2.0
- Very low-drop post regulator and high efficiency step-up PWM with integrated power NMOS allow low power losses
- Two output pins suitable to by-pass the output R-L filter and avoid any tone distortion (R-L filter as per DiSEqC™ 2.0 specs, see typ. application circuits)
- Overload and over-temperature internal protections with I²C diagnostic bits
- Output voltage and output current level diagnostic feedback by I²C bits
- LNB short circuit dynamic protection
- ± 4 kV ESD tolerant on output power pins



**PowerSSO-24 (Exposed pad)**



**QFN32 (5 x 5 mm.) (Exposed pad)**

## Description

Intended for analog and digital satellite receivers/sat-TV, sat-PC cards, the LNBH23 is a monolithic voltage regulator and interface IC, assembled in PowerSSO-24 ePAD and QFN32 (5 x 5 mm.) ePAD, specifically designed to provide the 13/18 V power supply and the 22 kHz tone signalling to the LNB down-converter in the antenna dish or to the multi-switch box. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with simple design and I²C standard interfacing.

**Table 1. Device summary**

| Order code | Package | Packaging |
|---|---|---|
| LNBH23PPR | PowerSSO-24 (Exposed pad) | Tape and reel |
| LNBH23QTR | QFN32 (Exposed pad) | Tape and reel |



This is information on a product in full production. www.st.com

# Contents


1 **Block diagram . . . . . 3**

2 **Application information . . . . . 4**

2.1 DiSEqC™ data encoding and decoding . . . . . 4

2.2 DiSEqC™ 2.0 implementation . . . . . 4

2.3 DiSEqC™ 1.X implementation . . . . . 4

2.4 Data encoding by external tone generator (EXTM) . . . . . 5

2.5 I²C interface . . . . . 5

2.6 Output voltage selection . . . . . 5

2.7 Diagnostic and protection functions . . . . . 6

2.8 Output voltage diagnostic - VMON . . . . . 6

2.9 22 kHz tone diagnostic - TMON . . . . . 6

2.10 Minimum output current diagnostic - IMON . . . . . 6

2.11 Output current limit selection . . . . . 7

2.12 Over-current and short circuit protection and diagnostic . . . . . 7

2.13 Thermal protection and diagnostic . . . . . 7

3 **Pin configuration . . . . . 8**

4 **Maximum ratings . . . . . 10**

5 **Application circuit . . . . . 11**

6 **I²C bus interface . . . . . 13**

6.1 Data validity . . . . . 13

6.2 Start and stop condition . . . . . 13

6.3 Byte format . . . . . 13

6.4 Acknowledge . . . . . 13

6.5 Transmission without acknowledge . . . . . 13

7 **LNBH23 software description . . . . . 16**

7.1 Interface protocol . . . . . 16

7.2 System register (SR, 1 byte) . . . . . 16

7.3 Transmitted data (I²C bus write mode) . . . . . 16
7.4 Diagnostic received data (I²C read mode) . . . . . 17
7.5 Power-on I²C interface reset . . . . . 18
7.6 Address pin . . . . . 18
7.7 DiSEqC™ implementation . . . . . 18

**8 Electrical characteristics . . . . . 19**

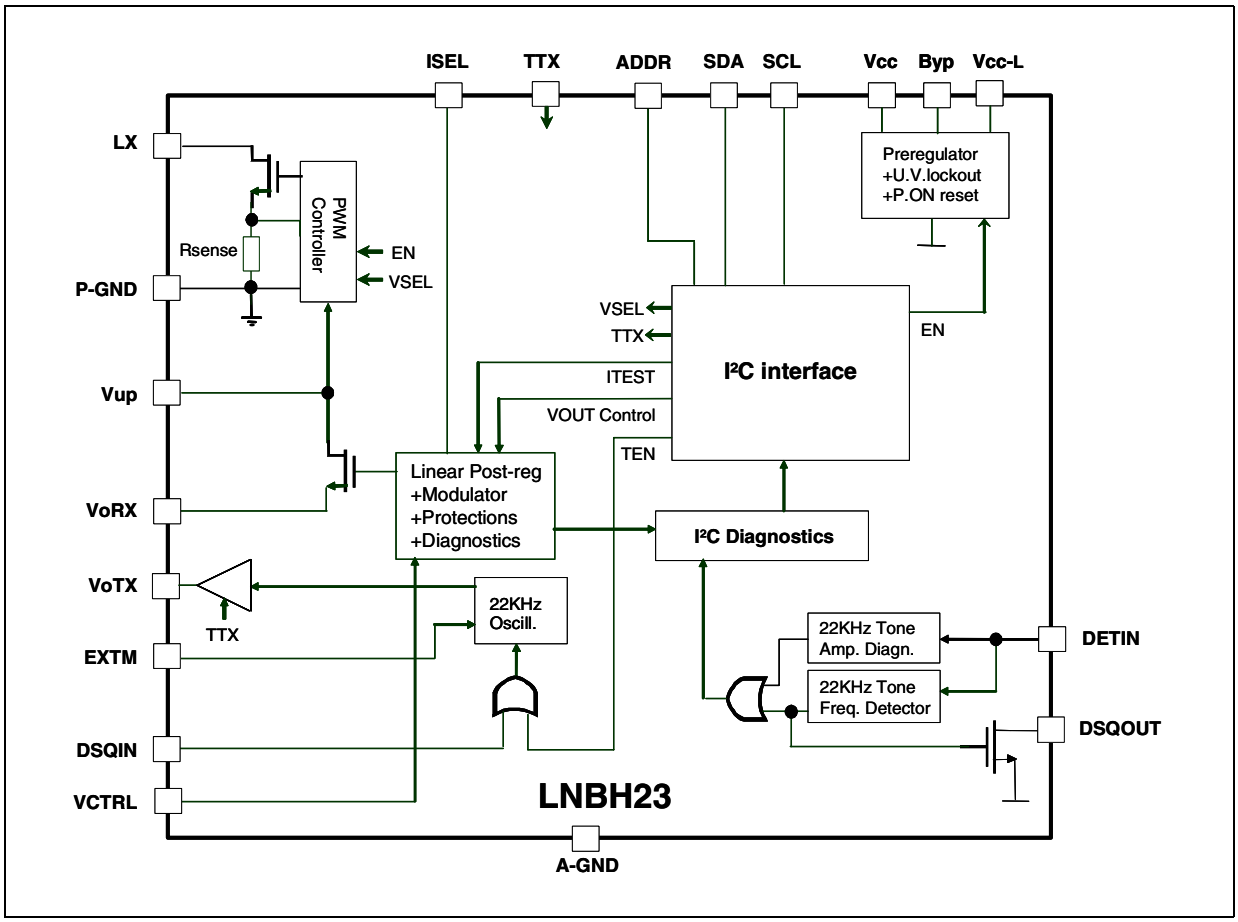
**9 Typical performance characteristics . . . . . 22**

**10 Package mechanical data . . . . . 26**

**11 Revision history . . . . . 31**

# 1 Block diagram

**Figure 1. Block diagram**



# 2 Application information

This IC has a built-in DC-DC step-up converter with integrated NMOS that, from a single source from 8 V to 15 V, generates the voltages ($V_{UP}$) that let the linear post-regulator to work at a minimum dissipated power of 0.375 W Typ. @ 500 mA load (the linear post-regulator drop voltage is internally kept at $V_{UP}$-$V_{ORX}$=0.75 V typ.). An under voltage lockout circuit will disable the whole circuit when the supplied $V_{CC}$ drops below a fixed threshold (6.7 V typically).

*Note: In this document the output voltage ($V_O$) is intended as the voltage present at the linear post-regulator output ($V_{ORX}$ pin).*

## 2.1 DiSEqC™ data encoding and decoding

The new internal 22 kHz tone generator (patent pending) is factory trimmed in accordance to the standards, and can be selected by I²C interface TTX bit (or TTX pin) and activated by a dedicated pin (DSQIN) that allows immediate DiSEqC™ data encoding, or through TEN I²C bit in case the 22 kHz presence is requested in continuous mode. In stand-by condition (EN bit LOW) The TTX function must be disabled setting TTX to LOW.

## 2.2 DiSEqC™ 2.0 implementation

The built-in 22 kHz tone detector completes the fully bi-directional DiSEqC™ 2.0 interfacing (see *Note 1*). It's input pin (DETIN) must be AC coupled to the DiSEqC™ BUS, and extracted PWK data are available on the DSQOUT pin. To comply to the bi-directional DiSEqC™ 2.0 bus hardware requirements an output R-L filter is needed. The LNBH23 is provided with two output pins, one for the dc voltage output ($V_{oRX}$) and one for the 22 kHz tone transmission ($V_{oTX}$). The $V_{oTX}$ must be activated only during the tone transmission while the $V_{oRX}$ provides the 13/18 V output voltage. This allows the 22 kHz Tone to pass without any losses due to the R-L filter impedance (see *Figure 4* typ. application circuit). During the 22 kHz transmission, in DiSEqC™ 2.0 applications, activated by DSQIN pin or by the TEN bit, the $V_{oTX}$ pin must be preventively set ON by the TTX function. This can be controlled both through the TTX pin and by I²C bit. As soon as the tone transmission is expired, the $V_{oTX}$ must be disabled by setting the TTX to LOW to set the device in the 22 kHz receiving mode. The 13/18 V power supply is always provided to the LNB from the $V_{oRX}$ pin through the R-L filter.

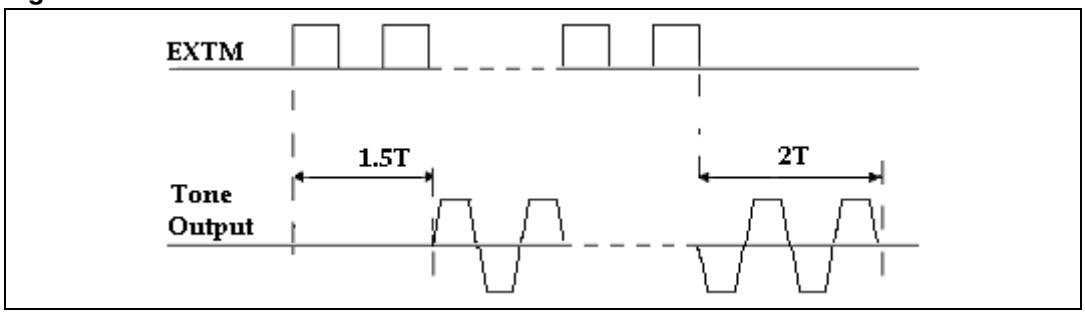
## 2.3 DiSEqC™ 1.X implementation

When the LNBH23 is used in DiSEqC™ 1.x applications the R-L filter is always needed for the proper operation of the new 22 kHz tone generator (patent pending. See application circuit). Also in this case, the TTX function must be preventively enabled before to start the 22 kHz data transmission and disabled as soon as the data transmission has been expired. The tone can be activated both with the DSQIN pin or the TEN I²C bit. The DSQIN internal circuit activates the 22 kHz tone on the $V_{oTX}$ output with 0.5 cycles ±25 µs delay from the TTL signal presence on the DSQIN pin, and it stops with 1 cycles ±25 µs delay after the TTL signal is expired.

## 2.4 Data encoding by external tone generator (EXTM)

In order to improve design flexibility an external tone input pin is available (EXTM). The EXTM is a logic input pin which activates the 22 kHz tone output, on the $V_{oTX}$ pin, by using the LNBH23 integrated tone generator (similarly to the DSQIN pin function). As a matter of fact, the output tone waveform characteristics will be always internally controlled by the LNBH23 tone generator and the EXTM signal will be used just as a timing control of the DiSEqC tone data encoding on the $V_{oTX}$ output. A TTL compatible 22 kHz signal is required for the proper control of the EXTM pin function. Before to send the TTL signal on the EXTM pin, the $V_{oTX}$ tone generator must be previously enabled through the TTX function (TTX pin or TTX bit set HIGH). As soon as the EXTM internal circuit detects the 22 kHz TTL signal code, it activates the 22 kHz tone on the $V_{oTX}$ output with 1.5 cycles ±25 µs delay from the TTL signal presence on the EXTM pin, and it stops with 2 cycles ±25 µs delay after the TTL signal is expired. Refer to the below *Figure 2*.

**Figure 2. EXTM waveform**




## 2.5 I²C interface

The main functions of the IC are controlled via I²C bus by writing 8 bits on the system register (SR 8 bits in write mode). On the same register there are 8 bits that can be read back (SR 8 bits in read mode) to provide 8 diagnostic functions: five bits will report the diagnostic status of five internal monitoring functions (IMON, VMON, TMON, OTF, OLF) while, three will report the last output voltage register status (EN, VSEL, LLC) received by the IC (see below diagnostic functions section).

## 2.6 Output voltage selection

When the IC sections are in stand-by mode (EN bit LOW), the power blocks are disabled. When the regulator blocks are active (EN bit HIGH), the output can be logic controlled to be 13 or 18 V by means of the $V_{SEL}$ bit (Voltage SELect) for remote controlling of non-DiSEqC LNBs. Additionally, the LNBH23 is provided with the LLC I²C bit that increases the selected voltage value by +1 V to compensate the excess of voltage drop along the coaxial cable. The LNBH23 is also compliant to the USA LNB power supply standards. In order to allow fast transition of the output voltage from 18 V to 13 V and vice versa, the LNBH23 is provided with the VCTRL TTL pin which keeps the output to 13 V when it is set LOW and to 18 V when it is set HIGH or floating. $V_{SEL}$ and, if required, LLC bits must be set HIGH before to use the VCTRL pin to switch the output voltage level. If VCTRL=1 or floating $V_{oRX}$=18.5 V (or 19.5 V if LLC=1). With VCTRL=0 $V_{oRX}$=13.4 V (LLC= either 0 or 1). Be aware that the VCTRL pin controls only the linear regulator $V_{oRX}$ stage while the step-up $V_{UP}$ voltage is controlled only through the VSEL and LLC I²C bits, that is: Even if VCTRL=0 (keeping $V_{oRX}$=13.4 V) you will have $V_{UP}$=19.25 V typ when $V_{SEL}$=1 and 20.25 V with $V_{SEL}$=LLC=1.

This means that VCTRL=0 must be used only for short time to avoid the higher power dissipation. In stand-by condition (EN bit LOW) all the I²C bits and the TTX pin must be set LOW (if the TTX pin is not used it can be left floating but the TTX bit must be set LOW during the stand-by condition).

## 2.7 Diagnostic and protection functions

The LNBH23 has 5 diagnostic internal functions provided via I²C bus by reading 5 bits on the system register (SR bits in read mode). All the diagnostic bits are, in normal operation (no failure detected), set to LOW. Two diagnostic bits are dedicated to the over-temperature and over-load protections status (OTF and OLF) while, the remaining 3 bits, are dedicated to the output voltage level (VMON), 22 kHz tone (TMON) and to the minimum load current diagnostic function (IMON).

## 2.8 Output voltage diagnostic - VMON

When $V_{SEL}$=0 or 1 and LLC=0, the output voltage pin ($V_{oRX}$) is internally monitored and, as long as the output voltage level is below the guaranteed limits the VMON I²C bit is set to "1". The output voltage diagnostic is valid only with LLC=0. Any VMON information with LLC=1 must be disregarded by the MCU.

## 2.9 22 kHz tone diagnostic - TMON

The 22 kHz tone can be internally detected and monitored if DETIN pin is connected to the LNB output bus (see typical application circuits *Figure 4*) through a decoupling capacitor. The tone diagnostic function is provided with the TMON I²C bit. If the 22 kHz Tone amplitude and/or the tone frequency is out of the guaranteed limits (see TMON limits in the electrical characteristics *Table 13*), the TMON I²C bit is set to "1".

## 2.10 Minimum output current diagnostic - IMON

In order to detect the output load absence (no LNB connected on the bus or cable not connected to the IRD) the LNBH23 is provided with a minimum output current flag by the IMON I²C bit in read mode, which is set to "1" if the output current is lower than 12 mA typically with ITEST=1 and 6 mA with ITEST=0. The minimum current diagnostic function (IMON) is always active. In order to make it work even in a multi-IRD configuration (multi-switch), where the supply current could be sunk only from the higher supply voltage connected to the multi-switch box, the LNBH23 is provided with the AUX I²C bit which can be set HIGH, in write mode by the MCU, before to read the IMON I²C bit status, to force the LNBH23 output voltage as the highest voltage on the bus (22 V typ.) during the minimum current diagnostic phase. When the AUX bit is set to HIGH, the $V_{oRX}$ is set to 22 V (typ.) and $V_{UP}$ is set to 22.75 V ($V_{UP}$ = $V_{oRX}$+0.75 V typ.) independently of the VSEL/LLC bits status. If the AUX function is used to force the $V_{oRX}$ to 22 V, it is recommended to set the AUX bit to LOW as soon as the minimum current test phase is expired, so that the $V_{oRX}$ voltage will be controlled again as per the VSEL/LLC bits status. In order to avoid false triggering, the IMON function must be used only with the 22 kHz tone transmission deactivated (TEN=TTX=0 and DSQIN=LOW), otherwise the IMON bit could be erroneously set to 0 even if the output current is below the minimum current thresholds (6 mA or 12 mA). Any TMON information with 22 kHz tone enabled must be disregarded by the MCU.

## 2.11 Output current limit selection

The linear regulator current limit threshold can be set by an external resistor connected to $I_{SEL}$ pin. The resistor value defines the output current limit by the equation:

$I_{MAX}[A] = 10000/R_{SEL}$

where $R_{SEL}$ is the resistor connected between $I_{SEL}$ and GND. The highest selectable current limit threshold is 1.0 A typ with $R_{SEL}$=10 kΩ. The above equation defines the typical threshold value.

## 2.12 Over-current and short circuit protection and diagnostic

In order to reduce the total power dissipation during an overload or a short circuit condition, the device is provided with a dynamic short circuit protection. It is possible to set the short circuit current protection either statically (simple current clamp) or dynamically by the PCL bit of the I²C SR. When the PCL (pulsed current limiting) bit is set lo LOW, the over current protection circuit works dynamically: as soon as an overload is detected, the output current is provided for 90 ms (typ.), after that the output is set in shut-down for a time $T_{OFF}$ of typically 900 ms. Simultaneously the diagnostic OLF I²C bit of the system register is set to "1". After this time has elapsed, the output is resumed for a time $T_{ON}$=1/10 $T_{OFF}$ = 90 ms (typ.). At the end of $T_{ON}$, if the overload is still detected, the protection circuit will cycle again through $T_{OFF}$ and $T_{ON}$. At the end of a full $T_{ON}$ in which no overload is detected, normal operation is resumed and the OLF diagnostic bit is reset to LOW. Typical $T_{ON}$ +$T_{OFF}$ time is 990 ms and an internal timer determines it. This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start-up in most conditions. However, there could be some cases in which a highly capacitive load on the output may cause a difficult start-up when the dynamic protection is chosen. This can be solved by initiating any power start-up in static mode (PCL=1) and, then, switching to the dynamic mode (PCL=0) after a chosen amount of time depending on the output capacitance. Also in static mode, the diagnostic OLF bit goes to "1" when the current clamp limit is reached and returns LOW when the overload condition is cleared.

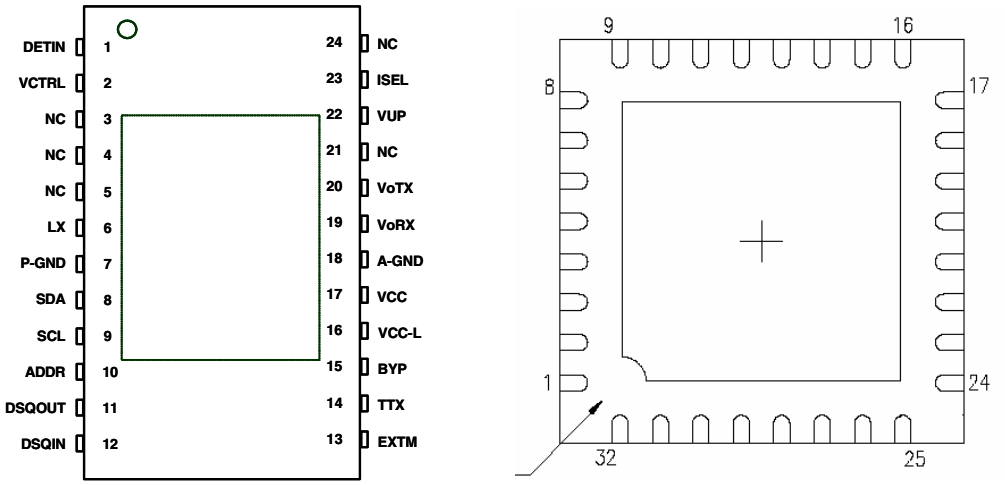
## 2.13 Thermal protection and diagnostic

The LNBH23 is also protected against overheating: when the junction temperature exceeds 150 °C (typ.), the step-up converter and the liner regulator are shut-off, and the diagnostic OTF SR bit is set to "1". Normal operation is resumed and the OTF bit is reset to LOW when the junction is cooled down to 135 °C (typ.).

*Note: 1 External components are needed to comply to bidirectional DiSEqC™ bus hardware requirements. Full compliance of the whole application with DiSEqC™ specifications is not implied by the use of this IC. NOTICE: DiSEqC™ is a trademark of EUTELSAT. I²C is trademark of Philips Semiconductors.*

# 3 Pin configuration

**Figure 3. Pin connections (top view for PowerSSO-24, bottom view for QFN32)**




PowerSSO-24 QFN32 (5 x 5 mm.)

**Table 2. Pin description**

| Pin n° for QFN32 | Pin n° for PSSO-24 | Symbol | Name | Function |
|---|---|---|---|---|
| 19 | 17 | $V_{CC}$ | Supply input | 8 to 15 V IC DC-DC power supply. |
| 18 | 16 | $V_{CC-L}$ | Supply input | 8 to 15 V analog power supply. |
| 4 | 6 | LX | N-MOS drain | Integrated N-Channel power MOSFET drain. |
| 27 | 22 | $V_{UP}$ | Step-Up voltage | Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor. |
| 21 | 19 | $V_{oRX}$ | LDO output port | Output of the integrated low drop linear post-regulator. See truth tables for voltage selections and description. |
| 22 | 20 | $V_{oTX}$ | Output port for 22 kHz tone TX | TX Output to the LNB. See truth tables for selection. |
| 6 | 8 | SDA | Serial data | Bi-directional data from/to I²C bus. |
| 9 | 9 | SCL | Serial clock | Clock from I²C bus. |
| 12 | 12 | DSQIN | DiSEqC input | This pin will accept the DiSEqC code from the main microcontroller. The LNBH23 will use this code to modulate the internally generated 22 kHz carrier. Set to ground if not used. |
| 14 | 14 | TTX | TTX enable | This pin can be used, as well as the TTX I²C bit of the system register, to control the TTX function enable before to start the 22 kHz tone transmission. Set floating or to GND if not used. |
| 29 | 1 | DETIN | Tone decoder input | 22 kHz tone decoder Input, must be AC coupled to the DiSEqC 2.0 bus. |

**Table 2. Pin description (continued)**

| Pin n° for QFN32 | Pin n° for PSSO-24 | Symbol | Name | Function |
|---|---|---|---|---|
| 11 | 11 | DSQOUT | DiSEqC output | Open drain output of the tone decoder to the main microcontroller for DiSEqC 2.0 data decoding. It is LOW when tone is detected on DETIN pin. |
| 13 | 13 | EXTM | External modulation | External modulation logic input pin which activates the 22 kHz tone output on the $V_{oTX}$ pin. Set to ground if not used. |
| 15 | 15 | BYP | By-pass capacitor | Needed for internal pre-regulator filtering. The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device. |
| 10 | 10 | ADDR | Address setting | Two I²C bus addresses available by setting the Address pin level voltage. See address pin characteristics *Table 10* |
| 28 | 23 | ISEL | Current selection | The resistor “RSEL” connected between ISEL and GND defines the linear regulator current limit threshold by the equation: Imax(typ.)=10000/ RSEL. |
| 30 | 2 | VCTRL | Output voltage control | 13V-18V linear regulator $V_{oRX}$ switch control. To be used only with $V_{SEL}$=1. If VCTRL=1 or floating $V_{oRX}$=18.5V (or 19.5V if LLC=1). If VCTRL=0 than $V_{oRX}$=13.4V (LLC=either 0 or 1). Leave floating if not used. Do not connect to ground if not used. |
| 5 | 7 | P-GND | Power ground | DC-DC converter power ground. |
| Epad | Epad | Epad | Exposed pad | To be connected with power grounds and to the ground layer through vias to dissipate the heat. |
| 20 | 18 | A-GND | Analog ground | Analog circuits ground. |
| 1, 2, 3, 7, 8, 16, 17, 23, 24, 25, 26, 31, 32 | 3, 4, 5, 21, 24 | N.C. | Not connected | Not internally connected pins. |

# 4 Maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC-L}$, $V_{CC}$ | DC power supply input voltage pins | -0.3 to 16 | V |
| $V_{UP}$ | DC input voltage | -0.3 to 24 | V |
| $I_O$ | Output current | Internally Limited | mA |
| $V_{oRX}$ | DC output pin voltage | -0.3 to 25 | V |
| $V_{oTX}$ | Tone output pin voltage | -0.3 to 25 | V |
| $V_I$ | Logic input voltage (TTX, SDA, SCL, DSQIN, EXTM, VCTRL, ADDR) | -0.3 to 7 | V |
| LX | LX input voltage | -0.3 to 24 | V |
| $V_{DETIN}$ | Detector input signal amplitude | 2 | $V_{PP}$ |
| $V_{OH}$ | Logic high output voltage (DSQOUT) | -0.3 to 7 | V |
| $V_{BYP}$ | Internal reference pin voltage (*Note 2*) | -0.3 to 4.6 | V |
| ISEL | Current selection pin voltage | -0.3 to 4.6 | V |
| $T_{STG}$ | Storage temperature range | -50 to 150 | °C |
| $T_J$ | Operating junction temperature range | -25 to 125 | °C |
| ESD | ESD rating with human body model (HBM) for all pins unless 6, 19, 20 (for PSSO24) and unless 4, 21, 22 (for QFN32) | 2 | kV |
| | ESD rating with human body model (HBM) for pins 19, 20 (for PSSO24) and pins 21, 22 (for QFN32) | 4 | |
| | ESD rating with human body model (HBM) for pin 6 (for PSSO24) and pin 4 (for QFN32) | 0.6 | |

*Note: 1 Absolute maximum ratings are those values beyond which damage to the device may occur. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to network ground terminal.*

*2 The BYP pin is intended only to connect an external ceramic capacitor. Any connection of this pin to external current or voltage sources may cause permanent damage to the device.*

**Table 4. Thermal data**

| Symbol | Parameter | QFN32 | PowerSSO-24 | Unit |
|---|---|---|---|---|
| $R_{thJC}$ | Thermal resistance junction-case | 2 | 2 | °C/W |
| $R_{thJA}$ | Thermal resistance junction-ambient (PowerSSO-24) with device soldered on 2s2p PC Board | 35 | 30 | °C/W |

# 5 Application circuit

**Figure 4. Typical application circuit**

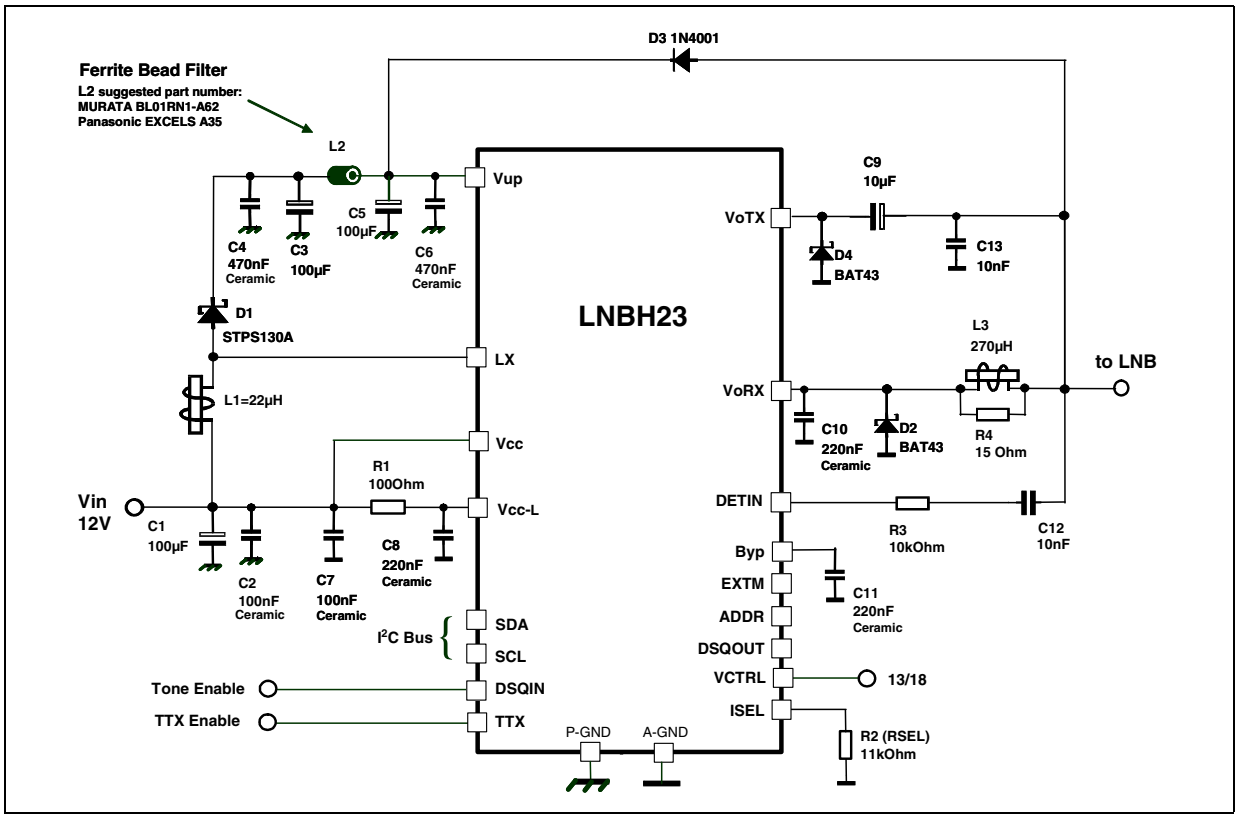



**Table 5. Bill of material**

| Component | Notes |
|---|---|
| R1, R4 | 1/4W resistors. Refer to the typical application circuit for the relative values |
| R2 (RSEL), R3 | 1/4W resistors. Refer to the typical application circuit for the relative values |
| C1 | 25V electrolytic capacitor, 100µF or higher is suitable. |
| C9 | 10µF, >35V electrolytic capacitor |
| C3, C5 | 100µF, >25V electrolytic capacitor, ESR in the 150mΩ to 350mΩ range |
| C2, C4, C6, C7, C8, C10, C11, C12, C13 | >25V ceramic capacitors. Refer to the typ. appl. circuit for the relative values |
| D1 | STPS130A or any similar schottky diode with $V_{RRM}$>25V and $I_{F(AV)}$ higher than: $I_{F(AV)} > I_{OUT_MAX} \times (V_{UP_MAX}/V_{IN_MIN})$ |
| D2, D4 | BAT43, 1N5818, or any schottky diode with $I_{F(AV)} > 0.2A$, $V_{RRM} > 25$ V, $V_F < 0.5$ V |
| D3 | 1N4001 or equivalent |
| L1 | 22 µH Inductor with $I_{sat}>I_{peak}$ where $I_{peak}$ is the boost converter peak current (see *Equation 1*) |

**Table 5. Bill of material (continued)**

| Component | Notes |
|---|---|
| L2 | FERRITE BEAD, Panasonic-EXCELS A35 or Murata-BL01RN1-A62 or Taiyo-Yuden-BKP1608HS600 or equivalent with similar or higher impedance and current rating higher than 2A |
| L3 | 220µH-270µH Inductor with current rating higher than rated output current |

To calculate the boost converter peak current ($I_{PEAK}$) of L1, use the following formula:

**Equation 1**

$$I_{PEAK} = \frac{V_{UP_MAX} * I_{OUT_MAX}}{Eff * V_{IN_MIN}} + \frac{V_{IN_MIN}}{2LF}\left(1 - \frac{V_{IN_MIN}}{V_{UP_MAX}}\right)$$

# 6 I²C bus interface

Data transmission from main MCU to the LNBH23 and vice versa takes place through the 2 wires I²C bus Interface, consisting of the 2 lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

## 6.1 Data validity

As shown in *Figure 5*, the data on the SDA line must be stable during the high semi-period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

## 6.2 Start and stop condition

As shown in *Figure 6* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

## 6.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

## 6.4 Acknowledge

The master (MCU) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 7*). The peripheral (LNBH23) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed has to generate acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBH23 won't generate acknowledge if the $V_{CC}$ supply is below the under voltage lockout threshold (6.7 V typ.).

## 6.5 Transmission without acknowledge

Avoiding to detect the acknowledges of the LNBH23, the MCU can use a simpler transmission: simply it waits one clock cycle without checking the slave acknowledging, and sends the new data. This approach of course is less protected from misworking and decreases the noise immunity.

**Figure 5. Data validity on the I²C bus**

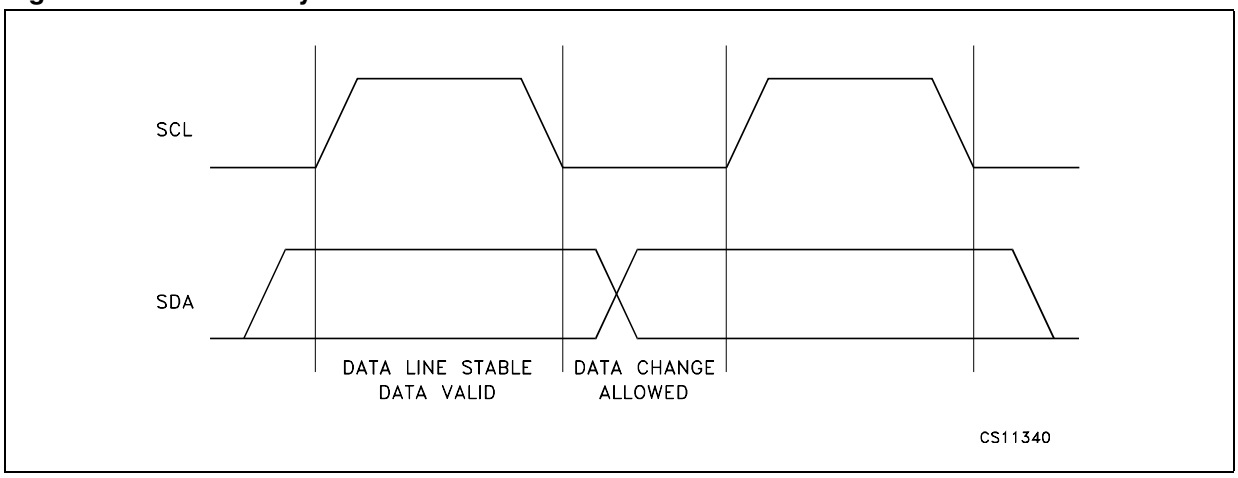



**Figure 6. Timing diagram of I²C bus**

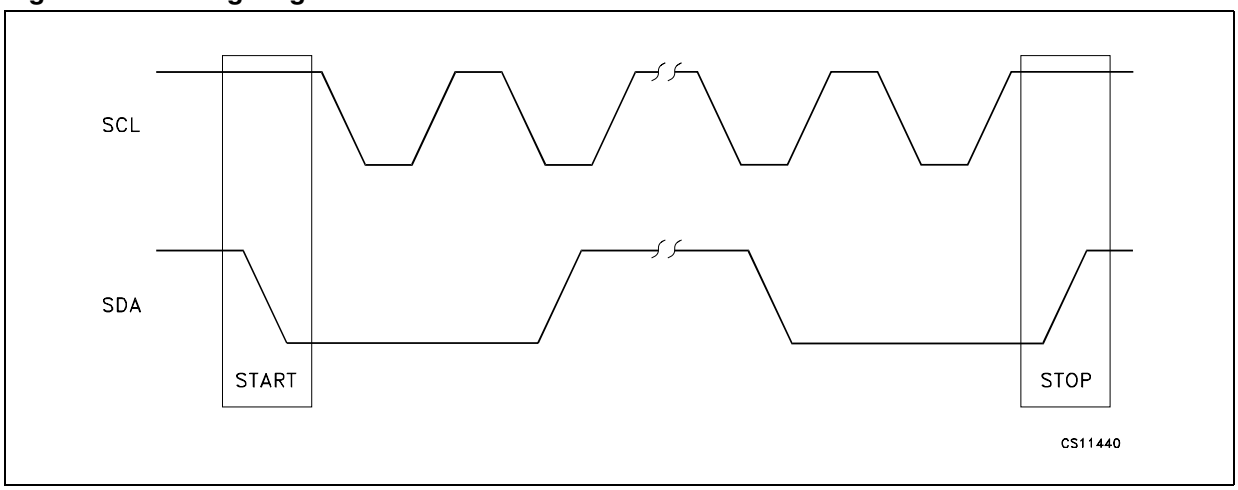
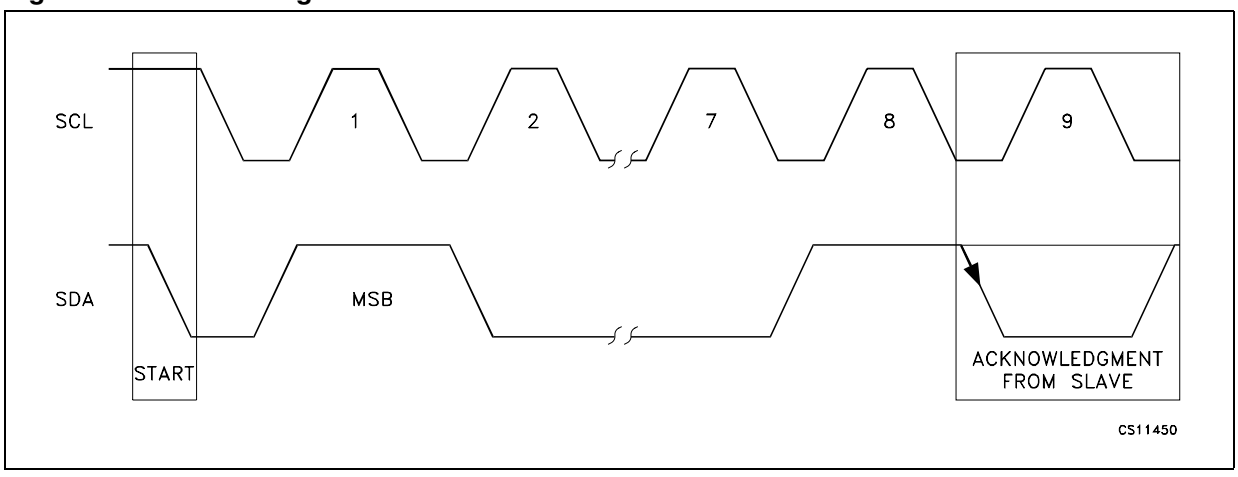



**Figure 7. Acknowledge on the I²C bus**



# 7 LNBH23 software description

## 7.1 Interface protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte (the LSB bit determines read(=1)/write(=0) transmission)
- A sequence of data (1 byte + acknowledge)
- A stop condition (P)

| | Chip address | | | | | | | | | Data | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MSB | | | | | | | LSB | | MSB | | | | | | | LSB | | |
| S | 0 | 0 | 0 | 1 | 0 | 1 | X | R/W | ACK | | | | | | | | | ACK | P |

ACK = Acknowledge

S = Start

P = Stop

R/W = 1/0, Read/Write bit

X = 0/1, two selectable addresses available through ADDR pin (see Address pin characteristics *Table 10*)

## 7.2 System register (SR, 1 byte)

| Mode | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| **Write** | PCL | TTX | TEN | LLC | VSEL | EN | ITEST | AUX |
| **Read** | IMON | VMON | TMON | LLC | VSEL | EN | OTF | OLF |

Write = control bits functions in write mode

Read= diagnostic bits in read mode.

All bits reset to 0 at power On

## 7.3 Transmitted data (I²C bus write mode)

When the R/W bit in the chip address is set to 0, the main MCU can write on the system register (SR) of the LNBH23 via I²C bus. All and 8 bits are available and can be written by the MCU to control the device functions as per the below truth table.

**Table 6. Truth table**

| PCL | TTX | TEN | LLC | VSEL | EN | ITEST | AUX | Function |
|---|---|---|---|---|---|---|---|---|
| | 0 | | 0 | 0 | 1 | | 0 | $V_{oRX}$= 13.4V, $V_{UP}$=14.15V, ($V_{UP}$-$V_{oRX}$=0.75V) |
| | 0 | | 0 | 1 | 1 | | 0 | $V_{oRX}$= 18.5V, $V_{UP}$=19.25V, ($V_{UP}$-$V_{oRX}$=0.75V) |
| | 0 | | 1 | 0 | 1 | | 0 | $V_{oRX}$= 14.4V, $V_{UP}$=15.15V, ($V_{UP}$-$V_{oRX}$=0.75V) |
| | 0 | | 1 | 1 | 1 | | 0 | $V_{oRX}$= 19.5V, $V_{UP}$=20.25V, ($V_{UP}$-$V_{oRX}$=0.75V) |
| | | | X | X | 1 | X | 1 | $V_{oRX}$= 22V, $V_{UP}$=22.75V, ($V_{UP}$-$V_{oRX}$=0.75V) |
| | | 0 | | | 1 | | | 22 kHz controlled by DSQIN pin (only if TTX=1) |
| | 1 | 1 | | | 1 | | | 22 kHz tone output is always activated |
| | 0 | | | | 1 | | | $V_{oRX}$ output is ON, $V_{oTX}$ Tone generator output is OFF |
| | 1 | | | | 1 | | | $V_{oRX}$ output is ON, $V_{oTX}$ Tone generator output is ON |
| 0 | | | | | 1 | | | Pulsed (Dynamic) current limiting is selected |
| 1 | | | | | 1 | | | Static current limiting is selected |
| | | | X | X | 1 | 0 | | Minimum output current diagnostic threshold = 6mA typ. |
| | | | X | X | 1 | 1 | | Minimum output current diagnostic threshold = 12mA typ. |
| X | X | X | X | X | 0 | X | X | Power block disabled |

X = don't care
All values are typical unless otherwise specified
Valid with TTX pin floating or to GND

## 7.4 Diagnostic received data (I²C read mode)

LNBH23 can provide to the MCU Master a copy of the diagnostic system register information via I²C bus in read mode. The read mode is master activated by sending the chip address with R/W bit set to 1. At the following master generated clocks bits, LNBH23 issues a byte on the SDA data bus line (MSB transmitted first). At the ninth clock bit the master can:

- Acknowledge the reception, starting in this way the transmission of another byte from the LNBH23
- No acknowledge, stopping the read mode communication

Three bits of the register are read back as a copy of the corresponding write output voltage register status (LLC, VSEL, EN), while, the other five bits convey diagnostic information about the over-temperature (OTF), output voltage level (VMON), output over-load (OLF), Minimum output current presence (IMON) and 22 kHz tone (TMON). In normal operation the diagnostic bits are set to zero, while, if a failure is occurring, the corresponding bit is set to one. At start-up all the bits are reset to zero.

**Table 7. Register**

| IMON | VMON | TMON | LLC | VSEL | EN | OTF | OLF | Function |
|---|---|---|---|---|---|---|---|---|
| | | | These bits are read exactly the same as they were left after last write operation | | | 0 | | $T_J$ < 135°C, normal operation (1) |
| | | | | | | 1 | | $T_J$ > 150°C, power blocks disabled (1) |
| | | | | | | | 0 | $I_O$ < $I_{OMAX}$, normal operation |
| | | | | | | | 1 | $I_O$ > $I_{OMAX}$, Overload Protection triggered |
| 0/1 (2) | 0/1 (3) | 0/1 | | | | | | These bits are set to 1 if the relative parameter is out of the specification limits. |

1. Values are typical unless otherwise specified
2. IMON information must be disregarded if 22 kHz TONE output is enabled
3. VMON information must be disregarded if LLC=1 (valid only if LLC=0)

## 7.5 Power-on I²C interface reset

I²C interface built in LNBH23 is automatically reset at power-on. As long as the $V_{CC}$ stays below the under voltage lockout (UVL) threshold (6.7 V), the interface does not respond to any I²C command and the system register (SR) is initialized to all zeroes, thus keeping the power blocks disabled. Once the $V_{CC}$ rises above 7.3 V typ. The I²C interface becomes operative and the SR can be configured by the main MCU. This is due to 500 mV of hysteresis provided in the UVL threshold to avoid false retriggering of the power-on reset circuit.

## 7.6 Address pin

It is possible to select two I²C interface addresses by means of ADDR pin. This pin is TTL compatible and can be set as per hereafter address pin characteristics *Table 10*.

## 7.7 DiSEqC™ implementation

LNBH23 helps system designer to implement bi-directional DiSEqC 2.0 protocol by allowing an easy PWK modulation/demodulation of the 22 kHz carrier. Between the LNBH23 and the main MCU the PWK data is exchanged using logic levels that are compatible with both 3.3 V and 5 V MCU. This data exchange is made through two dedicated pins, DSQIN and DSQOUT, in order to maintain the timing relationships between the PWK data and the PWK modulation as accurate as possible. These two pins should be directly connected to two I/O pins of the MCU, thus leaving to the firmware the task of encoding and decoding the PWK data in accordance to the DiSEqC protocol.
Full compliance of the system to the specification is thus not implied by the bare use of the LNBH23. The system designer should also take in consideration the bus hardware requirements; that can be simply accomplished by the R-L termination connected between $V_{oRX}$ and $V_{oTX}$ pins of LNBH23, as shown in the typical application circuit in *Figure 4*. To avoid any losses due to the R-L impedance during the tone transmission, LNBH23 has dedicated Tone output ($V_{oTX}$) that is connected after the filter and must be enabled by setting the TTX function to HIGH only during the tone transmission (see DiSEqC 2.0 operation implementation in section *2.2* and *2.3*). Also unidirectional DiSEqC 1.x and non-DiSEqC systems need this termination connected through a bypass capacitor and after a R-L filter with 15 Ω in parallel with a 220 µH-270 µH inductor but, there is no need of tone decoding, thus DETIN and DSQOUT pins can be left connected to GND.

# 8 Electrical characteristics

Refer to the typical application circuit, $T_J$ = 0 to 85 °C, EN=1, VSEL=LLC=TEN=PCL=ITEST=TTX=AUX=0, $R_{SEL}$ = 11 kΩ, DSQIN = LOW, $V_I$ = 12 V, $I_O$ = 50 mA, unless otherwise stated. Typical values are referred to $T_J$ = 25 °C. $V_O$ = $V_{oRX}$ pin voltage. See software description section for I²C access to the system register.

**Table 8. Electrical characteristics**

| Symbol | Parameter | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_I$ | Supply voltage | $I_O$=750mA, VSEL=LLC=1 | | 8 | 12 | 15 | V |
| $I_I$ | Supply current | $I_O$=0 | | | 7 | 15 | mA |
| | | EN=TEN=TTX=1, $I_O$=0 | | | 20 | 40 | |
| | | EN=0 | | | 2 | | |
| $V_O$ | Output voltage | AUX=1; $I_O$=50mA | | | 22 | | V |
| | | $V_{SEL}$=1 $I_O$=750mA | LLC=0 | 17.8 | 18.5 | 19.2 | |
| | | | LLC=1 | 18.8 | 19.5 | 20.2 | |
| | | $V_{SEL}$=0 $I_O$=750mA | LLC=0 | 12.8 | 13.4 | 14 | |
| | | | LLC=1 | 13.8 | 14.4 | 15 | |
| $V_O$ | Line regulation | $V_I$=8 to 15V | VSEL=0 | | 5 | 40 | mV |
| | | | VSEL=1 | | 5 | 60 | |
| $V_O$ | Load regulation | $V_{SEL}$=0 or 1, $I_O$ from 50 to750mA | | | | 200 | mV |
| 13/18 $T_R$ - $T_F$ | 13/18V Rise and Fall transition time by $V_{CTRL}$ pin | $V_{SEL}$=LLC=1, $V_{CTRL}$ from LOW to HIGH and vice versa, $I_O$ from 6 to 450mA, $C_O$ from 10 to 330nF | | | 575 | | µs |
| $I_{MAX}$ | Output current limiting | $R_{SEL}$=11kΩ | | 750 | | 1000 | mA |
| | | $R_{SEL}$= 22kΩ | | 300 | | 600 | |
| $I_{SC}$ | Output short circuit current | $V_{SEL}$=0/1, AUX=0/1 | | | 1000 | | mA |
| $T_{OFF}$ | Dynamic overload protection OFF time | PCL=0, Output shorted | | | 900 | | ms |
| $T_{ON}$ | Dynamic overload protection ON time | PCL=0, Output shorted | | | $T_{OFF}$/10 | | |
| $F_{TONE}$ | Tone frequency | DSQIN=HIGH or TEN=1, TTX=1 | | 20 | 22 | 24 | kHz |
| $A_{TONE}$ | Tone amplitude | DSQIN=HIGH or TEN=1, TTX=1<br>$I_O$ from 0 to750mA<br>$C_O$ from 0 to 750nF | | 0.4 | 0.650 | 0.9 | $V_{PP}$ |
| $D_{TONE}$ | Tone duty cycle | DSQIN=HIGH or TEN=1, TTX=1 | | 43 | 50 | 57 | % |
| $t_r$, $t_f$ | Tone rise or fall time | DSQIN=HIGH or TEN=1, TTX=1 | | 5 | 8 | 15 | µs |
| $F_{EXTM}$ | EXTM frequency | $V_{EXTM-H}$ =3.3V, $V_{EXTM-L}$ =0V, (1) | | 20 | 22 | 24 | kHz |
| $Eff_{DC-DC}$ | DC-DC converter efficiency | $I_O$=750mA | | | 93 | | % |
| $F_{SW}$ | DC-DC converter switching freq. | | | | 220 | | kHz |
| $F_{DETIN}$ | Tone detector freq. capture range | 0.4$V_{PP}$ sine wave(2) | | 19 | 22 | 25 | kHz |

**Table 8. Electrical characteristics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DETIN}$ | Tone detector input amplitude | Sine wave signal, 22 kHz | 0.3 | | 1.5 | $V_{PP}$ |
| $Z_{DETIN}$ | Tone detector input impedance | | | 150 | | kΩ |
| $V_{OL}$ | DSQOUT pin logic LOW | DETIN Tone present, $I_{OL}$=2mA | | 0.3 | 0.5 | V |
| $I_{OZ}$ | DSQOUT pin leakage current | DETIN Tone absent, $V_{OH}$=6V | | | 10 | µA |
| $V_{IL}$ | DSQIN,TTX,13/18, EXTM pin logic Low | | | | 0.8 | V |
| $V_{IH}$ | DSQIN,TTX,13/18, EXTM pin logic High | | 2 | | | V |
| $I_{IH}$ | DSQIN,TTX,13/18, EXTM pin input current | $V_{IH}$=5V | | 15 | | µA |
| $I_{OBK}$ | Output backward current | EN=0, $V_{OBK}$=21V | | -6 | -15 | mA |
| $T_{SHDN}$ | Thermal shut-down threshold | | | 150 | | °C |
| $\Delta T_{SHDN}$ | Thermal shut-down hysteresis | | | 15 | | °C |

1. External signal frequency range in which the EXTM function is guaranteed.
2. Frequency range in which the DETIN function is guaranteed. The $V_{PP}$ level is intended on the LNB bus (before the C12 capacitor. See *Figure 4*)

$T_J$ from 0 to 85 °C, $V_I$ = 12 V

**Table 9. I²C electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | LOW Level input voltage | SDA, SCL | | | 0.8 | V |
| $V_{IH}$ | HIGH Level input voltage | SDA, SCL | 2 | | | V |
| $I_I$ | Input current | SDA, SCL, $V_I$ = 0.4 to 4.5V | -10 | | 10 | µA |
| $V_{OL}$ | Low level output voltage | SDA (open drain), $I_{OL}$ = 6mA | | | 0.6 | V |
| $f_{MAX}$ | Maximum clock frequency | SCL | | | 400 | kHz |

$T_J$ from 0 to 85 °C, $V_I$ = 12 V

**Table 10. Address pin characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{ADDR-1}$ | "0001010(R/W)" Address pin voltage range | R/W bit determines the transmission mode: read (R/W=1) write (R/W=0) | 0 | | 0.8 | V |
| $V_{ADDR-2}$ | "0001011(RW)" Address pin voltage range | R/W bit determines the transmission mode: read (R/W=1) write (R/W=0) | 2 | | 5 | V |
| $V_{ADDR-3}$ (1) | "0001000(RW)" Address pin voltage range | R/W bit determines the transmission mode: read (R/W=1) write (R/W=0) | 0 | | 5 | V |

1. This I²C address is reserved only for internal usage. Do not use this address with other I²C peripherals to avoid address conflicts.

Refer to the typical application circuit, $T_J$ from 0 to 85 °C, EN=1, VSEL=LLC=TEN=PCL=ITEST=TTX=AUX=0, $R_{SEL}$=11 kΩ, DSQIN=LOW, $V_I$ = 12 V, $I_O$ = 50 mA, unless otherwise stated. Typical values are referred to $T_J$ = 25 °C. $V_O$=$V_{oRX}$ pin voltage. See software description section for I²C access to the system register.

**Table 11. Output voltage diagnostic (VMON bit) characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{TH-L}$ | Diagnostic low threshold at $V_O$=13.4V | EN=1, VSEL=0 LLC=0 | 85 | 90 | 95 | % |
| $V_{TH-L}$ | Diagnostic low threshold at $V_O$=18.5V | EN=VSEL=1 LLC=0 | 84 | 90 | 96 | % |

*Note: If the output voltage is lower than the min. value the VMON I²C bit is set to 1.*

*When VSEL=0: If VMON=0 then $V_{oRX}$>85% of $V_{oRX}$ typical; If VMON=1 then $V_{oRX}$<95% of $V_{oRX}$ typical.*

*When VSEL=1: If VMON=0 then $V_{oRX}$>84% of $V_{oRX}$ typical; If VMON=1 then $V_{oRX}$<96% of $V_{oRX}$ typical.*

$T_J$ from 0 to 85 °C, EN = 1, VSEL=LLC=TEN=PCL=TTX=0, DSQIN=LOW, $V_I$ = 12 V, unless otherwise stated. See software description section for I²C access to the system register.

**Table 12. Minimum output current diagnostic (IMON bit) characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{TH}$ | Minimum current diagnostic threshold | ITEST=1, AUX=0/1 | 5 | 12 | 20 | mA |
| | | ITEST=0, AUX=0/1 | 2.5 | 6 | 10 | |

*Note: If the output current is lower than the min. threshold limit the IMON I²C bit is set to 1. if the output current is higher than the max threshold limit the IMON I²C bit is set to 0.*

Refer to the typical application circuit, $T_J$ from 0 to 85 °C, EN = 1, VSEL=LLC=TEN=PCL=ITEST=TTX=AUX=0, $R_{SEL}$ = 11 KΩ, DSQIN=LOW, $V_I$ = 12 V, $I_O$ = 50 mA, unless otherwise stated. Typical values are referred to $T_J$=25°C. $V_{oRX}$=$V_{oRX}$ pin voltage. See software description section for I²C access to the system register.

**Table 13. 22 kHz tone diagnostic (TMON bit) characteristics**

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $A_{TH-L}$ | Amplitude diagnostic low threshold | DETIN pin AC coupled | 200 | 300 | 400 | mV |
| $A_{TH-H}$ | Amplitude diagnostic high threshold | DETIN pin AC coupled | 900 | 1100 | 1200 | mV |
| $F_{TH-L}$ | Frequency diagnostic low thresholds | DETIN pin AC coupled | 13 | 16.5 | 20 | kHz |
| $F_{TH-H}$ | Frequency diagnostic high thresholds | DETIN pin AC coupled | 24 | 29.5 | 38 | kHz |

*Note: If the 22 kHz tone parameters are lower or higher than the above limits the TMON I²C bit is set to 1.*

# 9 Typical performance characteristics

(Refer to the typical application circuit, $T_J$ from 0 to 85 °C, EN = 1, VSEL=LLC=TEN=PCL=ITEST=TTX=AUX=0, $R_{SEL}$ = 11 kΩ, DSQIN=LOW, $V_I$ = 12 V, $I_O$ = 50 mA, unless otherwise stated. Typical values are referred to $T_J$ = 25 °C. $V_O$=$V_{oRX}$ pin voltage. See software description section for I²C access to the system register).

**Figure 8. Output voltage vs. temperature**

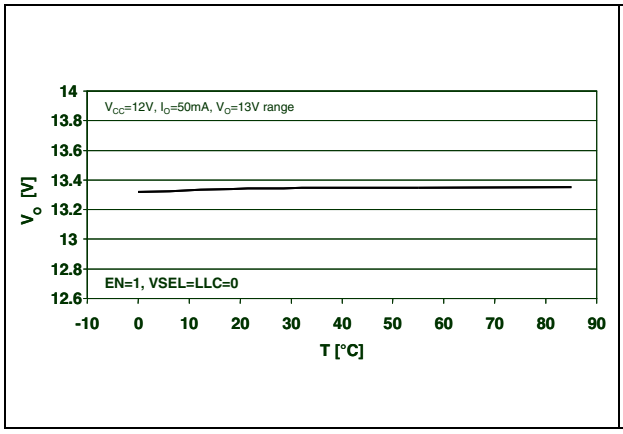



**Figure 9. Output voltage vs. temperature**

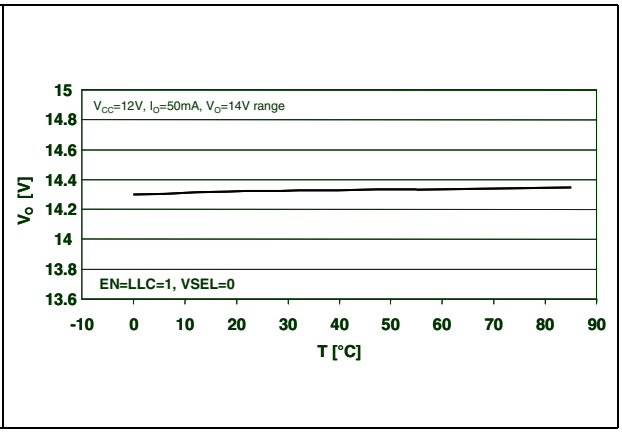



**Figure 10. Output voltage vs. temperature**

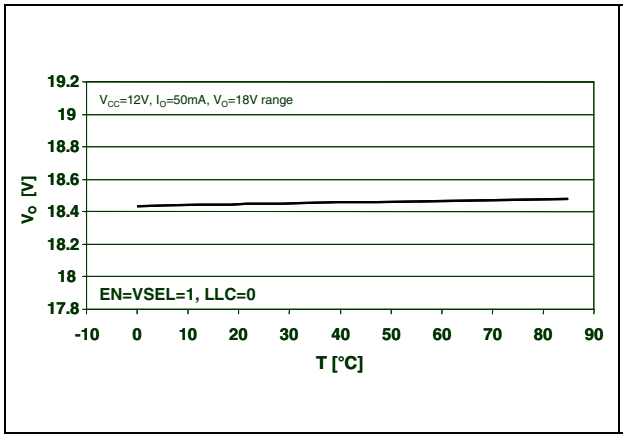



**Figure 11. Output voltage vs. temperature**

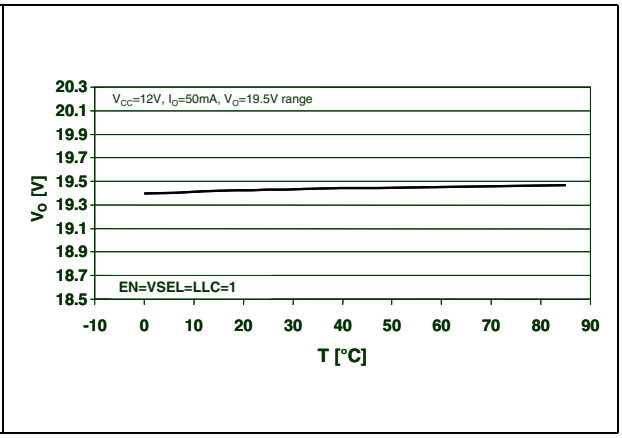



**Figure 12. Load regulation vs. temperature**

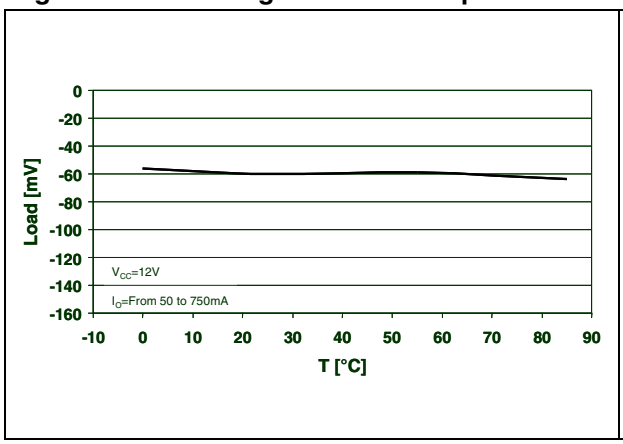



**Figure 13. Supply current vs. temperature**

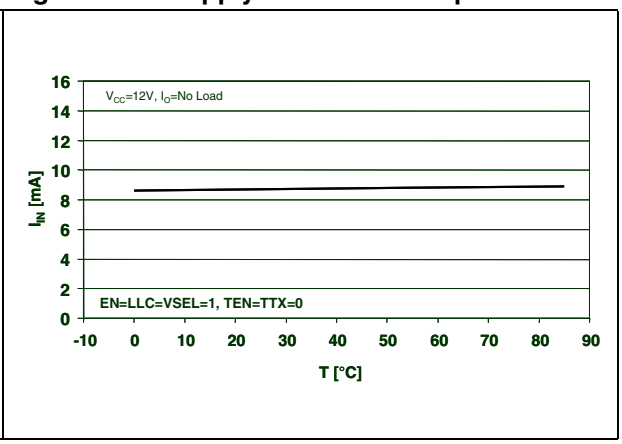


**Figure 14. Supply current vs. temperature**

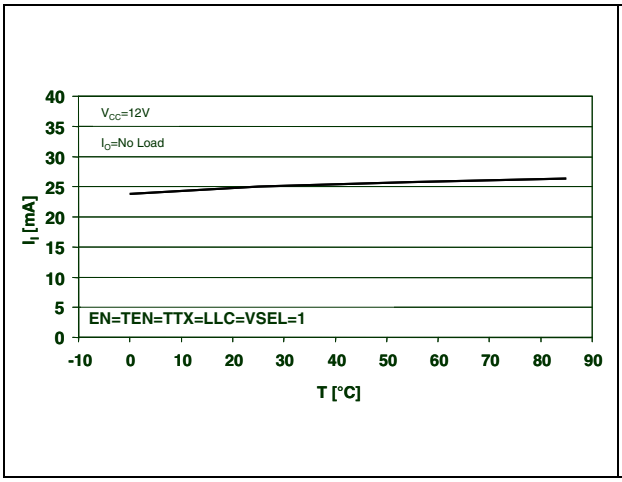



**Figure 15. Dynamic overload protection ON time vs. temperature**

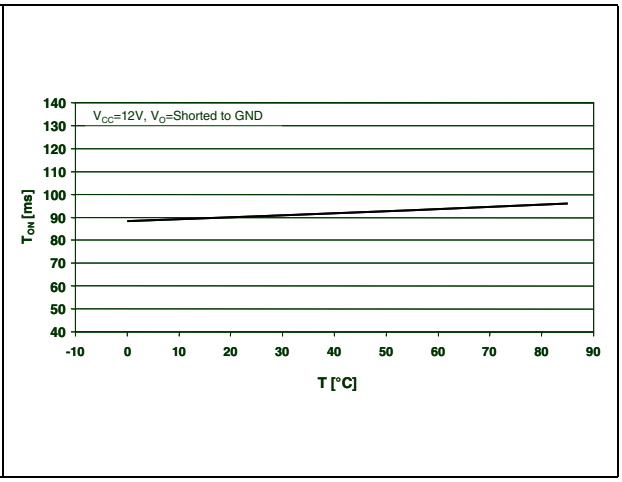



**Figure 16. Dynamic overload protection OFF time vs. temperature**

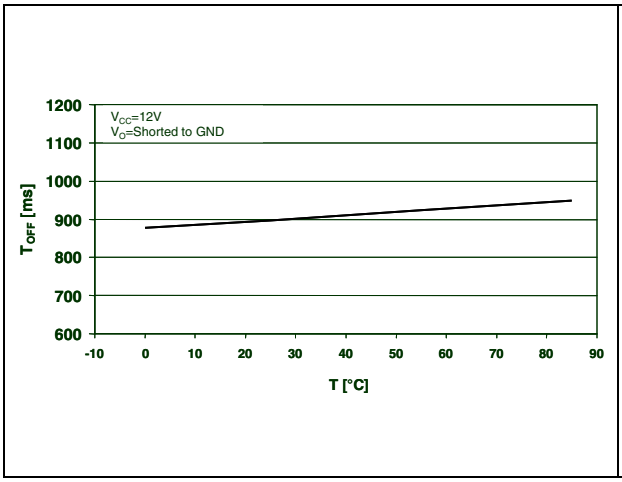



**Figure 17. Output current limiting vs. $R_{SEL}$**

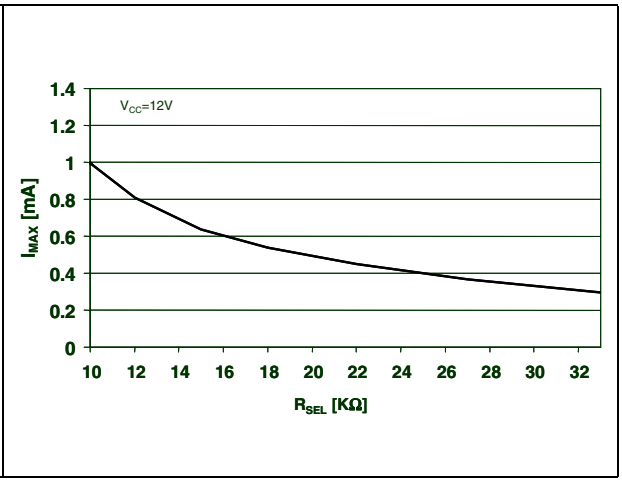



**Figure 18. Output current limiting vs. temperature**

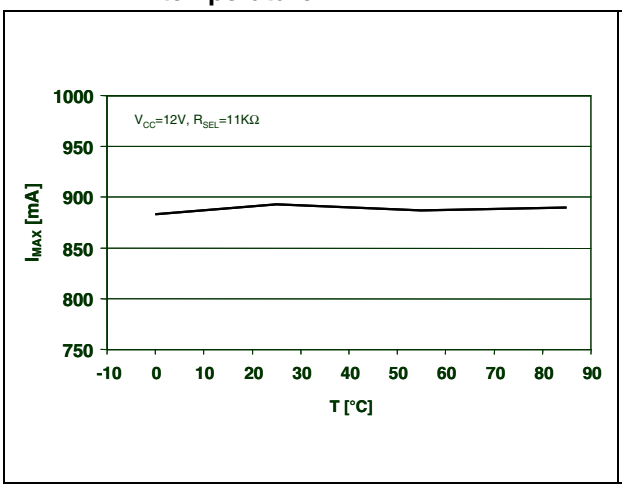



**Figure 19. Output current limiting vs. temperature**

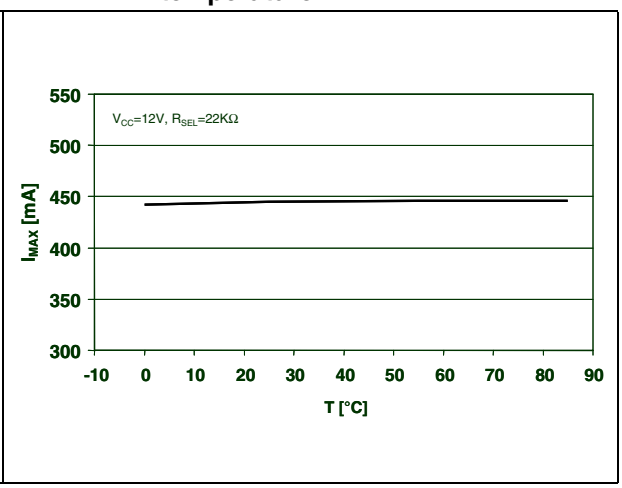


Figure 20. Tone frequency vs. temperature

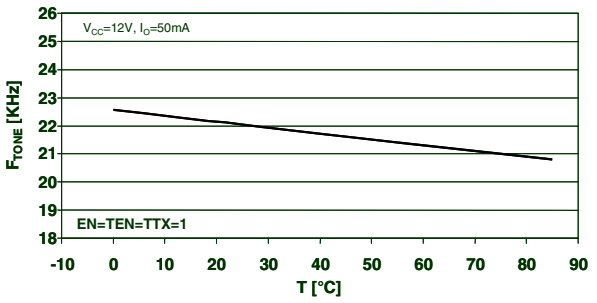



Figure 21. Tone amplitude vs. temperature

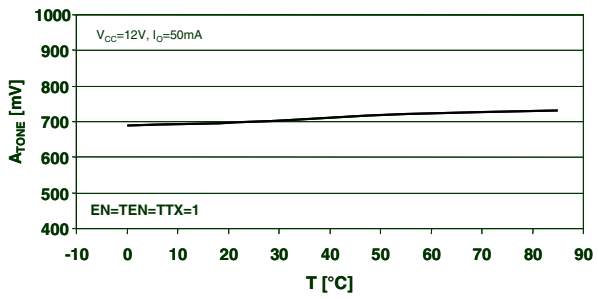



Figure 22. Tone duty cycle vs. temperature

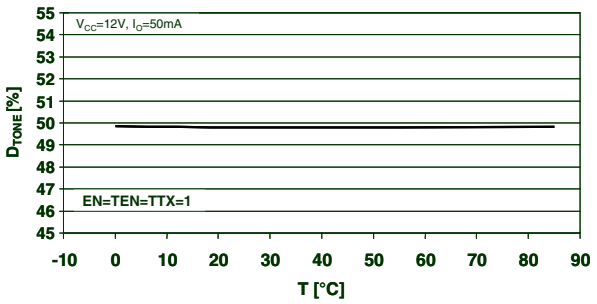



Figure 23. Tone rise time vs. temperature

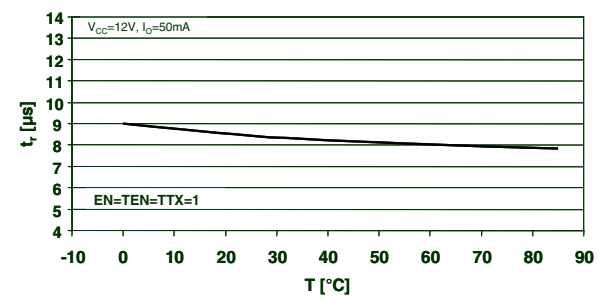



Figure 24. Tone fall time vs. temperature

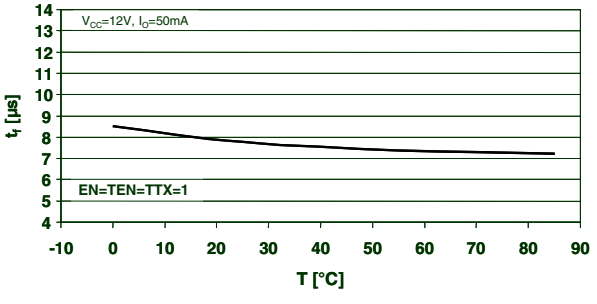



Figure 25. Output backward current vs. temperature

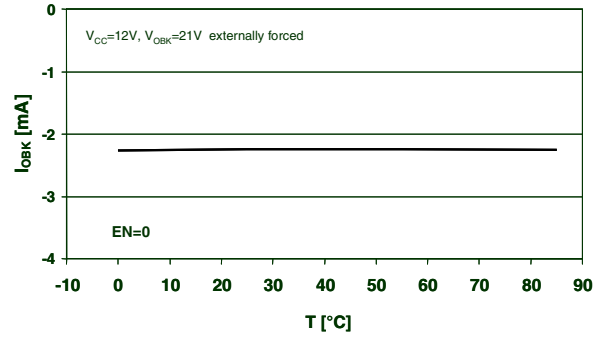


**Figure 26. DC-DC Converter efficiency vs. temperature**

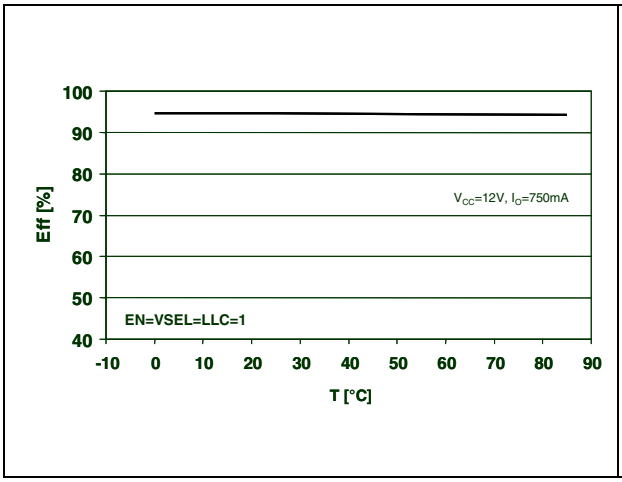



**Figure 27. 22 kHz tone waveform**

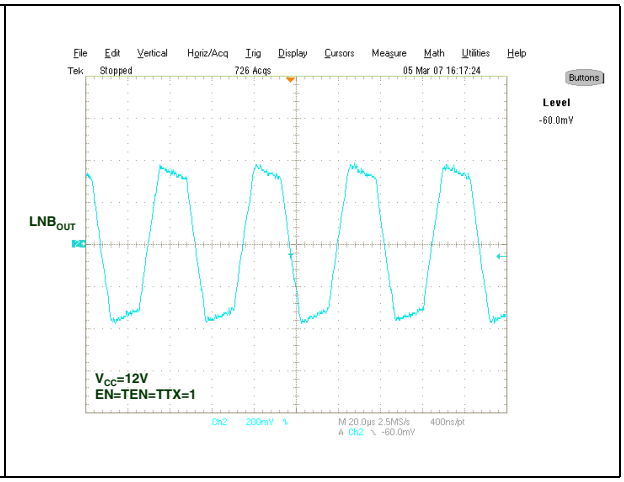



**Figure 28. DSQIN tone enable transient response**

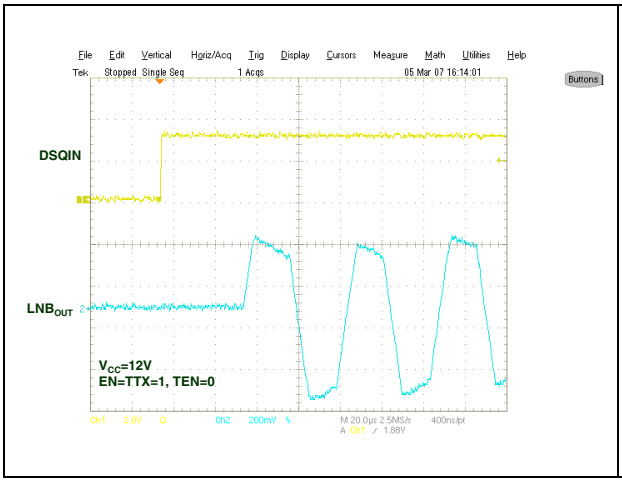
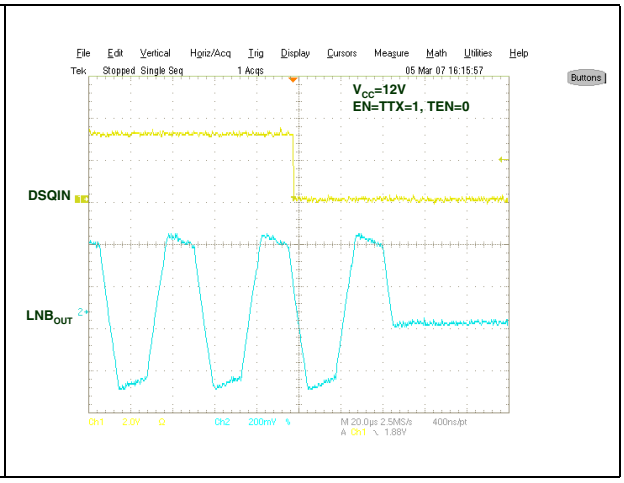



**Figure 29. DSQIN tone disable transient response**



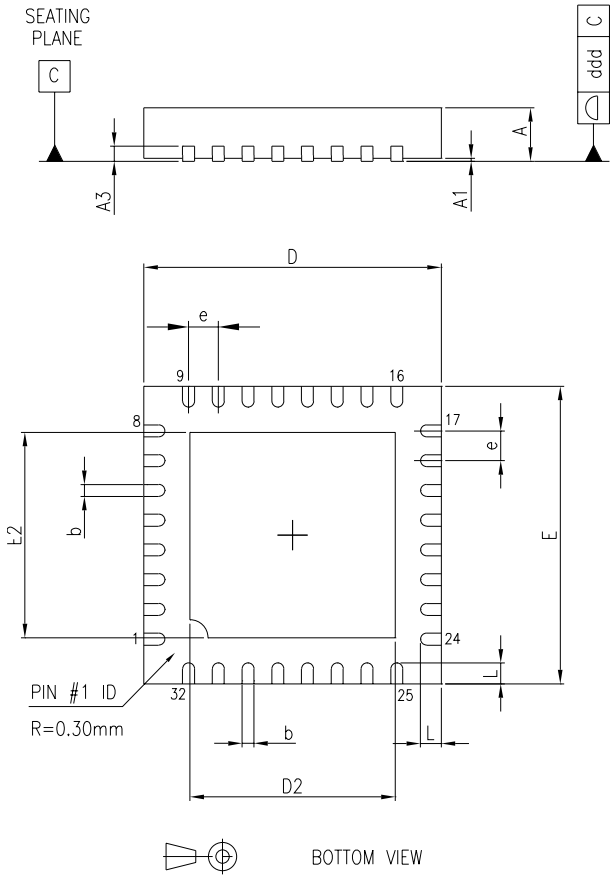
# 10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

**Table 14. QFN32 (5 x 5 mm.) mechanical data**

| Dim. | (mm.) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | | 0.20 | |
| b | 0.18 | 0.25 | 0.30 |
| D | 4.85 | 5.00 | 5.15 |
| D2 | 3.20 | | 3.70 |
| E | 4.85 | 5.00 | 5.15 |
| E2 | 3.20 | | 3.70 |
| e | | 0.50 | |
| L | 0.30 | 0.40 | 0.50 |
| ddd | | | 0.08 |

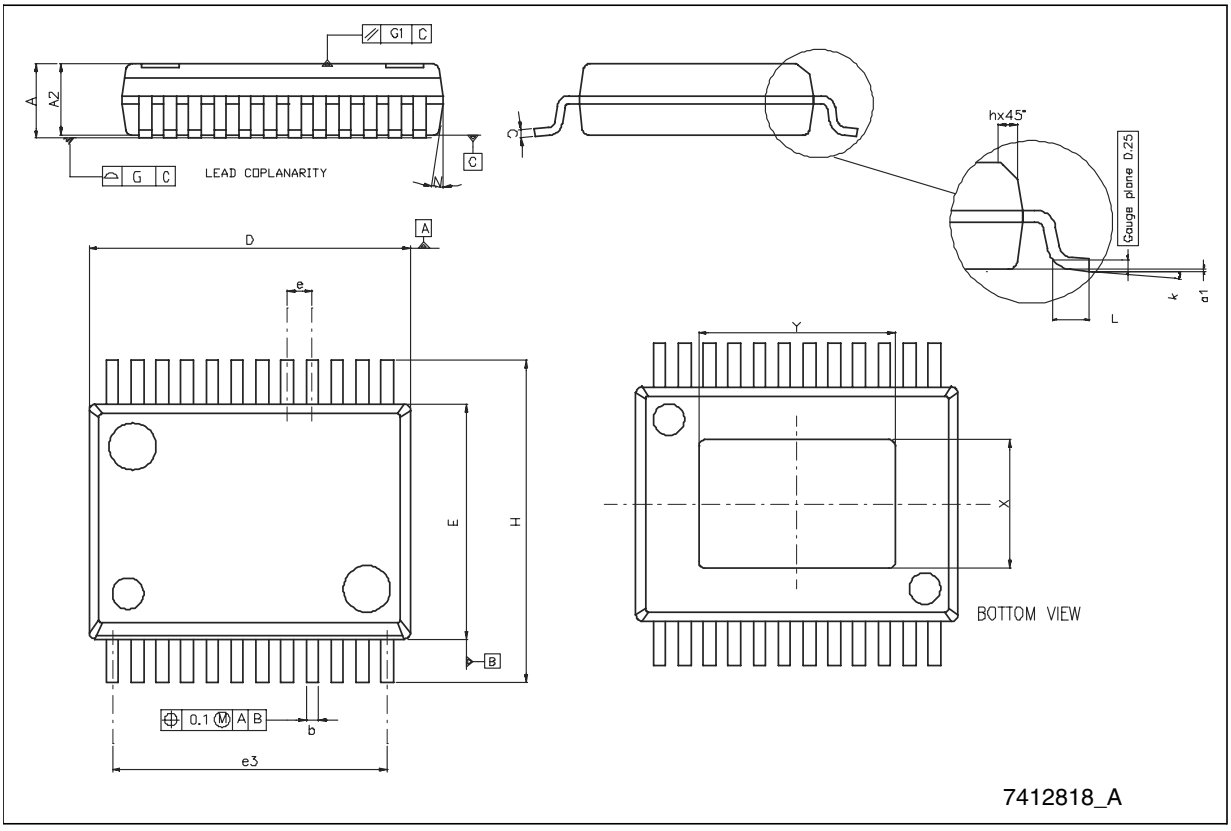
**Figure 30. QFN32 package dimensions**



## PowerSSO-24 mechanical data

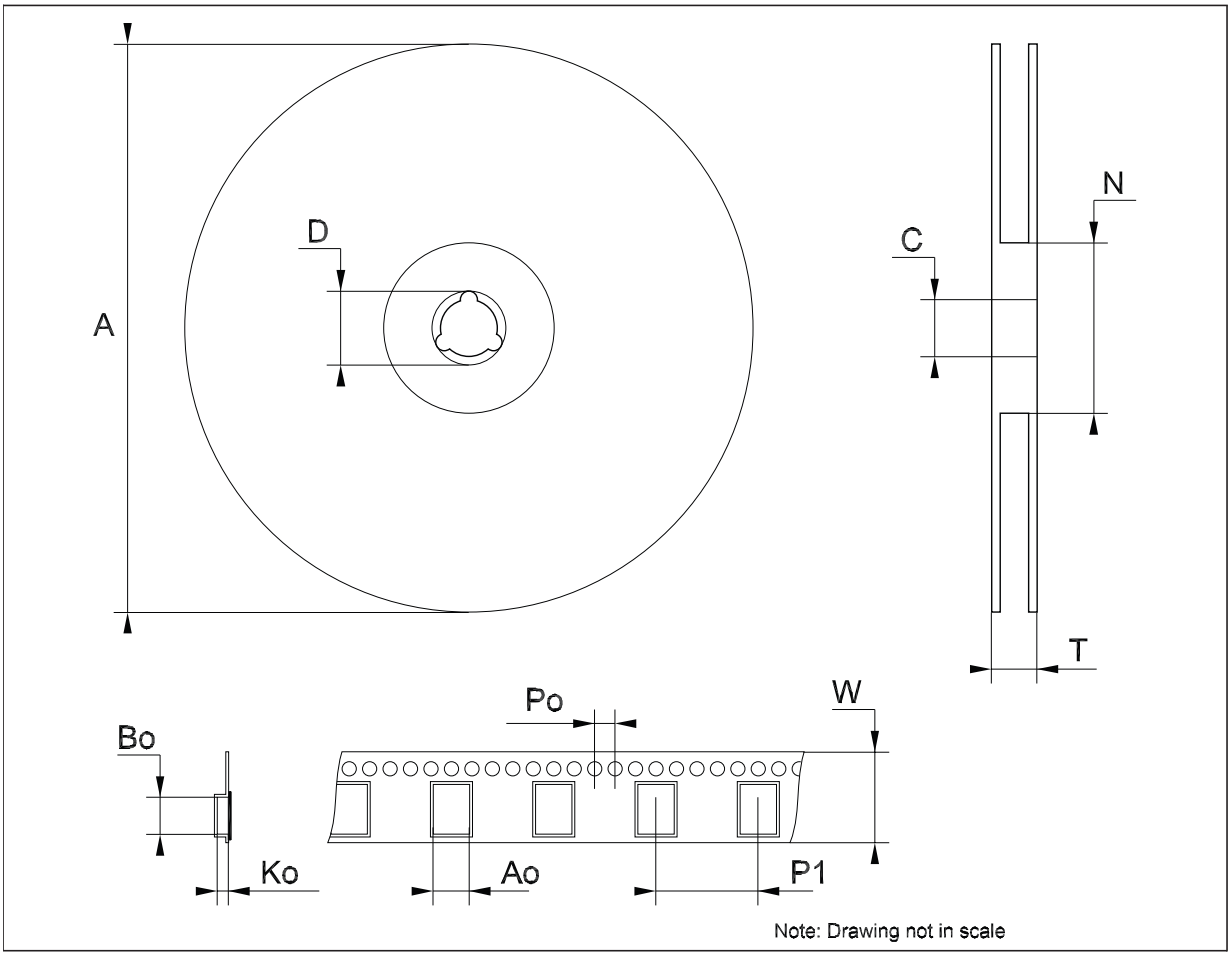
| Dim. | mm. | | | inch. | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 2.15 | | 2.47 | 0.085 | | 0.097 |
| A2 | 2.15 | | 2.40 | 0.085 | | 0.094 |
| a1 | 0 | | 0.075 | 0 | | 0.003 |
| b | 0.33 | | 0.51 | 0.013 | | 0.020 |
| c | 0.23 | | 0.32 | 0.009 | | 0.013 |
| D (1) | 10.10 | | 10.50 | 0.398 | | 0.413 |
| E (1) | 7.4 | | 7.6 | 0.291 | | 0.299 |
| e | | 0.8 | | | 0.031 | |
| e3 | | 8.8 | | | 0.346 | |
| G | | | 0.10 | | | 0.004 |
| G1 | | | 0.06 | | | 0.002 |
| H | 10.10 | | 10.50 | 0.398 | | 0.413 |
| h | | | 0.40 | | | 0.016 |
| L | 0.55 | | 0.85 | 0.022 | | 0.033 |
| N | 10° (max) | | | | | |
| X | 4.10 | | 4.70 | 0.161 | | 0.185 |
| Y | 4.90 | | 5.50 | 0.193 | | 0.217 |

(1) “D and E” do not include mold flash or protusions - Mold flash or protusions shall not exceed 0.15 mm. (0.006”)



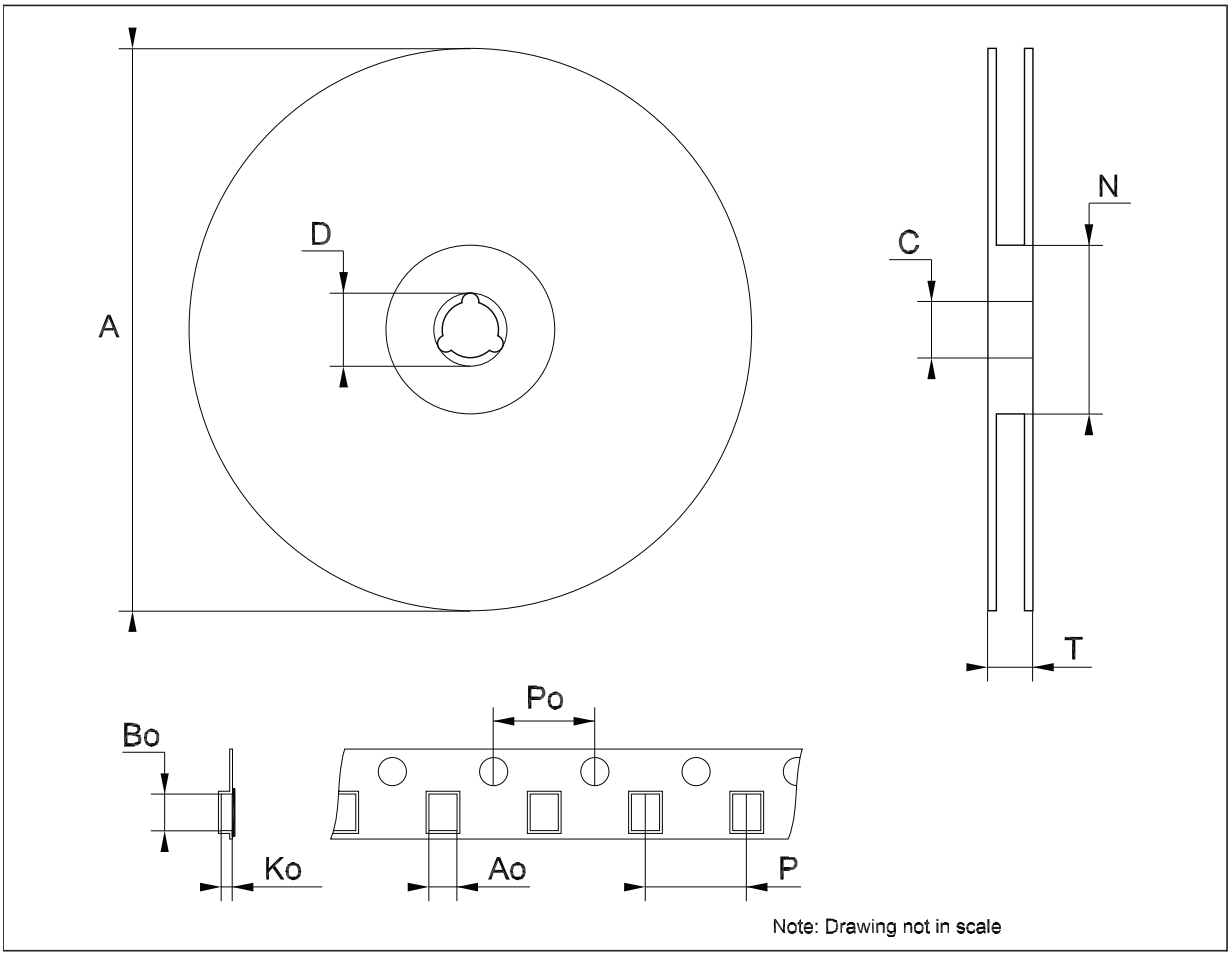
## Tape & reel PowerSSO-24 mechanical data

| Dim. | mm. | | | inch. | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 30.4 | | | 1.197 |
| Ao | 10.8 | | 11.0 | 0.425 | | 0.433 |
| Bo | 10.7 | | 10.9 | 0.421 | | 0.429 |
| Ko | 2.65 | | 2.85 | 0.104 | | 0.112 |
| Po | 3.9 | | 4.1 | 0.154 | | 0.161 |
| $P_1$ | 11.9 | | 12.1 | 0.469 | | 0.476 |
| W | 23.7 | | 24.3 | 0.933 | | 0.957 |



## Tape & reel QFNxx/DFNxx (5x5 mm.) mechanical data

| Dim. | mm. | | | inch. | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 330 | | | 12.992 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 99 | | 101 | 3.898 | | 3.976 |
| T | | | 14.4 | | | 0.567 |
| Ao | | 5.25 | | | 0.207 | |
| Bo | | 5.25 | | | 0.207 | |
| Ko | | 1.1 | | | 0.043 | |
| Po | | 4 | | | 0.157 | |
| P | | 8 | | | 0.315 | |




Note: Drawing not in scale

# 11 Revision history

**Table 15. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 02-Apr-2007 | 1 | Initial release. |
| 15-Nov-2007 | 2 | Added *Note 2* on *Table 3*. |
| 11-Jan-2008 | 3 | Added: new package QFN32 and *Table 5*. |
| 26-Mar-2008 | 4 | Modified: mechanical data for QFN32 *Figure 30 on page 27* and *Table 14 on page 27*. |
| 08-Jan-2009 | 5 | Modified: ESD parameter *Table 3 on page 11*. |
| 23-Mar-2009 | 6 | Modified: Y dimension mechanical data for PowerSSO-24 *on page 28*. |
| 29-Nov-2010 | 7 | Modified: *Table 10 on page 20*. |
| 01-Feb-2013 | 8 | Modified: Maximum clock frequency Max. value *Table 9 on page 20*. |

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