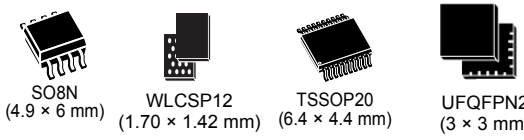
STM32C011x4/x6

Arm®Cortex®-M0+ 32-bit MCU, 32 KB flash, 6 KB RAM, 2 x USART, timers, ADC, comm. I/Fs, 2-3.6 V

Datasheet - production data

Features

- Includes ST state-of-the-art patented technology
- Core: Arm® 32-bit Cortex®-M0+ CPU, frequency up to 48 MHz
- -40°C to 85°C/105°C/125°C operating temperature
- Memories
  - Up to 32 Kbytes of flash memory with protection
  - 6 Kbytes of SRAM with hardware parity check
- CRC calculation unit
- Reset and power management
  - Voltage range: 2.0 V to 3.6 V
  - Power-on / power-down reset (POR/PDR)
  - Programmable brownout reset (BOR)
  - Low-power modes: Sleep, Stop, Standby, Shutdown
- Clock management
  - 4 to 48 MHz crystal oscillator
  - 32 kHz crystal oscillator with calibration
  - Internal 48 MHz RC oscillator (±1 %)
  - Internal 32 kHz RC oscillator (±5 %)
- Up to 18 fast I/Os
  - All mappable on external interrupt vectors
  - All 5 V-tolerant
- 3-channel DMA controller with flexible mapping
- 12-bit, 0.4 µs ADC (up to 13 ext. channels)
  - Conversion range: 0 to 3.6 V
- 8 timers: 16-bit for advanced motor control, four 16-bit general-purpose, two watchdogs, SysTick timer
- Calendar RTC with alarm



- Communication interfaces
  - One I^2C-bus interface supporting Fast-mode Plus (1 Mbit/s) with extra current sink; supporting SMBus/PMBus™ and wake-up from Stop mode
  - Two USARTs with master/slave synchronous SPI; one supporting ISO7816 interface, LIN, IrDA capability, auto baud rate detection and wake-up feature
  - One SPI (24 Mbit/s) with 4- to 16-bit programmable bitframe, multiplexed with I²S interface; two extra SPIs through USARTs
- Development support: serial wire debug (SWD)
- All packages ECOPACK 2 compliant

Table 1. Device summary

Reference	Part number
STM32C011x4	STM32C011F4, STM32C011J4
STM32C011x6	STM32C011F6, STM32C011J6, STM32C011D6

This is information on a product in full production. www.st.com

Contents

1 Introduction 8

2 Description 9

3 Functional overview 11

3.1 Arm® Cortex®-M0+ core with MPU 11

3.2 Memory protection unit 11

3.3 Embedded flash memory 11

3.4 Embedded SRAM 12

3.5 Boot modes 12

3.6 Cyclic redundancy check calculation unit (CRC) 13

3.7 Power supply management 13

3.7.1 Power supply schemes 13

3.7.2 Power supply supervisor 14

3.7.3 Voltage regulator 14

3.7.4 Low-power modes 14

3.7.5 Reset mode 15

3.8 Interconnect of peripherals 15

3.9 Clocks and startup 16

3.10 General-purpose inputs/outputs (GPIOs) 17

3.11 Direct memory access controller (DMA) 17

3.12 DMA request multiplexer (DMAMUX) 18

3.13 Interrupts and events 18

3.13.1 Nested vectored interrupt controller (NVIC) 18

3.13.2 Extended interrupt/event controller (EXTI) 19

3.14 Analog-to-digital converter (ADC) 19

3.14.1 Temperature sensor 19

3.14.2 Internal voltage reference (V_{REFINT}) 20

3.15 Timers and watchdogs 20

3.15.1 Advanced-control timer (TIM1) 21

3.15.2 General-purpose timers (TIM3, 14, 16, 17) 21

3.15.3 Independent watchdog (IWDG) 21

3.15.4 System window watchdog (WWDG) 22

3.15.5 SysTick timer . . . 22
3.16 Real-time clock (RTC) . . . 22
3.17 Inter-integrated circuit interface (I^2C) . . . 23
3.18 Universal synchronous/asynchronous receiver transmitter (USART) . . . 24
3.19 Serial peripheral interface (SPI) . . . 24
3.20 Development support . . . 25
3.20.1 Serial wire debug port (SW-DP) . . . 25

4 Pinouts, pin description and alternate functions . . . 26

5 Electrical characteristics . . . 33
5.1 Parameter conditions . . . 33
5.1.1 Minimum and maximum values . . . 33
5.1.2 Typical values . . . 33
5.1.3 Typical curves . . . 33
5.1.4 Loading capacitor . . . 33
5.1.5 Pin input voltage . . . 33
5.1.6 Power supply scheme . . . 34
5.1.7 Current consumption measurement . . . 34
5.2 Absolute maximum ratings . . . 35
5.3 Operating conditions . . . 36
5.3.1 General operating conditions . . . 36
5.3.2 Operating conditions at power-up / power-down . . . 36
5.3.3 Embedded reset and power control block characteristics . . . 36
5.3.4 Embedded voltage reference . . . 37
5.3.5 Supply current characteristics . . . 38
5.3.6 Wake-up time from low-power modes . . . 48
5.3.7 External clock source characteristics . . . 49
5.3.8 Internal clock source characteristics . . . 53
5.3.9 flash memory characteristics . . . 54
5.3.10 EMC characteristics . . . 56
5.3.11 Electrical sensitivity characteristics . . . 57
5.3.12 I/O current injection characteristics . . . 58
5.3.13 I/O port characteristics . . . 59
5.3.14 NRST input characteristics . . . 63
5.3.15 Analog-to-digital converter characteristics . . . 64

5.3.16 Temperature sensor characteristics 69
5.3.17 Timer characteristics 69
5.3.18 Characteristics of communication interfaces 70

6 Package information 78
6.1 Device marking 78
6.2 SO8N package information (O7) 78
6.3 WLCSP12 package information (B0EK) 81
6.4 TSSOP20 package information (YA) 84
6.5 UFQFPN20 package information (A0A5) 86
6.6 Thermal characteristics 88
6.6.1 Reference documents 88

7 Ordering information 89

8 Important security notice 90

9 Revision history 91

List of tables

Table 1. Device summary . . . 1
Table 2. STM32C011x4/x6 family device features and peripheral counts . . . 9
Table 3. Access status versus readout protection level and execution modes . . . 12
Table 4. Interconnect of peripherals . . . 16
Table 5. Temperature sensor calibration values . . . 20
Table 6. Internal voltage reference calibration values . . . 20
Table 7. Timer feature comparison . . . 20
Table 8. I2C implementation . . . 23
Table 9. USART implementation . . . 24
Table 10. SPI/I2S implementation . . . 25
Table 11. Terms and symbols used in the pin assignment table . . . 28
Table 12. Pin assignment and description . . . 28
Table 13. Port A alternate function mapping (AF0 to AF7) . . . 30
Table 14. Port A alternate function mapping (AF8 to AF15) . . . 31
Table 15. Port B alternate function mapping (AF0 to AF7) . . . 31
Table 16. Port B alternate function mapping (AF8 to AF15) . . . 31
Table 17. Port C alternate function mapping (AF0 to AF7) . . . 31
Table 18. Port C alternate function mapping (AF8 to AF15) . . . 31
Table 19. Port F alternate function mapping . . . 32
Table 20. Voltage characteristics . . . 35
Table 21. Current characteristics . . . 35
Table 22. Thermal characteristics . . . 35
Table 23. General operating conditions . . . 36
Table 24. Operating conditions at power-up / power-down . . . 36
Table 25. Embedded reset and power control block characteristics . . . 36
Table 26. Embedded internal voltage reference . . . 37
Table 27. Current consumption in Run mode from flash memory at different die temperatures . . . 39
Table 28. Current consumption in Run mode from SRAM at different die temperatures . . . 40
Table 29. Typical current consumption in Run depending on code executed . . . 41
Table 30. Current consumption in Sleep mode . . . 43
Table 31. Current consumption in Stop mode . . . 44
Table 32. Current consumption in Standby mode . . . 45
Table 33. Current consumption in Shutdown mode . . . 45
Table 34. Current consumption of peripherals . . . 47
Table 35. Low-power mode wake-up times . . . 48
Table 36. High-speed external user clock characteristics . . . 49
Table 37. Low-speed external user clock characteristics . . . 49
Table 38. HSE oscillator characteristics . . . 50
Table 39. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) . . . 52
Table 40. HSI48 oscillator characteristics . . . 53
Table 41. LSI oscillator characteristics . . . 54
Table 42. Flash memory characteristics . . . 54
Table 43. Flash memory endurance and data retention . . . 55
Table 44. EMS characteristics . . . 56
Table 45. EMI characteristics . . . 57
Table 46. ESD absolute maximum ratings . . . 58
Table 47. Electrical sensitivity . . . 58
Table 48. I/O current injection susceptibility . . . 59

Table 49. I/O static characteristics . . . 59
Table 50. Output voltage characteristics . . . 61
Table 51. I/O AC characteristics . . . 61
Table 52. NRST pin characteristics . . . 63
Table 53. ADC characteristics . . . 64
Table 54. Maximum ADC R_{AIN} . . . 66
Table 55. ADC accuracy . . . 67
Table 56. Temperature sensor characteristics . . . 69
Table 57. TIMx characteristics . . . 69
Table 58. IWDG min/max timeout period at 32 kHz LSI clock . . . 70
Table 59. Minimum I2CCLK frequency . . . 70
Table 60. I2C analog filter characteristics . . . 71
Table 61. SPI characteristics . . . 71
Table 62. I^2S characteristics . . . 74
Table 63. USART (SPI mode) characteristics . . . 76
Table 64. SO8N -Mechanical data . . . 78
Table 65. WLCSP12 – Mechanical data . . . 82
Table 66. WLCSP12 - Example of PCB design rules . . . 83
Table 67. TSSOP20 – Mechanical data . . . 84
Table 68. UFQFPN20 – Mechanical data . . . 87
Table 69. Thermal characteristics . . . 88
Table 70. Document revision history . . . 91

List of figures

Figure 1. Block diagram . . . 10
Figure 2. Power supply overview . . . 14
Figure 3. STM32C011JxM SO8N pinout . . . 26
Figure 4. STM32C011DxY WLCSP12 ballout . . . 26
Figure 5. STM32C011FxP TSSOP20 pinout . . . 27
Figure 6. STM32C011FxU UFQFPN20 pinout . . . 27
Figure 7. Pin loading conditions . . . 33
Figure 8. Pin input voltage . . . 33
Figure 9. Power supply scheme . . . 34
Figure 10. Current consumption measurement scheme . . . 34
Figure 11. V_{REFINT} vs. temperature . . . 38
Figure 12. High-speed external clock source AC timing diagram . . . 49
Figure 13. Low-speed external clock source AC timing diagram . . . 50
Figure 14. Typical application with an 8 MHz crystal . . . 52
Figure 15. Typical application with a 32.768 kHz crystal . . . 53
Figure 16. HSI48 frequency versus temperature . . . 54
Figure 17. I/O input characteristics . . . 60
Figure 18. I/O AC characteristics definition(1) . . . 63
Figure 19. Recommended NRST pin protection . . . 64
Figure 20. ADC accuracy characteristics . . . 68
Figure 21. ADC typical connection diagram . . . 68
Figure 22. SPI timing diagram - slave mode and CPHA = 0 . . . 72
Figure 23. SPI timing diagram - slave mode and CPHA = 1 . . . 73
Figure 24. SPI timing diagram - master mode . . . 73
Figure 25. I^2S slave timing diagram (Philips protocol) . . . 74
Figure 26. I^2S master timing diagram (Philips protocol) . . . 75
Figure 27. USART timing diagram in SPI master mode . . . 76
Figure 28. USART timing diagram in SPI slave mode . . . 77
Figure 29. SO8N -Outline . . . 78
Figure 30. SO8N - Footprint example . . . 80
Figure 31. WLCSP12 – Outline . . . 81
Figure 32. WLCSP12 – Footprint example . . . 83
Figure 33. WLCSP12 package marking example . . . 84
Figure 34. TSSOP20 – Outline . . . 84
Figure 35. TSSOP20 – Footprint example . . . 85
Figure 36. UFQFPN20 – Outline . . . 86
Figure 37. UFQFPN20 – Footprint example . . . 87

1 Introduction

This document provides information on STM32C011x4/x6 microcontrollers, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging, and ordering codes.

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32C011x4/x6 errata sheet ES0569.

Information on memory mapping and control registers is the subject of the reference manual RM0490.

Information on Arm®(a) Cortex®-M0+ core is available from the www.arm.com website.

arm

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2 Description

The STM32C011x4/x6 mainstream microcontrollers are based on high-performance Arm® Cortex®-M0+ 32-bit RISC core operating at up to 48 MHz frequency. Offering a high level of integration, they are suitable for a wide range of applications in consumer, industrial and appliance domains and ready for the Internet of Things (IoT) solutions.

The devices incorporate a memory protection unit (MPU), high-speed embedded memories (6 Kbytes of SRAM and up to 32 Kbytes of flash program memory with read and write protection), DMA, an extensive range of system functions, enhanced I/Os, and peripherals. The devices offer standard communication interfaces (one I^2Cs, one SPI / one I^2S, and two USARTs), one 12-bit ADC (2.5 MSps) with up to 15 channels, a low-power RTC, an advanced control PWM timer, four general-purpose 16-bit timers, two watchdog timers, and a SysTick timer.

The devices operate within ambient temperatures from -40 to 125°C and with supply voltages from 2.0 V to 3.6 V. Optimized dynamic consumption combined with power-saving modes allows the design of low-power applications.

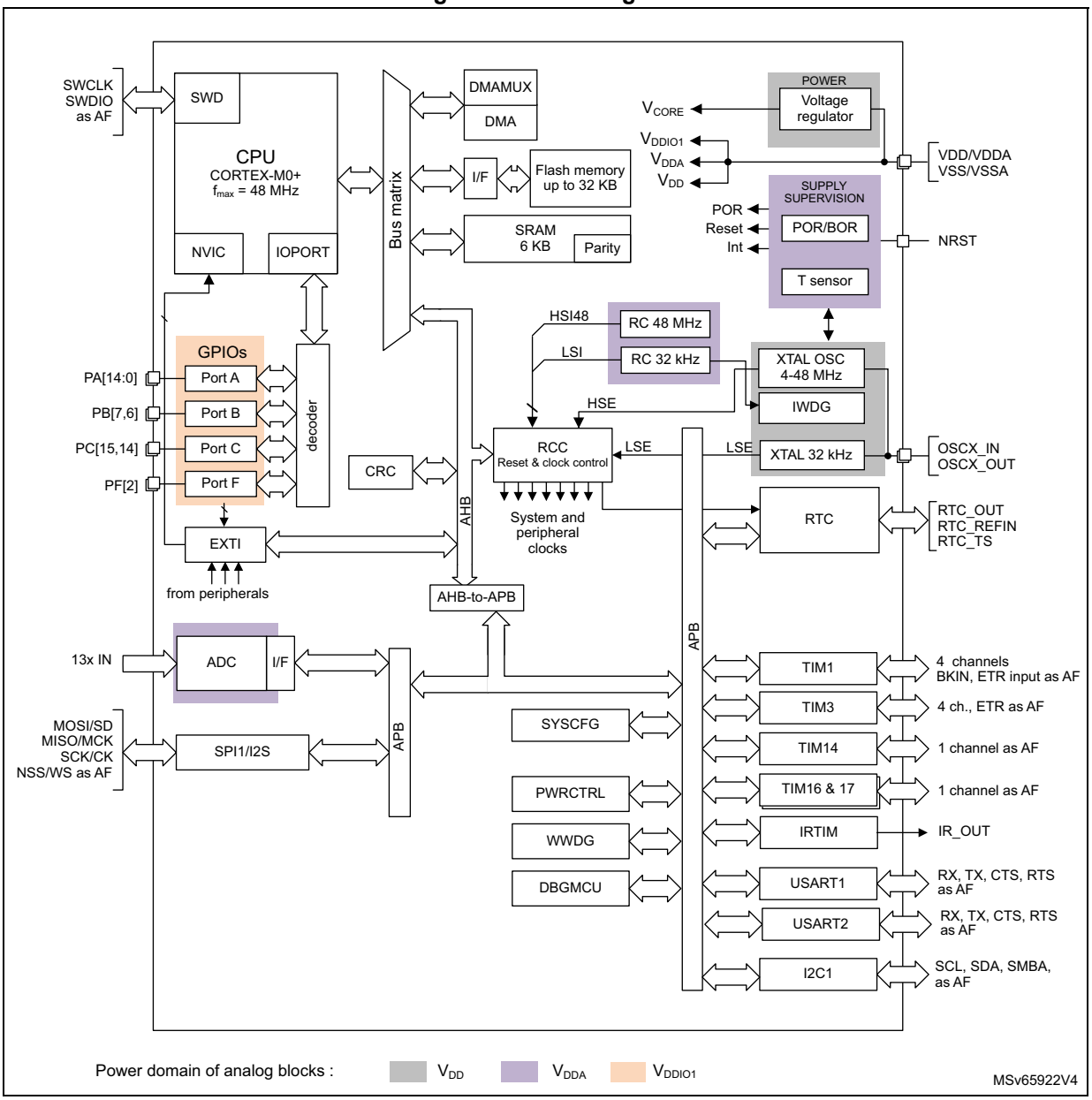
The devices are housed in packages with 8 to 20 pins.

Table 2. STM32C011x4/x6 family device features and peripheral counts

Peripheral		STM32C011_				
		_J4	_J6	_D6	_F4	_F6
Flash memory (Kbyte)		16	32	32	16	32
SRAM (Kbyte)		6 with parity				
Timers	Advanced control	1 (16-bit)				
	General-purpose	4 (16-bit)				
	SysTick	1				
	Watchdog	2				
Comm. interfaces	SPI [I2S](1)	1 [1] + 2 extra through USARTs				
	I2C	1				
	USART	2				
RTC / RNG / AES / VREFBUF		Yes / No / No / No				
GPIOs (all 5V-tolerant)		6		10	18	
DMA channels		3				
Wakeup pins		2		4		
12-bit ADC channels (external + internal)		5 + 2		7 + 2	13 + 2	
Max. CPU frequency		48 MHz				
Operating voltage		2.0 to 3.6 V				
Operating temperature(2)		Ambient: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C				
Package		SO8N		WLCSP12	UFQFPN20	
Bootloader		USART1, I2C1				

1. The number in brackets denotes the count of SPI interfaces configurable as I2S interface.
2. Depends on order code. Refer to *Section 7: Ordering information* for details.

Figure 1. Block diagram



3 Functional overview

3.1 Arm® Cortex®-M0+ core with MPU

The Cortex-M0+ is an entry-level 32-bit Arm Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture, easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area- and power-optimized 32-bit core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to embedded Arm core, the STM32C011x4/x6 devices are compatible with Arm tools and software.

The Cortex-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC) described in *Section 3.13.1*.

3.2 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3 Embedded flash memory

STM32C011x4/x6 devices feature up to 32 Kbytes of embedded flash memory available for storing code and data.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M0+ serial wire), boot in RAM and bootloader selection are disabled. This selection is irreversible.

Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.

3.4 Embedded SRAM

STM32C011x4/x6 devices have 6 Kbytes of embedded SRAM with parity. Hardware parity check allows memory data errors to be detected, which contributes to increasing functional safety of applications.

The memory can be read/write-accessed at CPU clock speed, with 0 wait states.

3.5 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- boot from main flash memory
- boot from system memory
- boot from embedded SRAM

The boot pin is shared with a standard GPIO and can be enabled through the boot selector option bit. The boot loader is located in system memory. It manages the flash memory reprogramming through one of the following interfaces:

- USART on pins PA9/PA10
- I^2C-bus on pins PB6/PB7

If the BOOT0 pin selects the boot from the main flash memory of which the first location is empty, the flash memory empty checker forces the boot from the system memory. The system memory contains an embedded bootloader that then configures some of the GPIOs out of their by-default high-Z state. Refer to AN2606 for more details on the bootloader and on the GPIO configuration when booting from the system memory.

3.6 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

3.7 Power supply management

3.7.1 Power supply schemes

The STM32C011x4/x6 devices require 2.0 V to 3.6 V operating supply voltage (V_{DD}). Several different power supplies are provided to specific peripherals:

- V_{DD} = 2.0 V (1.96 V) to 3.6 V

  V_{DD} is the external power supply for the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD/VDDA pin.

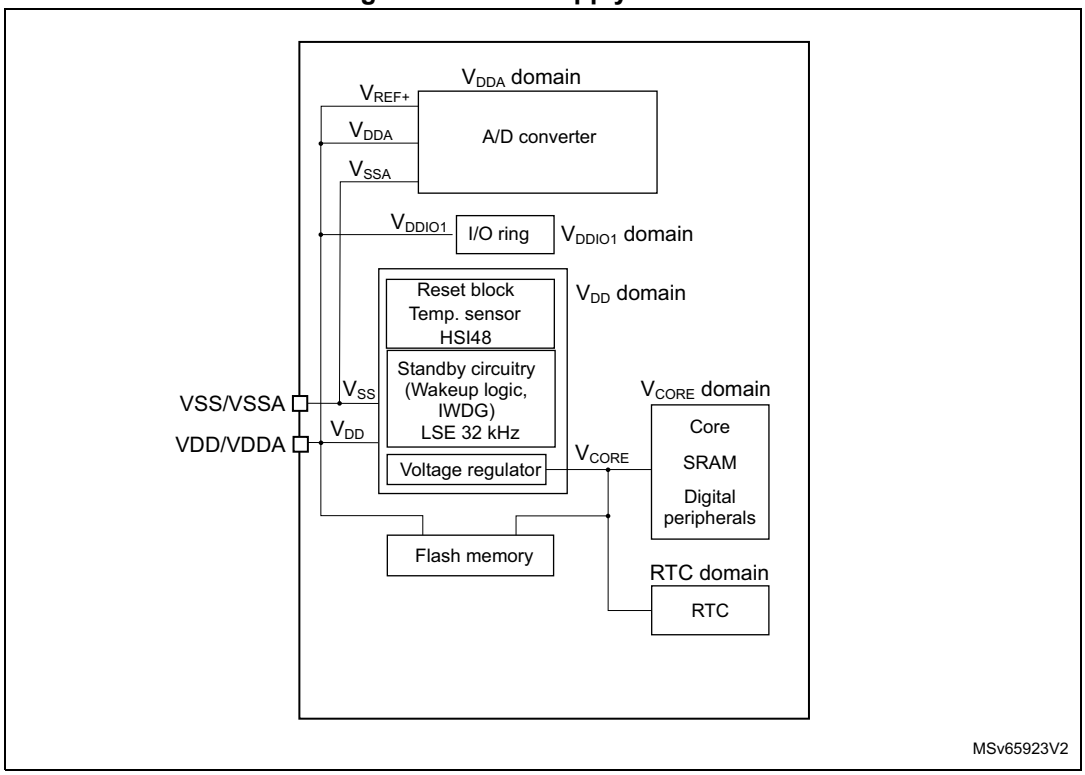
  The minimum voltage of 2.0 V corresponds to power-on reset release threshold V_{POR}(max). Once this threshold is crossed and power-on reset is released, the functionality is guaranteed down to power-down reset threshold V_{PDR}(min) of 1.96 V.
- V_{DDA} = 2.0 V (1.96 V) (ADC) to 3.6 V

  V_{DDA} is the analog power supply for the A/D converter. V_{DDA} voltage level is identical to V_{DD} voltage as it is provided externally through VDD/VDDA pin.
- V_{DDIO1} = V_{DD}

  V_{DDIO1} is the power supply for the I/Os. V_{DDIO1} voltage level is identical to V_{DD} voltage as it is provided externally through VDD/VDDA pin.
- V_{REF+} is the analog peripheral input reference voltage.

  V_{REF+} is internally connected with V_{DD}.
- V_{CORE} is an internal supply for digital peripherals, SRAM and flash memory. It is produced by an embedded linear voltage regulator. On top of V_{CORE}, the flash memory is also powered from V_{DD}.

Figure 2. Power supply overview



3.7.2 Power supply supervisor

The device has an integrated power-on/power-down (POR/PDR) reset active in all power modes except Shutdown and ensuring proper operation upon power-on and power-down. It maintains the device in reset when the supply voltage is below $V_{POR/PDR}$ threshold, without the need for an external reset circuit. Brownout reset (BOR) function allows extra flexibility. It can be enabled and configured through option bytes, by selecting one of four thresholds for rising V_{DD} and other four for falling V_{DD}.

3.7.3 Voltage regulator

An embedded linear voltage regulator supplies most of the digital circuitry in the device.

In Standby and Shutdown modes, the regulator is powered down and its output set in high-impedance state, such as to bring its current consumption close to zero.

3.7.4 Low-power modes

By default, the device is in Run mode after system or power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop** mode

  In Stop mode, the device achieves the lowest power consumption while retaining the SRAM and register contents. All clocks in the V_{CORE} are stopped. The HSE and HSI48

oscillators stop. The HSI48 can be restarted by a peripheral with wake-up capability requiring HSI48.
The LSE and LSI can be kept running. The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

The event of exiting Stop mode enables the HSI48 oscillator and select HSISYS as system clock.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption, with POR/PDR always active in this mode. The regulator is switched off to power down V_{CORE} domain. The HSI48 RC oscillator and the HSE crystal oscillator are also powered down. The RTC is switched off.

  For each I/O, the software can determine whether a pull-up, a pull-down or no resistor shall be applied to that I/O during Standby mode.

  Upon entering Standby mode, register contents are lost, except for 16-bit backup registers whose contents are kept.

  The device exits Standby mode upon external reset event (NRST pin), IWDG reset event, wake-up event (WKUP pin, configurable rising or falling edge), or when a failure is detected on LSE (CSS on LSE).

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off to power down the V_{CORE} domain. The HSI48 and LSI RC-oscillators and HSE crystal oscillator are also powered down. The RTC is off.
  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode.

  SRAM and register contents are lost.

  The device exits Shutdown mode upon external reset event (NRST pin), or wake-up event (WKUP pin, configurable rising or falling edge).

3.7.5 Reset mode

During and upon exiting reset, the Schmitt triggers of I/Os are disabled so as to reduce power consumption. In addition, when the reset source is internal, the built-in pull-up resistor on NRST pin is deactivated.

3.8 Interconnect of peripherals

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep and Stop modes.

Table 4. Interconnect of peripherals

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Stop
TIMx	TIMx	Timer synchronization or chaining	Y	Y	-
	ADCx	Conversion triggers	Y	Y	-
	DMA	Memory-to-memory transfer trigger	Y	Y	-
ADCx	TIM1	Timer triggered by analog watchdog	Y	Y	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	-
All clock sources (internal and external)	TIM14,16,17	Clock source used as input channel for RC measurement and trimming	Y	Y	-
CSS RAM (parity error)	TIM1,16,17	Timer break	Y	Y	-
CPU (hard fault)	TIM1,16,17	Timer break	Y	-	-
GPIO	TIM1,3	External trigger	Y	Y	-
	ADC	Conversion external trigger	Y	Y	-

3.9 Clocks and startup

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** the following clock sources can deliver SYSCLK system clock:
  - 4-48 MHz high-speed oscillator with external crystal or ceramic resonator (HSE). The HSE can also be configured in bypass mode for an external clock.
  - 48 MHz high-speed internal RC oscillator (HSI48), trimmable by software.
  - 32.768 kHz low-speed oscillator with external crystal (LSE), supporting two drive capability modes. The LSE can also be configured in bypass mode for using an external clock.
  - 32 kHz low-speed internal RC oscillator (LSI) with ±5% accuracy, also used to clock an independent watchdog.

- **Peripheral clock sources:** several peripherals (I2S, USART1, I2C1, ADC) can operate with a clock source independent of the system clock.
- **Clock security system (CSS):** in the event of HSE or LSE clock failure, the system clock is automatically switched to HSI48 or LSI, respectively. If enabled, a software interrupt is generated. The CCS feature can be enabled by software.
- **Clock output:**
  - **MCO and MCO2 (microcontroller clock output)** provides one of the internal clocks for external use by the application.
  - **LSCO (low speed clock output)** provides LSI or LSE in all low-power modes.

Several prescalers allow the application to configure AHB and APB domain clock frequencies, 48 MHz at maximum.

3.10 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function (AF). Most of the GPIO pins are shared with special digital or analog functions.

Through a specific sequence, this special function configuration of I/Os can be locked, such as to avoid spurious writing to I/O control registers.

3.11 Direct memory access controller (DMA)

The direct memory access (DMA) controller is a bus master and system peripheral with single-AHB architecture.

With 3 channels, it performs data transfers between memory-mapped peripherals and/or memories, to offload the CPU.

Each channel is dedicated to managing memory access requests from one or more peripherals. The unit includes an arbiter for handling the priority between DMA requests.

Main features of the DMA controller:

- Single-AHB master
- Peripheral-to-memory, memory-to-peripheral, memory-to-memory and peripheral-to-peripheral data transfers
- Access, as source and destination, to on-chip memory-mapped devices such as flash memory, SRAM, and AHB and APB peripherals
- All DMA channels independently configurable:
  - Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
  - Priority between the requests is programmable by software (four levels per channel: very high, high, medium, low) and by hardware in case of equality (such as request to channel 1 has priority over request to channel 2).
  - Transfer size of source and destination are independent (byte, half-word, word), emulating packing and unpacking. Source and destination addresses must be aligned on the data size.

  - Support of transfers from/to peripherals to/from memory with circular buffer management
  - Programmable number of data to be transferred: 0 to 2^{16} - 1
- Generation of an interrupt request per channel. Each interrupt request originates from any of the three DMA events: transfer complete, half transfer, or transfer error.

3.12 DMA request multiplexer (DMAMUX)

The DMAMUX request multiplexer enables routing a DMA request line between the peripherals and the DMA controller. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. DMAMUX may also be used as a DMA request generator from programmable events on its input trigger signals.

3.13 Interrupts and events

The device flexibly manages events causing interrupts of linear program execution, called exceptions. The Cortex-M0+ processor core, a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI) are the assets contributing to handling the exceptions. Exceptions include core-internal events such as, for example, a division by zero and, core-external events such as logical level changes on physical lines. Exceptions result in interrupting the program flow, executing an interrupt service routine (ISR) then resuming the original program flow.

The processor context (contents of program pointer and status registers) is stacked upon program interrupt and unstacked upon program resume, by hardware. This avoids context stacking and unstacking in the interrupt service routines (ISRs) by software, thus saving time, code and power. The ability to abandon and restart load-multiple and store-multiple operations significantly increases the device’s responsiveness in processing exceptions.

3.13.1 Nested vectored interrupt controller (NVIC)

The configurable nested vectored interrupt controller is tightly coupled with the core. It handles physical line events associated with a non-maskable interrupt (NMI) and maskable interrupts, and Cortex-M0+ exceptions. It provides flexible priority management.

The tight coupling of the processor core with NVIC significantly reduces the latency between interrupt events and start of corresponding interrupt service routines (ISRs). The ISR vectors are listed in a vector table, stored in the NVIC at a base address. The vector address of an ISR to execute is hardware-built from the vector table base address and the ISR order number used as offset.

If a higher-priority interrupt event happens while a lower-priority interrupt event occurring just before is waiting for being served, the later-arriving higher-priority interrupt event is served first. Another optimization is called tail-chaining. Upon a return from a higher-priority ISR then start of a pending lower-priority ISR, the unnecessary processor context unstacking and stacking is skipped. This reduces latency and contributes to power efficiency.

Features of the NVIC:

- Low-latency interrupt processing
- 4 priority levels
- Handling of a non-maskable interrupt (NMI)
- Handling of 32 maskable interrupt lines
- Handling of 10 Cortex-M0+ exceptions
- Later-arriving higher-priority interrupt processed first
- Tail-chaining
- Interrupt vector retrieval by hardware

3.13.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller adds flexibility in handling physical line events and allows identifying wake-up events at processor wake-up from Stop mode.

The EXTI controller has a number of channels, of which some with rising, falling or rising, and falling edge detector capability. Any GPIO and a few peripheral signals can be connected to these channels.

The channels can be independently masked.

The EXTI controller can capture pulses shorter than the internal clock period.

A register in the EXTI controller latches every event even in Stop mode, which allows the software to identify the origin of the processor's wake-up from Stop mode or, to identify the GPIO and the edge event having caused an interrupt.

3.14 Analog-to-digital converter (ADC)

A native 12-bit analog-to-digital converter is embedded into STM32C011x4/x6 devices. The ADC has up to 13 external channels and 2 internal channels (temperature sensor, voltage reference). It performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 2.5 MSps even with a low CPU speed. An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate in the whole V_{DD} supply range.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions with timers.

3.14.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to an ADC input to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor may vary from part to part due to process variation, the uncalibrated internal temperature sensor is suitable only for relative temperature measurements.

To improve the accuracy of the temperature sensor, each part is individually factory-calibrated by ST. The resulting calibration data are stored in the part's engineering bytes, accessible in read-only mode.

Table 5. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF7568-0x1FFF7569

3.14.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to an ADC input. The V_{REFINT} voltage is individually precisely measured for each part by ST during production test and stored in the part's engineering bytes. It is accessible in read-only mode.

Table 6. Internal voltage reference calibration values

Calibration value name	Description	Memory address
V_{REFINT}	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF756A-0x1FFF756B

3.15 Timers and watchdogs

The device includes an advanced-control timer, four general-purpose timers, two low-power timers, two watchdog timers and a SysTick timer. *Table 7* compares features of the advanced-control, general-purpose and basic timers.

Table 7. Timer feature comparison

Timer	Timer type	Counter resolution	Counter type	Maximum operating frequency	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary outputs
TIM1	Advanced-control	16-bit	Up, down, up/down	48 MHz	Integer from 1 to 2^{16}	Yes	4 +2 internal	3
TIM3	General-purpose	16-bit	Up, down, up/down	48 MHz	Integer from 1 to 2^{16}	Yes	4	-
TIM14	General-purpose	16-bit	Up	48 MHz	Integer from 1 to 2^{16}	No	1	-
TIM16 TIM17	General-purpose	16-bit	Up	48 MHz	Integer from 1 to 2^{16}	Yes	1	1

3.15.1 Advanced-control timer (TIM1)

The advanced-control timer can be seen as a three-phase PWM unit multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM output (edge or center-aligned modes) with full modulation capability (0-100%)
- one-pulse mode output

On top of these, there are two internal channels that can be used.

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled, so as to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.15.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.15.2 General-purpose timers (TIM3, 14, 16, 17)

There are four synchronizable general-purpose timers embedded in the device (refer to *Table 7* for comparison). Each general-purpose timer can be used to generate PWM outputs or act as a simple timebase.

- TIM3

  This is a full-featured general-purpose timer with 16-bit auto-reload up/downcounter and 16-bit prescaler.

  It has four independent channels for input capture/output compare, PWM or one-pulse mode output. It can operate in combination with other general-purpose timers via the Timer Link feature for synchronization or event chaining. It can generate independent DMA request and support quadrature encoders. Its counter can be frozen in debug mode.

- TIM14

  This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. It has one channel for input capture/output compare, PWM output or one-pulse mode output. Its counter can be frozen in debug mode.

- TIM16, TIM17

  These are general-purpose timers featuring:

  – 16-bit auto-reload upcounter and 16-bit prescaler

  – 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output. The timers can operate together via the Timer Link feature for synchronization or event chaining. They can generate independent DMA request. Their counters can be frozen in debug mode.

3.15.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 32 kHz internal RC (LSI).

Independent of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. Its counter can be frozen in debug mode.

3.15.4 System window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked by the system clock. It has an early-warning interrupt capability. Its counter can be frozen in debug mode.

3.15.5 SysTick timer

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter.

Features of SysTick timer:

- 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.16 Real-time clock (RTC)

The devices embed an RTC located in the RTC domain and supplied from V_{CORE}.

The RTC is an independent BCD timer/counter.

Features of the RTC:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Programmable alarm
- On-the-fly correction from 1 to 32767 RTC clock pulses, usable for synchronization with a master clock
- Reference clock detection - a more precise second-source clock (50 or 60 Hz) can be used to improve the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature to save a calendar snapshot, triggered by an event on the timestamp pin
- Multiple clock sources and references:
  - a 32.768 kHz external crystal (LSE)
  - an external resonator or oscillator (LSE)
  - the internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
  - the high-speed external clock (HSE) divided by 32

The RTC operates in Run, Sleep, and Stop mode.

RTC events (Alarm, Timestamp) can generate an interrupt and wake the device up from the low-power modes.

3.17 Inter-integrated circuit interface (I2C)

The devices embed one I2C peripheral. Refer to *Table 8* for the features.

The I2C peripheral handles communication between the microcontroller and the serial I^2C-bus. It controls all I^2C-bus-specific sequencing, protocol, arbitration and timing.

Features of the I2C peripheral:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and extra output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Clock stretching
- SMBus specification rev 3.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Command and data acknowledge control
  - Address resolution protocol (ARP) support
  - Host and device support
  - SMBus alert
  - Timeouts and idle condition detection
- PMBus rev 1.3 standard compatibility
- Independent clock: a choice of independent clock sources allowing the I^2C-bus communication speed to be independent of the PCLK reprogramming
- Wake-up from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 8. I2C implementation

I2C features(1)	I2C1
Standard-mode (up to 100 kbit/s)	X
Fast-mode (up to 400 kbit/s)	X
Fast-mode Plus (up to 1 Mbit/s) with extra output drive I/Os	X
Programmable analog and digital noise filters	X
SMBus/PMBus hardware support	X
Independent clock	X
Wake-up from Stop mode on address match	X

1. X: supported

3.18 Universal synchronous/asynchronous receiver transmitter (USART)

The devices embed two universal synchronous/asynchronous receivers/transmitters that communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, synchronous SPI communication and single-wire half-duplex communication mode. Some can also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and have a clock domain independent of the CPU clock, which allows them to wake up the MCU from Stop mode. The wake-up events from Stop mode are programmable and can be:

- start bit detection
- any received data frame
- a specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 9. USART implementation

USART modes/features(1)	USART1	USART2
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
SPI emulation master/slave (synchronous mode)	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wake-up from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X: supported

3.19 Serial peripheral interface (SPI)

The devices contain one SPI running at up to 24 Mbits/s in master and slave modes. It supports half-duplex, full-duplex and simplex communications. A 3-bit prescaler gives eight master mode frequencies. The frame size is configurable from 4 bits to 16 bits. The SPI peripherals support NSS pulse mode, TI mode and hardware CRC calculation.

The SPI peripherals can be served by the DMA controller.

The I^2S interface mode of the SPI peripheral (if supported, see the following table) supports four different audio standards can operate as master or slave, in half-duplex communication

mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 10. SPI/I2S implementation

SPI features(1)	SPI1
Hardware CRC calculation	X
Rx/Tx FIFO	X
NSS pulse mode	X
I^2S mode	X
TI mode	X

1. X = supported.

3.20 Development support

3.20.1 Serial wire debug port (SW-DP)

An Arm SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts, pin description and alternate functions

Figure 3. STM32C011JxM SO8N pinout

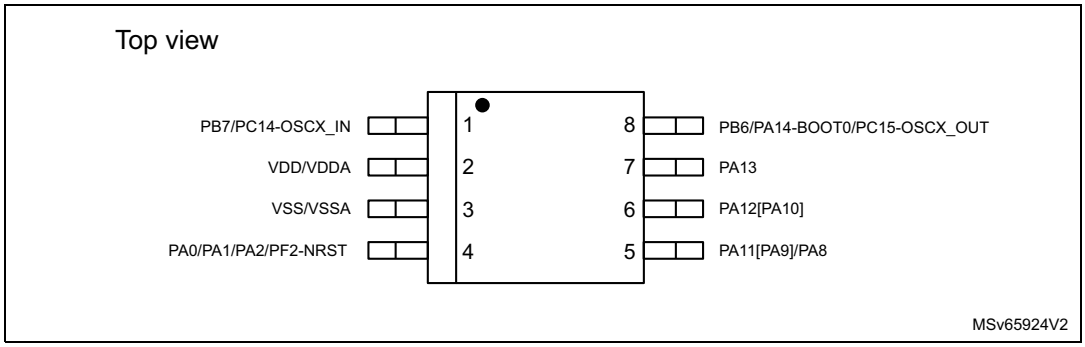


Figure 4. STM32C011DxY WLCSP12 ballout

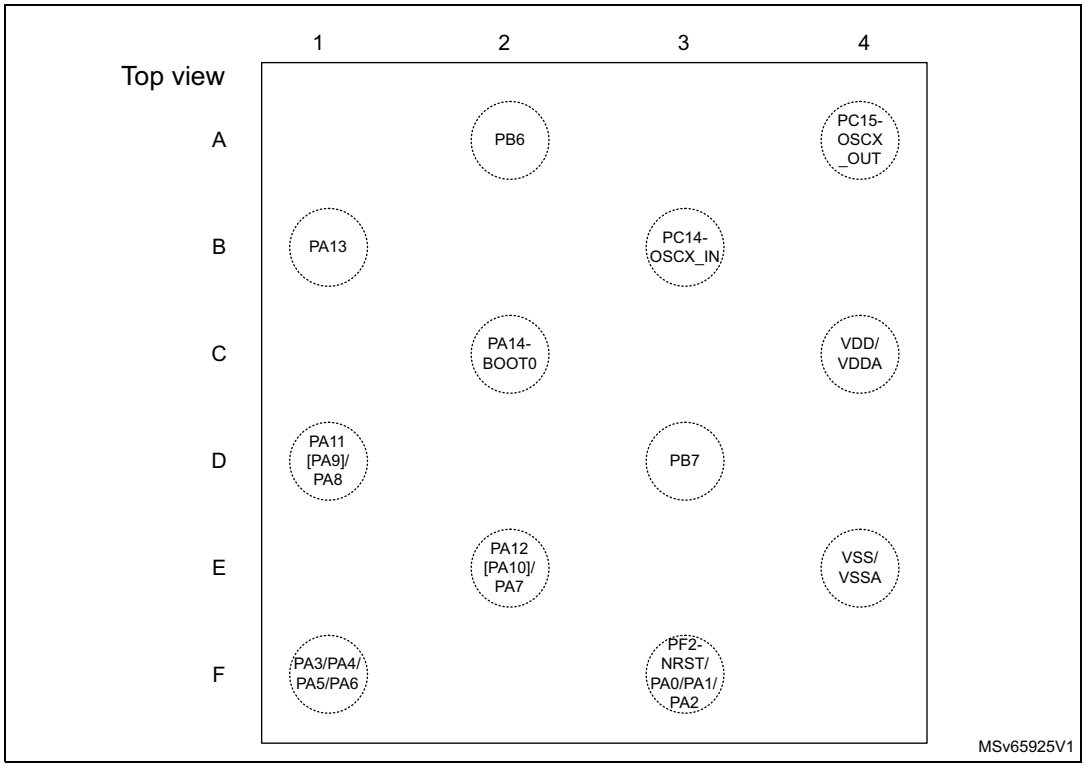


Figure 5. STM32C011FxP TSSOP20 pinout

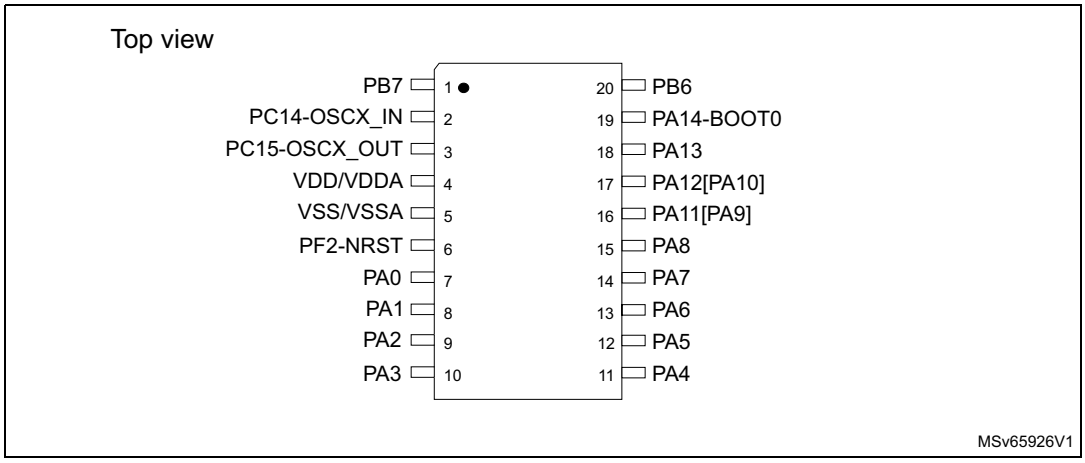


Figure 6. STM32C011FxU UFQFPN20 pinout

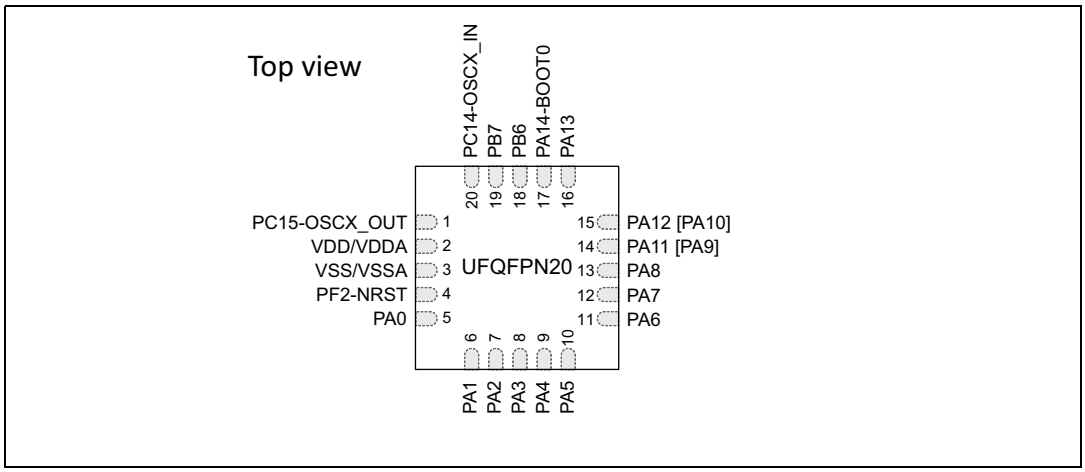


Table 11. Terms and symbols used in the pin assignment table

Column		Symbol	Definition
Pin name		Terminal name corresponds to its by-default function at reset, unless otherwise specified in parenthesis under the pin name.	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		RST	Reset pin with embedded weak pull-up resistor
		Options for FT I/Os	
		_f	I/O, Fm+ capable
		_a	I/O, with analog switch function
Note		Upon reset, all I/Os are set as analog inputs, unless otherwise specified.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 12. Pin assignment and description

Pin				Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
SO8N	WLCSP12	TSSOP20	UFQFPN20						
1	B3	2	20	PC14-OSCX_IN (PC14)	I/O	FT_f	-	USART1_TX, TIM1_ETR, TIM1_BKIN2, IR_OUT, USART2_RTS_DE_CK, TIM17_CH1, TIM3_CH2, I2C1_SDA, EVENTOUT	OSCX_IN
8	A4	3	1	PC15-OSCX_OUT (PC15)	I/O	FT	-	OSC32_EN, OSC_EN, TIM1_ETR, TIM3_CH3	OSCX_OUT
2	C4	4	2	VDD/VDDA	S	-	-	-	-
3	E4	5	3	VSS/VSSA	S	-	-	-	-
4	F3	6	4	PF2-NRST	I/O	RST, FT	(1)	MCO, TIM1_CH4	NRST
4	F3	7	5	PA0	I/O	FT_a	-	USART2_CTS, TIM16_CH1, USART1_TX, TIM1_CH1	ADC_IN0, WKUP1
4	F3	8	6	PA1	I/O	FT_a	-	SPI1_SCK/I2S1_CK, USART2_RTS_DE_CK, TIM17_CH1, USART1_RX, TIM1_CH2, I2C1_SMBA, EVENTOUT	ADC_IN1

Table 12. Pin assignment and description (continued)

Pin				Pin name (function upon reset)	Pin type	I/O structure	Note	Alternate functions	Additional functions
SO8N	WLCSP12	TSSOP20	UFQFPN20						
4	F3	9	7	PA2	I/O	FT_a	-	SPI1_MOSI/I2S1_SD, USART2_TX, TIM16_CH1N, TIM3_ETR, TIM1_CH3	ADC_IN2, WKUP4,LSCO
-	F1	10	8	PA3	I/O	FT_a	-	USART2_RX, TIM1_CH1N, TIM1_CH4, EVENTOUT	ADC_IN3
-	F1	11	9	PA4	I/O	FT_a	-	SPI1_NSS/I2S1_WS, USART2_TX, TIM1_CH2N, TIM14_CH1, TIM17_CH1N, EVENTOUT	ADC_IN4, RTC_TS, RTC_OUT1, WKUP2
-	F1	12	10	PA5	I/O	FT_a	-	SPI1_SCK/I2S1_CK, USART2_RX, TIM1_CH3N, TIM1_CH1, EVENTOUT	ADC_IN5
-	F1	13	11	PA6	I/O	FT_a	-	SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1	ADC_IN6
-	E2	14	12	PA7	I/O	FT_a	-	SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM1_CH1N, TIM14_CH1, TIM17_CH1	ADC_IN7
5	D1	15	13	PA8	I/O	FT_a	-	MCO, USART2_TX, TIM1_CH1, EVENTOUT, SPI1_NSS/I2S1_WS, TIM1_CH2N, TIM1_CH3N, TIM3_CH3, TIM3_CH4, TIM14_CH1, USART1_RX, MCO2	ADC_IN8
-	-	-	-	PA9	I/O	FT_f	(2)	MCO, USART1_TX, TIM1_CH2, TIM3_ETR, I2C1_SCL, EVENTOUT	-
-	-	-	-	PA10	I/O	FT_f	(2)	USART1_RX, TIM1_CH3, MCO2, TIM17_BKIN, I2C1_SDA, EVENTOUT	-
5	D1	16	14	PA11 [PA9]	I/O	FT_a	(2)	SPI1_MISO/I2S1_MCK, USART1_CTS, TIM1_CH4, TIM1_BKIN2	ADC_IN11
6	E2	17	15	PA12 [PA10]	I/O	FT_a	(2)	SPI1_MOSI/I2S1_SD, USART1_RTS_DE_CK, TIM1_ETR, I2S_CKIN	ADC_IN12
7	B1	18	16	PA13	I/O	FT_a	(3)	SWDIO, IR_OUT, TIM3_ETR, USART2_RX, EVENTOUT	ADC_IN13
8	C2	19	17	PA14-BOOT0	I/O	FT_a	(3)	SWCLK, USART2_TX, EVENTOUT, SPI1_NSS/I2S1_WS, USART2_RX, TIM1_CH1, MCO2, USART1_RTS_DE_CK	ADC_IN14, BOOT0
8	A2	20	18	PB6	I/O	FT_f	-	USART1_TX, TIM1_CH3, TIM16_CH1N, TIM3_CH3, USART1_RTS_DE_CK, USART1_CTS, I2C1_SCL, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI1_MISO/I2S1_MCK, SPI1_SCK/I2S1_CK, TIM1_CH2, TIM3_CH1, TIM3_CH2, TIM16_BKIN, TIM17_BKIN	WKUP3
1	D3	1	19	PB7	I/O	FT_f	-	USART1_RX, TIM1_CH4, TIM17_CH1N, TIM3_CH4, I2C1_SDA, EVENTOUT, USART2_CTS, TIM16_CH1, TIM3_CH1, I2C1_SCL	RTC_REFIN

1. RST I/O structure when the PF2-NRST pin is configured as reset (input or input/output mode), FT I/O structure when the PF2-NRST pin is configured as GPIO
2. Pins PA9 and PA10 can be remapped in place of pins PA11 and PA12 (default mapping), using SYSCFG_CFGR1 register.
3. Upon reset, this pin is configured as SWD alternate function, and the internal pull-up on PA13 pin and the internal pull-down on PA14 pin are activated.

Table 13. Port A alternate function mapping (AF0 to AF7)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART2_CTS	TIM16_CH1	-	USART1_TX	TIM1_CH1	-	-
PA1	SPI1_SCK/I2S1_CK	USART2_RTS_DE_CK	TIM17_CH1	-	USART1_RX	TIM1_CH2	I2C1_SMBA	EVENTOUT
PA2	SPI1_MOSI/I2S1_SD	USART2_TX	TIM16_CH1N	TIM3_ETR	-	TIM1_CH3	-	-
PA3	-	USART2_RX	TIM1_CH1N	-	-	TIM1_CH4	-	EVENTOUT
PA4	SPI1_NSS/I2S1_WS	USART2_TX	TIM1_CH2N	-	TIM14_CH1	TIM17_CH1N	-	EVENTOUT
PA5	SPI1_SCK/I2S1_CK	USART2_RX	TIM1_CH3N	-	-	TIM1_CH1	-	EVENTOUT
PA6	SPI1_MISO/I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	-	-
PA7	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	-	-
PA8	MCO	USART2_TX	TIM1_CH1	-	-	-	-	EVENTOUT
PA9	MCO	USART1_TX	TIM1_CH2	TIM3_ETR	-	-	I2C1_SCL	EVENTOUT
PA10	-	USART1_RX	TIM1_CH3	MCO2	-	TIM17_BKIN	I2C1_SDA	EVENTOUT
PA11	SPI1_MISO/I2S1_MCK	USART1_CTS	TIM1_CH4	-	-	TIM1_BKIN2	-	-
PA12	SPI1_MOSI/I2S1_SD	USART1_RTS_DE_CK	TIM1_ETR	-	-	I2S_CKIN	-	-
PA13	SWDIO	IR_OUT	-	TIM3_ETR	USART2_RX	-	-	EVENTOUT
PA14	SWCLK	USART2_TX	-	-	-	-	-	EVENTOUT

Table 14. Port A alternate function mapping (AF8 to AF15)

Port	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA8	SPI1_NSS/I2S1_WS	TIM1_CH2N	TIM1_CH3N	TIM3_CH3	TIM3_CH4	TIM14_CH1	USART1_RX	MCO2
PA14	SPI1_NSS/I2S1_WS	USART2_RX	TIM1_CH1	MCO2	USART1_RTS_DE_CK	-	-	-

Table 15. Port B alternate function mapping (AF0 to AF7)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB6	USART1_TX	TIM1_CH3	TIM16_CH1N	TIM3_CH3	USART1_RTS_DE_CK	USART1_CTS	I2C1_SCL	I2C1_SMBA
PB7	USART1_RX	TIM1_CH4	TIM17_CH1N	TIM3_CH4	-	-	I2C1_SDA	EVENTOUT

Table 16. Port B alternate function mapping (AF8 to AF15)

Port	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB6	SPI1_MOSI/I2S1_SD	SPI1_MISO/I2S1_MCK	SPI1_SCK/I2S1_CK	TIM1_CH2	TIM3_CH1	TIM3_CH2	TIM16_BKIN	TIM17_BKIN
PB7	-	USART2_CTS	TIM16_CH1	TIM3_CH1	-	-	I2C1_SCL	-

Table 17. Port C alternate function mapping (AF0 to AF7)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC14	USART1_TX	TIM1_ETR	TIM1_BKIN2	-	-	-	-	-
PC15	OSC32_EN	OSC_EN	TIM1_ETR	TIM3_CH3	-	-	-	-

Table 18. Port C alternate function mapping (AF8 to AF15)

Port	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC14	IR_OUT	USART2_RTS_DE_CK	TIM17_CH1	TIM3_CH2	-	-	I2C1_SDA	EVENTOUT

Table 19. Port F alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF2	MCO	TIM1_CH4	-	-	-	-	-	-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

Parameter values defined at temperatures or in temperature ranges out of the ordering information scope are to be ignored.

Packages used for characterizing certain electrical parameters may differ from the commercial packages as per the ordering information.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A(max) (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions

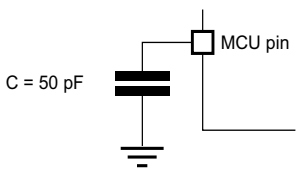
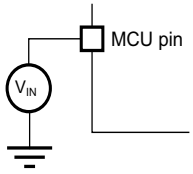
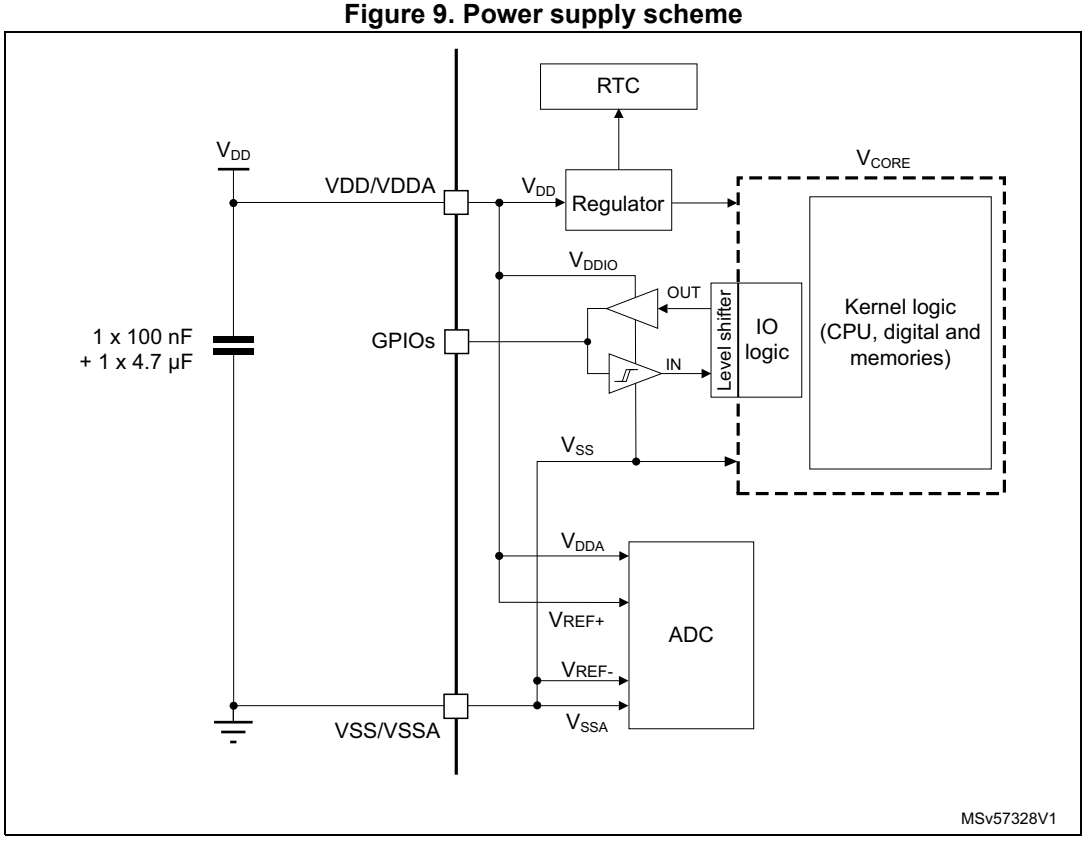


Figure 8. Pin input voltage



5.1.6 Power supply scheme

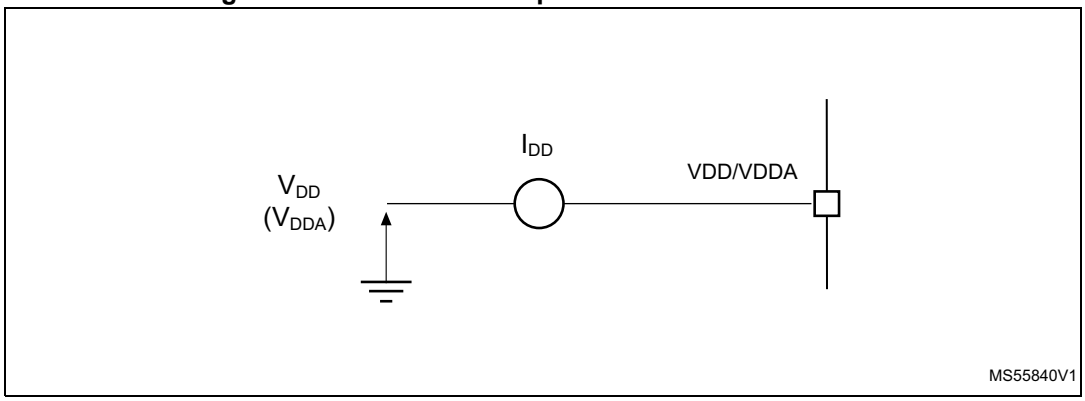
Figure 9. Power supply scheme



Caution: Power supply pin pair (VDD/VDDA and VSS/VSSA) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

5.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 20*, *Table 21* and *Table 22* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile (application conditions) is compliant with the JEDEC JESD47 qualification standard.

All voltages are defined with respect to V_{SS}.

Table 20. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External supply voltage	-0.3	4.0	V
V_{IN}(1)	Input voltage on pin	-0.3	V_{DD} + 4.0(2)(3)	

1. V_{IN} maximum must always be respected. Refer to *Table 21* for the maximum allowed injected current values.
2. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
3. When an FT_a pin is used for interfacing with an analog peripheral (such as ADC), the maximum V_{IN} is 4 V.

Table 21. Current characteristics

Symbol	Ratings	Max	Unit
$I_{VDD/VDDA}$	Current into VDD/VDDA power pin (source)	100	mA
$I_{VSS/VSSA}$	Current out of VSS/VSSA ground pin (sink)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(1)	80	
	Total output current sourced by sum of all I/Os and control pins(1)	80	
$I_{INJ(PIN)}$(1)(2)	Injected current on a FT_xx pin	-5 / 0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(3)	-25	

1. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
2. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 20: Voltage characteristics* for the maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 22. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	130	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 23. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Standard operating voltage	-	2.0(1)	3.6	V
V_{IN}	I/O input voltage	-	-0.3	Min (VDD + 3.6, 5.5)(2)	V
f_{PCLK}	APB clock frequency	-	-	48	MHz
T_A	Ambient temperature(3)	Suffix 6(4)	-40	85	°C
		Suffix 7(4)	-40	105	
		Suffix 3(4)	-40	125	
T_J	Junction temperature	Suffix 6(4)	-40	105	°C
		Suffix 7(4)	-40	125	
		Suffix 3(4)	-40	130	

1. When RESET is released functionality is guaranteed down to V_{PDR} min.
2. For operation with voltage higher than VDD +0.3 V, the internal pull-up and pull-down resistors must be disabled.
3. The T_A(max) applies to P_D(max). At $P_D < P_D$(max) the ambient temperature is allowed to go higher than T_A(max) provided that the junction temperature T_J does not exceed T_J(max). Refer to *Section 6.6: Thermal characteristics*.
4. Temperature range digit in the order code. See *Section 7: Ordering information*.

5.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 24* are derived from tests performed under the ambient temperature condition summarized in *Table 23*.

Table 24. Operating conditions at power-up / power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 25* are derived from tests performed under the ambient temperature conditions summarized in *Table 23*.

Table 25. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	POR temporization when V_{DD} crosses V_{POR}	V_{DD} rising	-	270	500	µs
V_{POR}(1)	Power-on reset threshold	-	1.9	1.94	1.98	V
V_{PDR}(1)	Power-down reset threshold	-	1.88	1.92	1.96	V

Table 25. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR1}	Brownout reset threshold 1	V_{DD} rising	2.05	2.10	2.18	V
		V_{DD} falling	1.95	2.00	2.08	
V_{BOR2}	Brownout reset threshold 2	V_{DD} rising	2.20	2.31	2.38	V
		V_{DD} falling	2.10	2.21	2.28	
V_{BOR3}	Brownout reset threshold 3	V_{DD} rising	2.50	2.62	2.68	V
		V_{DD} falling	2.40	2.52	2.58	
V_{BOR4}	Brownout reset threshold 4	V_{DD} rising	2.80	2.91	3.00	V
		V_{DD} falling	2.70	2.81	2.90	
$V_{hyst_POR_PDR}$	Hysteresis of V_{POR} and V_{PDR}	-	-	20	-	mV
V_{hyst_BOR}	Hysteresis of V_{BORx}	-	-	100	-	mV
$I_{DD(BOR)}$(1)	BOR consumption	-	-	2.2	2.5	µA

1. Specified by design – Not tested in production.

5.3.4 Embedded voltage reference

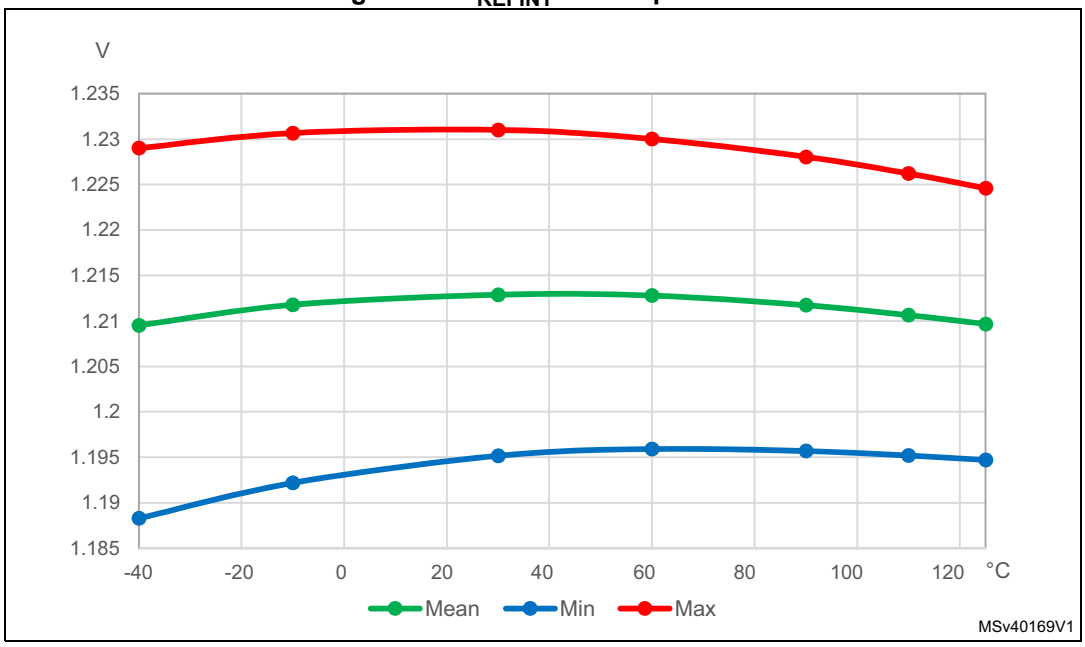
The parameters given in *Table 26* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 26. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-	1.182	1.212	1.232	V
$t_{S_vrefint}$ (1)(2)	ADC sampling time when reading the internal reference voltage	-	4	-	-	µs
$t_{start_vrefint}$(2)	Start time of reference voltage buffer when ADC is enable	-	-	8	12	µs
$I_{DD(VREFINTBUF)}$(2)	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	9	13.5	23	µA
ΔV_{REFINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	30	50	mV
T_{Coeff}	Averange temperature coefficient	-	-	20	70	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25 °C	-	300	1000	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200	ppm/V

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Specified by design – Not tested in production.

Figure 11. V_{REFINT} vs. temperature



5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0490 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$
- For flash memory and shared peripherals $f_{PCLK} = f_{HCLK} = f_{HCLKS}$

Unless otherwise stated, values given in *Table 27* through *Table 34* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 27. Current consumption in Run mode from flash memory at different die temperatures

Symbol	Parameter	Conditions			Typ				Max(1)				Unit
		General(2)	f_{HCLK}	Fetch from(3)	25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE_bypass}$ (> 32.768 kHz), $f_{HCLK} = f_{LSE_bypass}$ (= 32.768 kHz)	48 MHz	Flash memory	3.05	3.15	3.25	3.35	3.60	3.80	4.10	4.60	mA
			32 MHz		2.10	2.15	2.25	2.35	2.50	2.70	3.00	3.50	
			24 MHz		1.80	1.85	1.90	2.05	2.10	2.40	2.70	3.20	
			16 MHz		1.25	1.30	1.35	1.45	1.50	1.70	2.00	2.50	
			8 MHz		0.655	0.710	0.765	0.865	0.790	1.10	1.40	1.90	
			4 MHz		0.3654	0.420	0.470	0.570	0.460	0.700	0.980	1.50	
			2 MHz		0.225	0.270	0.325	0.425	0.290	0.540	0.820	1.40	
			1 MHz		0.150	0.200	0.250	0.350	0.200	0.450	0.730	1.30	
			500 kHz		0.115	0.160	0.215	0.315	0.160	0.410	0.690	1.20	
			125 kHz		0.0875	0.135	0.185	0.285	0.130	0.380	0.650	1.20	
			32.768 kHz		0.082	0.130	0.180	0.280	0.120	0.370	0.650	1.20	
		$f_{HCLK} = f_{HSI48/HSIDIV}$ (> 32 kHz), $f_{HCLK} = f_{LSI}$ (= 32 kHz)	48 MHz		3.40	3.50	3.55	3.60	3.90	4.10	4.40	4.90	
			24 MHz		2.25	2.30	2.35	2.45	2.60	2.80	3.10	3.60	
			12 MHz		1.45	1.50	1.55	1.65	1.70	1.90	2.20	2.70	
			6 MHz		1.05	1.10	1.15	1.20	1.20	1.40	1.70	2.20	
			3 MHz		0.855	0.880	0.925	1.00	0.960	1.20	1.50	2.00	
			1.5 MHz		0.750	0.780	0.825	0.915	0.840	1.10	1.40	1.90	
			750 kHz		0.700	0.730	0.775	0.865	0.780	1.00	1.30	1.80	
			375 kHz		0.675	0.705	0.750	0.840	0.760	0.970	1.30	1.80	
			32 kHz		0.082	0.130	0.180	0.280	0.120	0.370	0.650	1.20	

1. Evaluated by characterization – Not tested in production.
2. V_{DD} = 3.0 V for values in Typ columns and 3.6 V for values in Max columns, all peripherals disabled.
3. Prefetch disabled and cache enabled when fetching from flash memory.

Table 28. Current consumption in Run mode from SRAM at different die temperatures

Symbol	Parameter	Conditions			Typ				Max(1)				Unit
		General(2)	f_{HCLK}	Fetch from(3)	25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE_bypass}$ (>32.768 kHz), $f_{HCLK} = f_{LSE_bypass}$ (=32.768 kHz)	48 MHz	SRAM	2.80	2.90	2.95	3.05	3.20	3.40	3.70	4.20	mA
			32 MHz		1.90	1.95	2.00	2.10	2.20	2.40	2.70	3.20	
			24 MHz		1.45	1.50	1.55	1.65	1.70	1.90	2.20	2.70	
			16 MHz		0.990	1.05	1.10	1.20	1.20	1.40	1.70	2.20	
			8 MHz		0.535	0.585	0.635	0.735	0.630	0.860	1.20	1.70	
			4 MHz		0.305	0.355	0.405	0.505	0.380	0.630	0.900	1.40	
			2 MHz		0.195	0.240	0.295	0.390	0.250	0.500	0.770	1.30	
			1 MHz		0.135	0.185	0.235	0.335	0.180	0.430	0.710	1.30	
			500 kHz		0.110	0.155	0.205	0.305	0.150	0.400	0.670	1.20	
			125 kHz		0.0865	0.135	0.185	0.285	0.130	0.370	0.650	1.20	
			32.768 kHz		0.082	0.130	0.180	0.280	0.120	0.370	0.640	1.20	
		$f_{HCLK} = f_{HSI48/HSIDIV}$ (> 32 kHz), $f_{HCLK} = f_{LSI}$ (= 32 kHz)	48 MHz		3.15	3.20	3.25	3.30	3.50	3.70	3.90	4.40	
			24 MHz		1.90	1.95	2.00	2.05	2.10	2.30	2.60	3.10	
			12 MHz		1.30	1.30	1.35	1.45	1.50	1.70	1.90	2.40	
			6 MHz		0.965	0.995	1.05	1.15	1.15	1.30	1.60	2.10	
			3 MHz		0.810	0.835	0.880	0.970	0.900	1.20	1.40	1.90	
			1.5 MHz		0.730	0.760	0.800	0.890	0.810	1.10	1.30	1.80	
			750 kHz		0.690	0.720	0.765	0.855	0.770	0.990	1.30	1.80	
			375 kHz		0.670	0.700	0.745	0.835	0.750	0.970	1.30	1.80	
			32 kHz		0.082	0.130	0.180	0.280	0.120	0.370	0.640	1.20	

1. Evaluated by characterization – Not tested in production.
2. V_{DD} = 3.0 V for values in Typ columns and 3.6 V for values in Max columns, all peripherals disabled.
3. Code compiled with high optimization for space in SRAM.

Table 29. Typical current consumption in Run depending on code executed

Symbol	Parameter	Conditions			Typ	Unit	Typ	Unit
		General(1)	Code	Fetch from(2)	25 °C		25 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSE_bypass}$ = 48 MHz	Reduced code(3)	Flash memory	3.40	mA	70.8	µA/MHz
			Coremark		3.15		65.6	
			Dhrystone		3.20		66.7	
			Fibonacci		2.40		50.0	
			WhileLoop		1.80		37.5	
			Reduced code(3)	SRAM	2.80		58.3	
			Coremark		2.70		56.3	
			Dhrystone		2.70		56.3	
			Fibonacci		2.85		59.4	
			WhileLoop		2.15		44.8	
		$f_{HCLK} = f_{HSE_bypass}$ = 16 MHz	Reduced code(3)	Flash memory	1.25		78.1	
			Coremark		1.15		71.9	
			Dhrystone		1.15		71.9	
			Fibonacci		0.835		52.2	
			WhileLoop		0.645		40.3	
			Reduced code(3)	SRAM	0.990		61.9	
			Coremark		0.950		59.4	
			Dhrystone		0.945		59.1	
			Fibonacci		1.00		62.5	
			WhileLoop		0.775		48.4	
		$f_{HCLK} = f_{HSE_bypass}$ = 2 MHz	Reduced code(3)	Flash memory	0.225	µA	112.5	µA/MHz
			Coremark		0.210		105.0	
			Dhrystone		0.210		105.0	
			Fibonacci		0.175		87.5	
			WhileLoop		0.150		75.0	
			Reduced code(3)	SRAM	0.195		97.5	
			Coremark		0.190		95.0	
			Dhrystone		0.190		95.0	
			Fibonacci		0.195		97.5	
			WhileLoop		0.165		82.5	

Table 29. Typical current consumption in Run depending on code executed (continued)

Symbol	Parameter	Conditions			Typ	Unit	Typ	Unit
		General[1]	Code	Fetch from[2]	25 °C		25 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK} = f_{HSI48/HSIDIV}$ = 48 MHz (HSIDIV = 1)	Reduced code[3]	Flash memory	3.75	mA	78.1	µA/MHz
			Coremark		3.50		72.9	
			Dhrystone		3.55		74.0	
			Fibonacci		2.75		57.3	
			WhileLoop		2.15		44.8	
			Reduced code[3]	SRAM	3.15		65.6	
			Coremark		3.05		63.5	
			Dhrystone		3.05		63.5	
			Fibonacci		3.20		66.7	
			WhileLoop		2.50		52.1	
		$f_{HCLK} = f_{HSI48/HSIDIV}$ = 12 MHz (HSIDIV = 4)	Reduced code[3]	Flash memory	1.45		120.8	
			Coremark		1.40		116.7	
			Dhrystone		1.40		116.7	
			Fibonacci		1.15		95.8	
			WhileLoop		1.00		83.3	
			Reduced code[3]	SRAM	1.30		108.3	
			Coremark		1.25		104.2	
			Dhrystone		1.25		104.2	
			Fibonacci		1.30		108.3	
			WhileLoop		1.10		91.7	
		$f_{HCLK} = f_{HSI48/HSIDIV}$ = 3 MHz (HSIDIV = 16)	Reduced code[3]	Flash memory	0.855	µA	285.0	µA/MHz
			Coremark		0.835		278.3	
			Dhrystone		0.835		278.3	
			Fibonacci		0.780		260.0	
			WhileLoop		0.745		248.3	
			Reduced code[3]	SRAM	0.810		270.0	
			Coremark		0.800		266.7	
			Dhrystone		0.800		266.7	
			Fibonacci		0.810		270.0	
			WhileLoop		0.770		256.7	

1. V_{DD} = 3.0 V, all peripherals disabled
2. Prefetch and cache enabled when fetching from flash
3. Reduced code used for characterization results provided in *Table 27*.

Table 30. Current consumption in Sleep mode

Symbol	Parameter	Conditions			Typ				Max(1)				Unit
		General		f_{HCLK}	25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	All peripherals disabled, $f_{HCLK} = f_{HSI48/HSIDIV}$ (> 32 kHz), $f_{HCLK} = f_{LSI}$ (= 32 kHz)	Flash memory enabled	48 MHz	1.20	1.20	1.25	1.35	1.50	1.70	2.00	2.50	mA
				24 MHz	0.92	0.95	0.99	1.10	1.10	1.30	1.60	2.10	
				12 MHz	0.79	0.81	0.86	0.95	0.91	1.20	1.40	1.90	
				6 MHz	0.72	0.75	0.79	0.88	0.82	1.10	1.30	1.80	
				1.5 MHz	0.67	0.70	0.74	0.83	0.75	0.97	1.30	1.80	
				375 kHz	0.66	0.69	0.73	0.82	0.73	0.95	1.30	1.80	
				32 kHz	0.08	0.13	0.18	0.28	0.12	0.37	0.64	1.20	
		All peripherals disabled, $f_{HCLK} = f_{HSE_bypass}$ (> 32.768 kHz), $f_{HCLK} = f_{LSE_bypass}$ (= 32.768 kHz)		48 MHz	0.820	0.875	0.930	1.05	1.20	1.40	1.70	2.20	
				32 MHz	0.575	0.630	0.680	0.785	0.800	1.10	1.40	1.90	
				24 MHz	0.450	0.500	0.555	0.655	0.630	0.880	1.20	1.70	
				16 MHz	0.325	0.380	0.430	0.535	0.460	0.710	0.980	1.50	
				8 MHz	0.205	0.250	0.305	0.405	0.300	0.540	0.820	1.40	
				2 MHz	0.110	0.160	0.210	0.310	0.170	0.420	0.690	1.20	
				500 kHz	0.0875	0.135	0.185	0.285	0.130	0.380	0.650	1.20	
				32.768 kHz	0.0805	0.125	0.180	0.280	0.120	0.370	0.640	1.20	
			Flash memory disabled (flash memory power-down sleep mode)	48 MHz	0.815	0.870	0.925	1.05	1.20	1.40	1.70	2.20	
				32 MHz	0.570	0.620	0.675	0.775	0.790	1.10	1.40	1.90	
				24 MHz	0.445	0.495	0.545	0.650	0.630	0.870	1.20	1.70	
				16 MHz	0.320	0.375	0.425	0.525	0.460	0.700	0.980	1.50	
				8 MHz	0.200	0.245	0.295	0.395	0.290	0.530	0.810	1.40	
				2 MHz	0.105	0.150	0.205	0.300	0.160	0.410	0.680	1.20	
				500 kHz	0.0815	0.130	0.180	0.280	0.120	0.370	0.650	1.20	
				32.768 kHz	0.0745	0.120	0.170	0.270	0.110	0.360	0.630	1.20	

1. Evaluated by characterization – Not tested in production.

Table 31. Current consumption in Stop mode

Symbol	Parameter	Conditions	V_{DD}	Typ				Max(1)				Unit
				25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Stop)}$	Supply current in Stop mode	All clocks off	2 V	79.0	125	175	275	110	350	610	1100	µA
			2.4 V	79.0	125	175	275	110	350	610	1100	
			3 V	80.0	125	180	275	110	350	610	1100	
			3.6 V	81.5	130	180	280	110	350	610	1100	
		All clocks off Flash memory in power-down stop mode	2 V	70.5	120	170	270	97.0	340	600	1100	
			2.4 V	72.0	120	170	270	98.0	340	600	1100	
			3 V	73.5	120	170	270	100	340	600	1100	
			3.6 V	75.0	120	175	270	110	340	600	1100	
		RTC enabled and supplied with LSE bypass (32.768 kHz)	2 V	78.0	125	175	275	110	350	610	1100	
			2.4 V	78.5	125	175	275	110	350	610	1100	
			3 V	80.0	125	180	275	110	350	610	1100	
			3.6 V	82.0	130	180	280	110	350	610	1100	
		RTC enabled and supplied with LSE bypass (32.768 kHz) Flash memory in power-down stop mode	2 V	71.0	120	170	270	97.0	340	600	1100	
			2.4 V	72.5	120	170	270	98.0	340	600	1100	
			3 V	74.0	120	170	270	100	340	600	1100	
			3.6 V	75.5	120	175	270	110	340	600	1100	
		HSI Kernel on	2 V	605	630	675	765	640	850	1100	1600	
			2.4 V	605	630	675	765	640	850	1100	1600	
			3 V	605	630	675	765	640	850	1200	1600	
			3.6 V	605	635	680	770	640	850	1200	1600	

1. Evaluated by characterization – Not tested in production.

Table 32. Current consumption in Standby mode

Symbol	Parameter	Conditions	V_{DD}	Typ				Max(1)				Unit
				25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Standby)}$	Supply current in Standby mode	All clocks off	2 V	6.75	7.70	8.55	10.5	7.50	8.90	11.0	16.0	µA
			2.4 V	7.05	8.00	8.85	11.0	7.70	9.10	11.0	17.0	
			3 V	7.45	8.45	9.45	12.0	8.20	9.70	12.0	18.0	
			3.6 V	7.90	8.95	10.0	12.5	8.70	11.0	13.0	20.0	
		IWDG enabled and clocked by LSI	2 V	7.30	8.35	9.20	11.5	8.10	9.50	12.0	17.0	
			2.4 V	7.65	8.65	9.60	11.5	8.30	9.80	12.0	17.0	
			3 V	8.10	9.20	10.0	12.5	8.90	11.0	13.0	19.0	
			3.6 V	8.60	9.75	11.0	13.5	9.50	12.0	14.0	21.0	

1. Evaluated by characterization – Not tested in production.

Table 33. Current consumption in Shutdown mode

Symbol	Parameter	Conditions	V_{DD}	Typ				Max(1)				Unit
				25 °C	85 °C	105 °C	125 °C	25 °C	85 °C	105 °C	125 °C	
$I_{DD(Shutdown)}$	Supply current in Shutdown mode	All clocks off	2 V	9.00	290	835	2350	55	920	2700	7600	nA
			2.4 V	13.0	320	915	2550	62	970	2900	7900	
			3.0 V	19.0	375	1050	2900	72	1200	3300	8900	
			3.6 V	31.0	460	1250	3350	95	1400	3800	11000	

1. Evaluated by characterization – Not tested in production.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up or pull-down resistor generate current consumption when the pin is externally held low or high, respectively. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 49: I/O static characteristics*.

For the output pins, any pull-up or pull-down device (internal and external) and external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 34: Current consumption of peripherals*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal and external) of the pin:

$$I_{SW} = V_{DDIO1} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIO1} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following table. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 20: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in the following table. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 34. Current consumption of peripherals

Peripheral	Bus	Consumption in µA/MHz
IOPORT bus	IOPORT	0.72
GPIOA		1.64
GPIOB		1.64
GPIOC		0.82
GPIOF		0.74
Bus matrix	AHB	0.31
All AHB peripherals		8
DMA1		2.64
FLASH		4.56
SRAM1		0.01
CRC1		0.48
All APB peripherals	APB	30.76
AHB to APB bridge (2)		0.32
TIM3		3.66
RTCAPB		1.13
WWDG1		0.48
USART2		2.01
I2C1		3.44
I2C1 independent clock domain		2.59
DBGMCU1		0.09
PWR		0.3
SYSCFG		0.4
TIM1		5.84

Table 34. Current consumption of peripherals (continued)

Peripheral	Bus	Consumption in µA/MHz
SPI1	APB	3.18
SPI1 independent clock domain		1.44
USART1		2.22
USART1 independent clock domain		5.77
TIM14		1.42
TIM16		2.54
TIM17		2.45
ADC1		1.92
ADC1 independent clock domain		0.12
All peripherals		43.56

5.3.6 Wake-up time from low-power modes

The wake-up times given in *Table 35* are the latency between the event and the execution of the first user instruction.

Table 35. Low-power mode wake-up times(1)

Symbol	Parameter	Conditions		Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up time from Sleep to Run mode	HCLK = HSI48/4 = 12 MHz	Transiting to Run-mode execution in flash memory powered during Sleep mode	10	12	CPU clock cycles
			Transiting to Run-mode execution in flash memory not powered during Sleep mode	4.75	5.02	µs
$t_{WULPSTOP}$	Wake-up time from Stop mode	Clock after wake-up is HCLK = HSI48/4 = 12 MHz	Transiting to Run-mode execution in flash memory powered during Stop mode	2.7	3.1	µs
			Transiting to Run-mode execution in flash memory not powered during Stop mode	5.9	6.4	
			Transiting to Run-mode execution in SRAM	2.5	2.9	
t_{WUSTBY}	Wake-up time from Standby mode	Clock after wake-up is HCLK = HSI48/4 = 12 MHz	Transiting to Run mode	23	35	
t_{WUSHDN}	Wake-up time from Shutdown mode	Clock after wake-up is HCLK = HSI48/4 = 12 MHz	Transiting to Run mode	385	466	

1. Evaluated by characterization – Not tested in production.

5.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

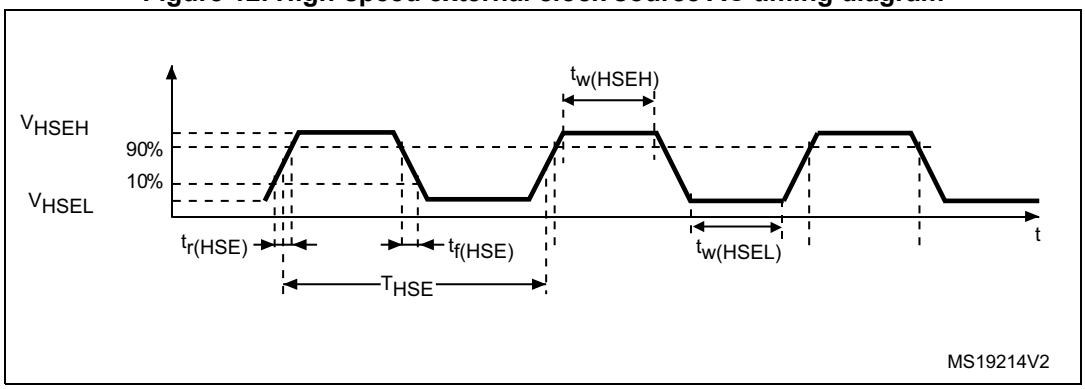
The external clock signal has to respect the I/O characteristics in *Section 5.3.13*. See *Figure 12* for recommended clock input waveform.

Table 36. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	-	8	48	MHz
V_{HSEH}	Digital OSC_IN input pin high level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}$/ $t_{w(HSEL)}$	Digital OSC_IN high or low time	-	7	-	-	ns

1. Specified by design – Not tested in production.

Figure 12. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 5.3.13*. See *Figure 13* for recommended clock input waveform.

Table 37. Low-speed external user clock characteristics(1)

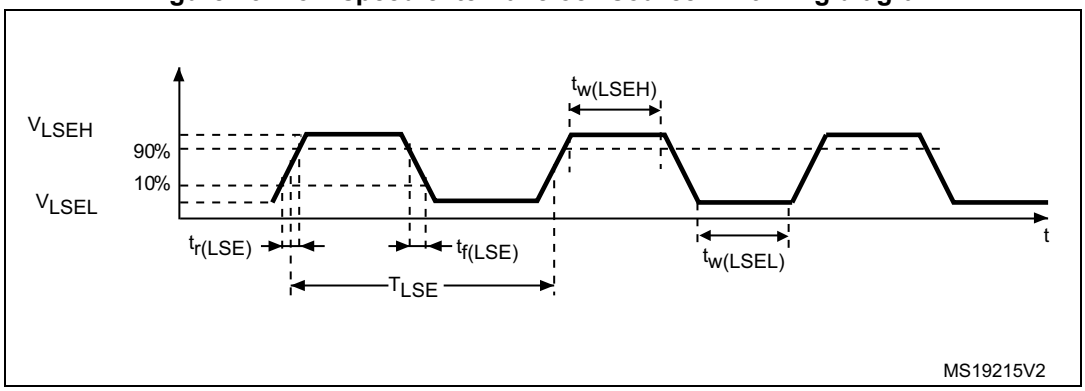
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz

Table 37. Low-speed external user clock characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIO1}	-	V_{DDIO1}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIO1}	
$t_{w(LSEH)}$/ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Specified by design – Not tested in production.

Figure 13. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 38*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 38. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ

Table 38. HSE oscillator characteristics(1) (continued)

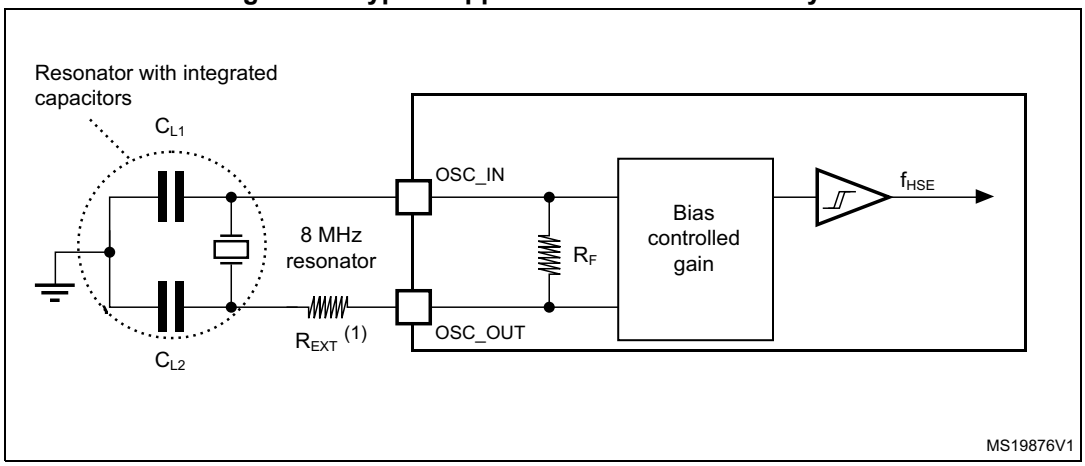
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.58	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.59	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.89	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	1.14	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.94	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Specified by design – Not tested in production.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 39*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

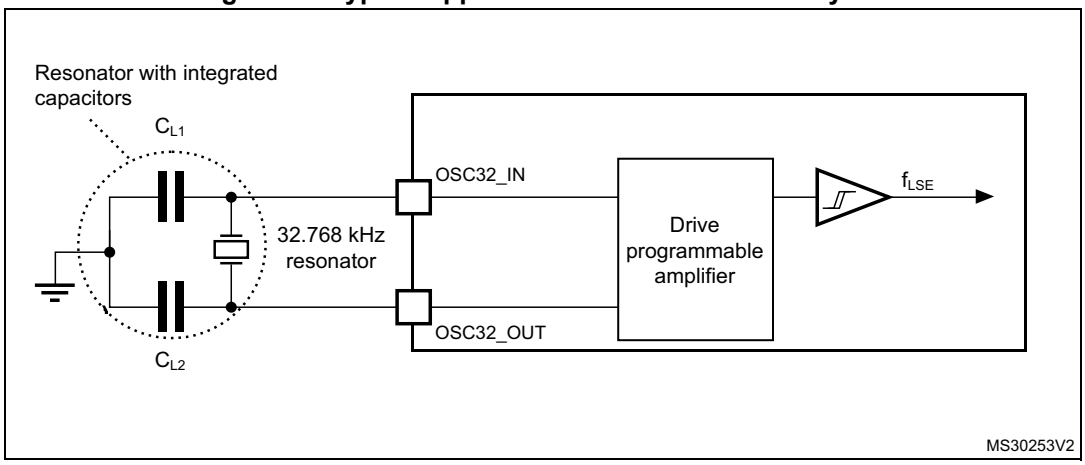
Table 39. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV = 0 Medium high drive capability	-	500	-	nA
		LSEDRV = 1 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV = 0 Medium high drive capability	-	-	1.7	µA/V
		LSEDRV = 1 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Specified by design – Not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 15. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

5.3.8 Internal clock source characteristics

The parameters given in *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*. The provided curves are characterization results, not tested in production.

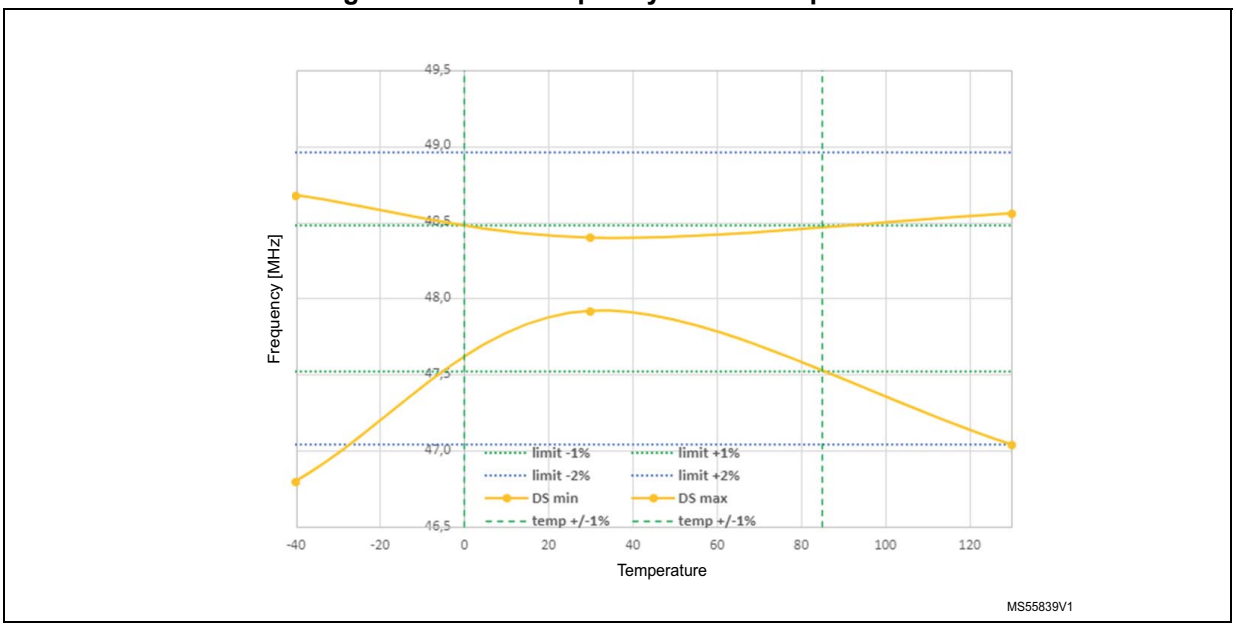
High-speed internal (HSI48) RC oscillator

Table 40. HSI48 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0 V, T_A=30 °C	47.92	-	48.40	MHz
$\Delta_{Temp(HSI)}$(1)	HSI48 oscillator frequency drift over temperature and V_{DD} full voltage range	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2.5	-	2	%
TRIM(1)	HSI48 oscillator frequency user trimming step	From code 127 to 128	-8	-6	-4	%
		From code 63 to 64 From code 191 to 192	-5.8	-3.8	-1.8	
		For all other code increments	0.2	0.3	0.4	
D_{HSI48}(2)	Duty cycle	-	45	-	55	%
$t_{su(HSI48)}$(2)	HSI48 oscillator start-up time	-	-	1.4	1.8	µs
$t_{stab(HSI48)}$(2)	HSI48 oscillator stabilization time	at 1% of target frequency	-	1.5	3.6	µs
$I_{DD(HSI48)}$(1)	HSI48 oscillator power consumption	-	-	525	570	µA

1. Based on characterization results, not tested in production
2. Specified by design – Not tested in production.

Figure 16. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI frequency	V_{DD} = 3.3 V, T_A = 25 °C	31.04	32	32.96	kHz
		V_{DD} = 2 V to 3.6 V, T_A = -40 to 125 °C	29.5 (1)	-	34(1)	
$t_{SU(LSI)}$(2)	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB(LSI)}$(2)	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	-	110	180	nA

1. Evaluated by characterization – Not tested in production.
2. Specified by design – Not tested in production.

5.3.9 flash memory characteristics

Table 42. Flash memory characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	Word programming time	64 bits	-	85.0	125.0	µs
t_{prog_row}	Row (32 double word) programming time	Normal programming	-	2.7	4.6	ms
		Fast programming	-	1.7	2.8	
t_{prog_page}	Page (2 Kbyte) programming time	Normal programming	-	21.8	36.6	
		Fast programming	-	13.7	22.4	
t_{ERASE}	Page (2 Kbyte) erase time	-	-	22.0	40.0	

Table 42. Flash memory characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog_bank}	Bank (32 Kbyte(2)) programming time	Normal programming	-	0.4	0.6	s
		Fast programming	-	0.2	0.4	
t_{ME}	Mass erase time	-	-	22.1	40.1	ms
$I_{DD(FlashA)}$	Average consumption from V_{DD}	Programming	-	3.0	-	mA
		Page erase	-	3.0	-	
		Mass erase	-	5.0	-	
$I_{DD(FlashP)}$	Maximum current (peak)	Programming, 2 µs peak duration	-	7.0	-	mA
		Erase, 41 µs peak duration	-	7.0	-	

1. Specified by design – Not tested in production.
2. Values provided also apply to devices with less flash memory than one 32 Kbyte bank

Table 43. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_J = -40 to +130 °C	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	15	
		1 kcycle(2) at T_A = 125 °C	7	
		10 kcycles(2) at T_A = 55 °C	30	
		10 kcycles(2) at T_A = 85 °C	15	
		10 kcycles(2) at T_A = 105 °C	10	

1. Evaluated by characterization – Not tested in production..
2. Cycling performed over the whole temperature range.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 44*. They are based on the EMS levels and classes defined in application note AN1709.

Table 44. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, $f_{HSE} = f_{HCLK}$ = 48 MHz, LQFP48, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, $f_{HSE} = f_{HCLK}$ = 48 MHz, LQFP48, conforming to IEC 61000-4-2	4B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- corrupted program counter
- unexpected reset
- critical data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

The following table gives the EMI characteristics for f_{HSI48} and f_{HCLK} of 48 MHz.

Table 45. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Max vs. [f_{HSI}/f_{CPU}]	Unit
				48 MHz / 48 MHz	48 MHz / 48 MHz	
S_{EMI}	Peak(1)	V_{DD} = 3.6 V, T_A = 25 °C, LQFP48 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	3	3	dBµV
			30 MHz to 130 MHz	5	-2	
			130 MHz to 1 GHz	1	-1	
			1 GHz to 2 GHz	7	8	
	Level(2)		0.1 MHz to 2 GHz	2	2	-

1. Refer to AN1709, section *EMI radiated test*
2. Refer to AN1709, section *EMI level classification*

5.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 46. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Package	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	All	1C	-2000/+1500	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-002	All	C2a	500	

1. Evaluated by characterization – Not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current is injected to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 47. Electrical sensitivity

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78	II Level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIO1} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter: ADC error above a certain limit (higher than 5 LSB TUE), induced leakage current on adjacent pins out of conventional limits (-5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 48. I/O current injection susceptibility(1)

Symbol	Description		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}(2)	Injected current on pin	Any IO	5	NA	mA

1. Evaluated by characterization – Not tested in production.
2. The injection current value is applicable when the switchable diode is activated, NA when not activated.

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under the conditions summarized in *Table 23: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

For information on GPIO configuration, refer to the application note AN4899 *STM32 GPIO configuration for hardware settings and low-power consumption*, available on the ST website www.st.com.

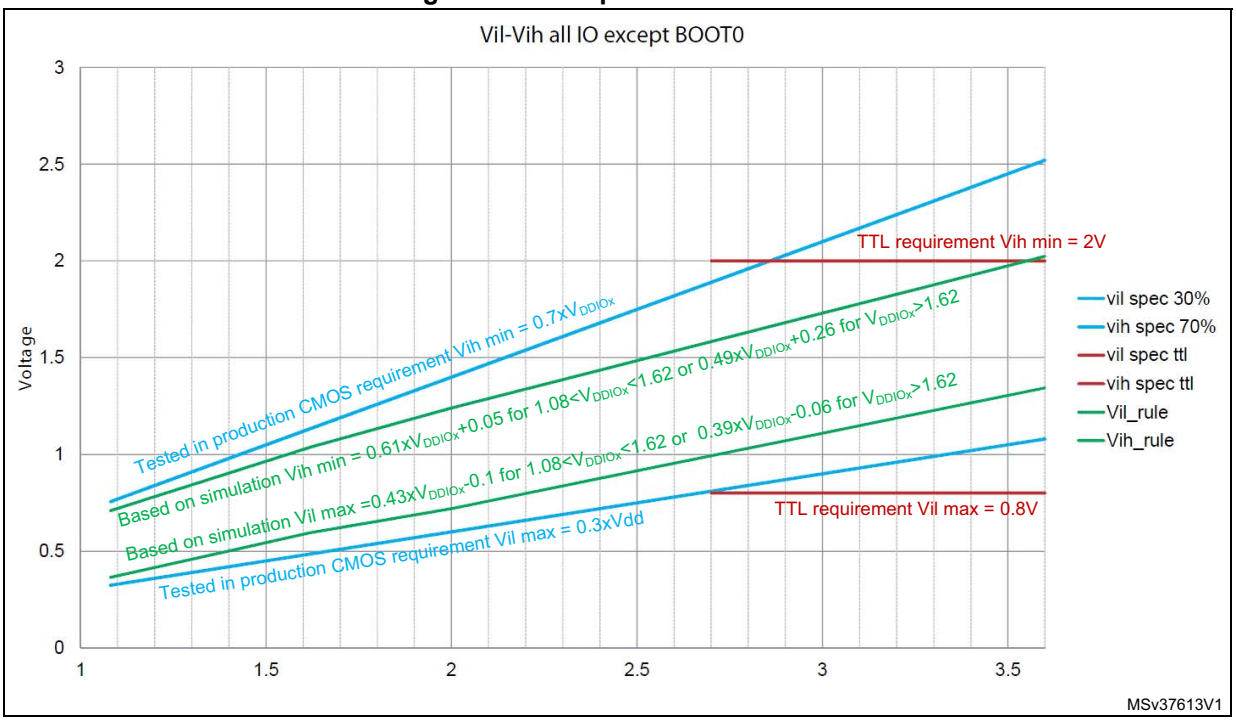
Table 49. I/O static characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage	All	2 V < V_{DDIO1} < 3.6 V	-	-	0.3 x V_{DDIO1}	V
V_{IH}(1)	I/O input high level voltage	All	2 V < V_{DDIO1} < 3.6 V	0.7 x V_{DDIO1}	-	-	V
V_{hys}(2)	I/O input hysteresis	-		-	200	-	mV
I_{lkg}(3)	Input leakage current(3)	0 < V_{IN} ≤ V_{DDIO1}		-	-70	-	nA
		V_{DDIO1} ≤ V_{IN} ≤ V_{DDIO1} +1 V		-	600	-	
		V_{DDIO1} +1 V ≤ V_{IN}		-	150	-	
R_{PU}	Weak pull-up equivalent resistor (4)	V_{IN} = V_{SS}		25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	V_{IN} = V_{DDIO1}		25	40	55	kΩ
C_{IO}	I/O pin capacitance	-		-	5	-	pF

1. Refer to *Figure 17: I/O input characteristics*.
2. Specified by design – Not tested in production.
3. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: ITotal_Ileak_max = 10 µA + [number of I/Os where VIN is applied on the pad] x Ilkg(Max).
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters, as shown in *Figure 17*.

Figure 17. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±6 mA, and up to ±15 mA with relaxed V_{OL}/V_{OH}.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIO1}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 20: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 20: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 50. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DD} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage		V_{DD} - 0.4	-	
V_{OL}(3)	Output low level voltage	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DD} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage		2.4	-	
V_{OL}(3)	Output low level voltage	All I/Os $\|I_{IO}\|$ = 20 mA $V_{DD} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage		V_{DD}- 1.3	-	
V_{OL}(3)	Output low level voltage	$\|I_{IO}\|$ = 4 mA $V_{DD} \geq 2.0$ V	-	0.45	
V_{OH}(3)	Output high level voltage		V_{DD} - 0.45	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode	$\|I_{IO}\|$ = 20 mA $V_{DD} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DD} \geq 2.0$ V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 20: Voltage characteristics* . The sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\sum I_{IO}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Specified by design – Not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 18* and *Table 51*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 51. I/O AC characteristics(1)(2)

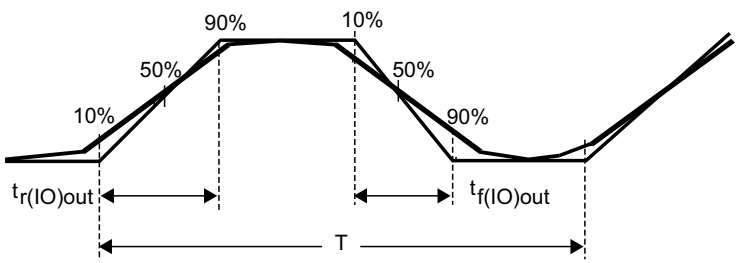
Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2	MHz
			C=50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	0.35	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.00	
			C=10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	0.45	
	Tr/Tf	Output rise and fall time(3)	C=50 pF,2.7 V ≤ V_{DD} ≤ 3.6 V	-	100.00	ns
			C=50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	225.00	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	75.00	
			C=10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	150.00	

Table 51. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	10.00	MHz
			C=50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	2.00	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	15.00	
			C=10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	2.50	
	Tr/Tf	Output rise and fall time(3)	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	30.00	ns
			C=50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	60.00	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	15.00	
			C=10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	30.00	
10	Fmax	Maximum frequency	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	30.00	MHz
			C=50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	15.00	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	60.00(4)	
			C=10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	30.00	
	Tr/Tf	Output rise and fall time(3)	C=50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	11.00	ns
			C=50 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	22.00	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.00	
			C=10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	8.00	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	60.00(4)	MHz
			C=30 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	30.00	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	80.00(4)	
			C=10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	40.00	
	Tr/Tf	Output rise and fall time(3)	C=30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.50	ns
			C=30 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	11.00	
			C=10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.50	
			C=10 pF, 2 V ≤ V_{DD} ≤ 2.7 V	-	5.00	

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0490 reference manual for a description of GPIO Port configuration register.
2. Specified by design – Not tested in production.
3. The fall time is defined between 70% and 30% of the output waveform, according to I^2C specification.
4. This value represents the I/O capability but the maximum system frequency is limited to 48 MHz.

Figure 18. I/O AC characteristics definition(1)



Maximum frequency is achieved with a duty cycle at (45 - 55%) when loaded by the specified capacitance.

1. Refer to *Table 51: I/O AC characteristics*.

5.3.14 NRST input characteristics

The NRST input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

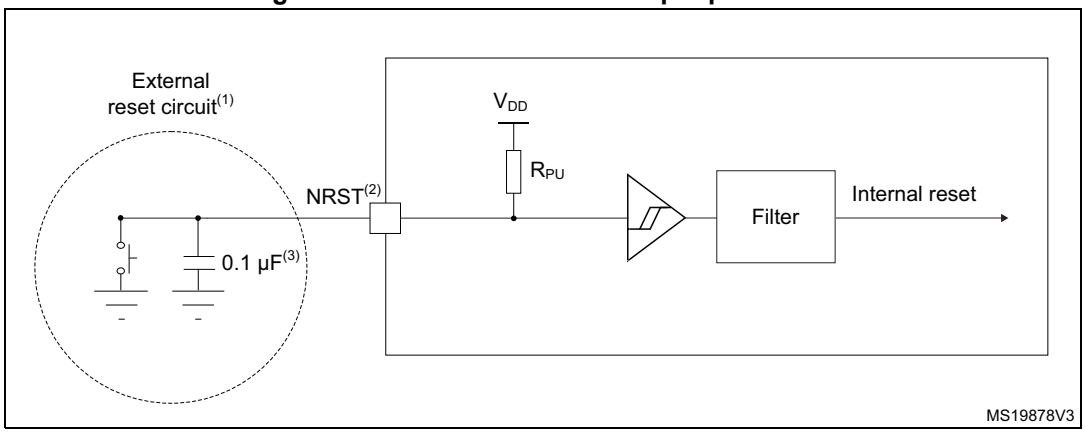
Unless otherwise specified, the parameters given in the following table are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 52. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.7 x V_{DD}	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}(1)	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$ (1)	NRST input filtered pulse	2.0 V < V_{DD} < 3.6 V	-	-	70	ns
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	2.0 V < V_{DD} < 3.6 V	350	-	-	ns

1. Specified by design – Not tested in production..
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 19. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that, upon power-on, the level on the NRST pin can exceed the minimum $V_{IH(NRST)}$ level specified in *Table 52: NRST pin characteristics*. Otherwise, the device does not exit the power-on reset. This applies to any NRST configuration set through the NRST_MODE[1:0] bitfield, the GPIO mode inclusive.
3. The external capacitor on NRST must be placed as close as possible to the device.

5.3.15 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in *Table 53* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 23: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 53. ADC characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.0	-	3.6	V
V_{REF+}	Positive reference voltage	-	2	-	V_{DD}	V
f_{ADC}	ADC clock frequency	-	0.14	-	35	MHz
f_s	Sampling rate	12 bits	-	-	2.50	MSps
		10 bits	-	-	2.92	
		8 bits	-	-	3.50	
		6 bits	-	-	4.38	
f_{TRIG}	External trigger frequency	f_{ADC} = 35 MHz; 12 bits	-	-	2.33	MHz
		12 bits	-	-	f_{ADC}/15	
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}(2)	V
R_{AIN}	External input impedance	-	-	-	50	kΩ

Table 53. ADC characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	ADC power-up time	LDO already started	2			Conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 35 MHz	2.35			µs
		-	82			$1/f_{ADC}$
t_{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	2	-	3	$1/f_{ADC}$
		CKMODE = 01	6.5			$1/f_{PCLK}$
		CKMODE = 10	12.5			
		CKMODE = 11	3.5			
t_s	Sampling time	f_{ADC} = 35 MHz	0.043	-	4.59	µs
			1.5	-	160.5	$1/f_{ADC}$
$t_{ADCVREG_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 35 MHz Resolution = 12 bits	0.40	-	4.95	µs
		Resolution = 12 bits	t_s + 12.5 cycles for successive approximation = 14 to 173			$1/f_{ADC}$
t_{IDLE}	Laps of time allowed between two conversions without rearm	-	-	-	100	µs
$I_{DDA(ADC)}$	ADC consumption from V_{DDA}	f_s = 2.5 MSps	-	410	-	µA
		f_s = 1 MSps	-	164	-	
		f_s = 10 kSps	-	17	-	
$I_{DDV(ADC)}$	ADC consumption from V_{REF+}	f_s = 2.5 MSps	-	65	-	µA
		f_s = 1 MSps	-	26	-	
		f_s = 10 kSps	-	0.26	-	

1. Specified by design – Not tested in production.
2. V_{REF+} is internally connected to V_{DDA} on some packages.Refer to *Section 4: Pinouts, pin description and alternate functions* for further details.

Table 54. Maximum ADC R_{AIN}

Resolution	Sampling cycle at 35 MHz	Sampling time at 35 MHz [ns]	Max. R_{AIN}(1) (Ω)
12 bits	1.5	43	50
	3.5	100	680
	7.5	214	2200
	12.5	357	4700
	19.5	557	8200
	39.5	1129	15000
	79.5	2271	33000
	160.5	4586	50000
10 bits	1.5	43	68
	3.5	100	820
	7.5	214	3300
	12.5	357	5600
	19.5	557	10000
	39.5	1129	22000
	79.5	2271	39000
	160.5	4586	50000
8 bits	1.5	43	82
	3.5	100	1500
	7.5	214	3900
	12.5	357	6800
	19.5	557	12000
	39.5	1129	27000
	79.5	2271	50000
	160.5	4586	50000
6 bits	1.5	43	390
	3.5	100	2200
	7.5	214	5600
	12.5	357	10000
	19.5	557	15000
	39.5	1129	33000
	79.5	2271	50000
	160.5	4586	50000

1. Specified by design – Not tested in production.

Table 55. ADC accuracy(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, $T_A = 25$°C	-	±3	±4	LSB
		$2\text{ V} < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, T_A = entire range	-	±3	±6.5	
EO	Offset error	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, $T_A = 25$°C	-	±1.5	±2	
		$2\text{ V} < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, T_A = entire range	-	±1.5	±4.5	
EG	Gain error	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, $T_A = 25$ °C	-	±3	±3.5	
		$2\text{ V} < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, T_A = entire range	-	±3	±5	
ED	Differential linearity error	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, $T_A = 25$ °C	-	±1.2	±1.5	
		$2\text{ V} < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, T_A = entire range	-	±1.2	±1.5	
EL	Integral linearity error	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, $T_A = 25$ °C	-	±2.5	±3	
		$2\text{ V} < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, T_A = entire range	-	±2.5	±3	
ENOB	Effective number of bits	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, $T_A = 25$ °C	10.1	10.2	-	bit
		$2\text{ V} < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, T_A = entire range	9.6	10.2	-	
SINAD	Signal-to-noise and distortion ratio	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, $T_A = 25$ °C	62.5	63	-	dB
		$2\text{ V} < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, T_A = entire range	59.5	63	-	
SNR	Signal-to-noise ratio	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, $T_A = 25$ °C	63	64	-	dB
		$2\text{ V} < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, T_A = entire range	60	64	-	
THD	Total harmonic distortion	$V_{DDA} = V_{REF+} = 3$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, $T_A = 25$ °C	-	-74	-73	dB
		$2\text{ V} < V_{DDA} = V_{REF+} < 3.6$ V $f_{ADC} = 35$ MHz, $f_s \leq 2.5$ Msps, T_A = entire range	-	-74	-70	

1. Evaluated by characterization – Not tested in production.
2. ADC DC accuracy values are measured after internal calibration.

Figure 20. ADC accuracy characteristics

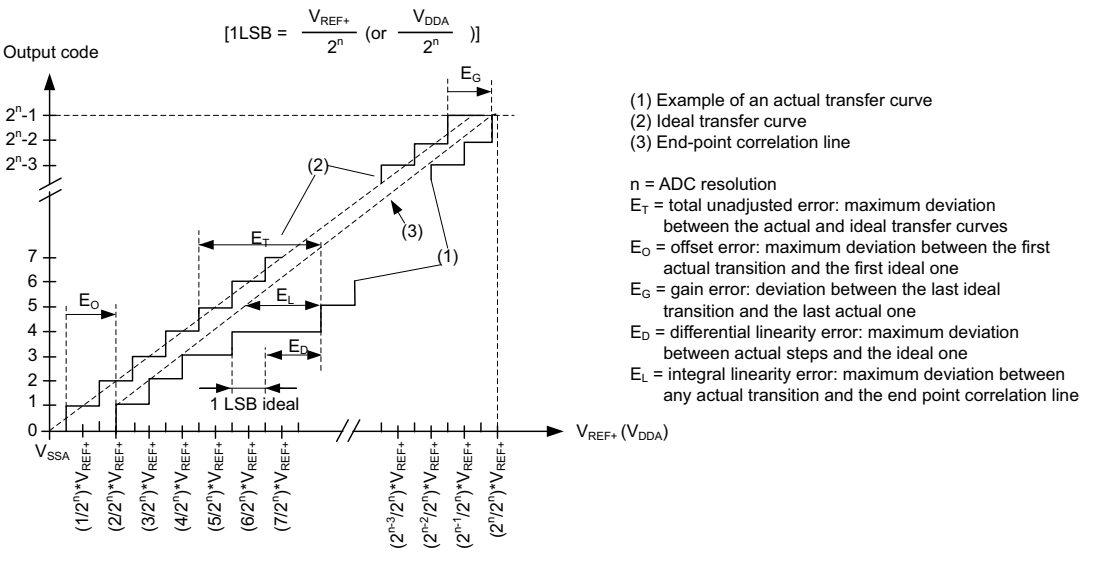
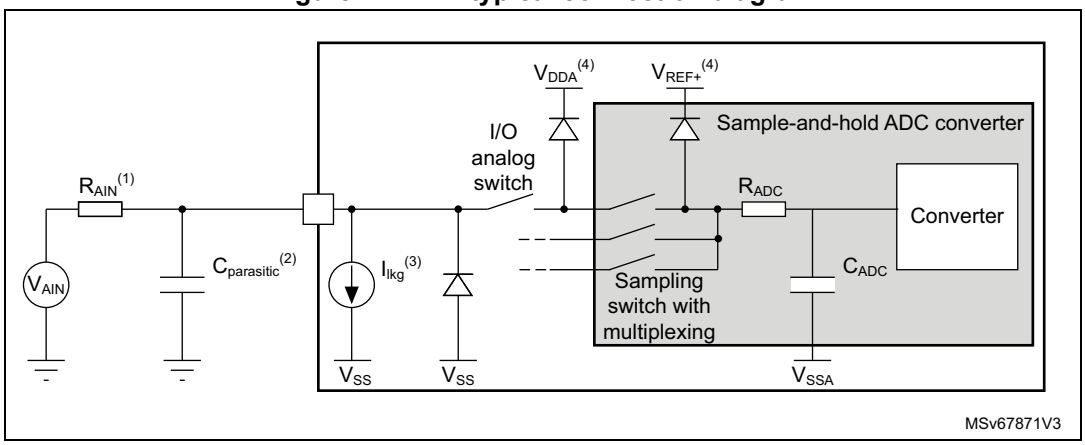


Figure 21. ADC typical connection diagram



1. Refer to *Table 53: ADC characteristics* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 49: I/O static characteristics* for the value of the pad capacitance). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
3. Refer to *Table 49: I/O static characteristics* for the values of I_{lkg}.
4. Refer to *Figure 2: Power supply overview*.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 9: Power supply scheme*. The 100 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

5.3.16 Temperature sensor characteristics

Table 56. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±5	°C
Avg_Slope(2)	Average slope from V_{SENSE} voltage	2.4	2.53	2.65	mV/°C
V_{30} (3)	Voltage at 30°C (±5 °C)	0.742	0.76	0.786	V
$t_{START(TS_BUF)}$ (1)	Sensor Buffer Start-up time in continuous mode	-	8	15	µs
t_{START} (1)	Start-up time when entering in continuous mode	-	8	120	
t_{S_temp} (1)	ADC sampling time when reading the temperature	5	-	-	
i_{sens} (1)	Temperature sensor consumption from VDD, when selected by ADC	-	4.7	7.0	µA

1. Specified by design – Not tested in production.
2. Evaluated by characterization – Not tested in production.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte.

5.3.17 Timer characteristics

The parameters given in the following tables are specified by design. Refer to *Section 5.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 57. TIMx(1) (2)characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.833	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/4$	MHz
Res_{TIM}	Timer resolution	TIMx	-	16	bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
t_{MAX_COUNT}	Maximum possible count with 16-bit counter	-	-	65536	$t_{TIMxCLK}$

1. TIMx, is used as a general term to refer to a timer (for example, TIM1).
2. Specified by design – Not tested in production.

Table 58. IWDG min/max timeout period at 32 kHz LSI clock(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings further depend on the phase of the APB interface clock versus the LSI clock, which causes an uncertainty of one RC period.

5.3.18 Characteristics of communication interfaces

I²C-bus interface characteristics

The I²C-bus interface meets timing requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The timings are specified by design as long as the I2C peripheral is properly configured (refer to the reference manual RM0490) and when the I2CCLK frequency is greater than the minimum shown in the following table.

Table 59. Minimum I2CCLK frequency

Symbol	Parameter	Condition		Typ	Unit
$f_{I2CCLK(min)}$	Minimum I2CCLK frequency for correct operation of I2C peripheral	Standard-mode		2	MHz
		Fast-mode	Analog filter enabled	9	
			DNF = 0		
			Analog filter disabled	9	
			DNF = 1		
		Fast-mode Plus	Analog filter enabled	19	
			DNF = 0		
			Analog filter disabled	16	
			DNF = 1		

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIO1} is disabled, but is still present. Only FT_f I/O pins

support Fm+ low-level output current maximum requirement. Refer to *Section 5.3.13: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the following table for its characteristics:

Table 60. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Limiting duration of spikes suppressed by the filter(2)	50	260	ns

1. Specified by design – Not tested in production.
2. Spikes shorter than the limiting duration are suppressed.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 61* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 23: General operating conditions*. The additional general conditions are:

- OSPEEDRy[1:0] set to 11 (output speed)
- capacitive load C = 30 pF
- measurement points at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 61. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode 2. V < V_{DD} < 3.6 V	-	-	24	MHz
		Master transmitter mode 2. V < V_{DD} < 3.6 V			24	
		Slave receiver mode			24	
		Slave transmitter mode/full duplex(2) 2.7 V < V_{DD} < 3.6 V			24	
		Slave transmitter mode/full duplex(2) 2 V < V_{DD} < 3.6 V			22	
$t_{su(NSS)}$	NSS setup time	Slave mode	4 * T_{PCLK}	-	-	ns
$t_{h(NSS)}$	NSS hold time		2 * T_{PCLK}	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PCLK} - 1	T_{PCLK}	T_{PCLK} + 1	ns
-	SCK low time	Master mode	T_{PCLK} - 2	T_{PCLK}	T_{PCLK} + 2	ns
$t_{su(MI)}$	Data input setup time	Master mode	4.5	-	-	ns
$t_{su(SI)}$		Slave mode	2	-	-	ns

Table 61. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(MI)}$	Data input hold time	Master mode	2	-	-	ns
$t_{h(SI)}$		Slave mode	3	-	-	ns
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V	-	10	16	ns
		Slave mode 2 V < V_{DD} < 3.6 V	-	10	22	
$t_{v(MO)}$		Master mode	-	3	5.5	ns
$t_{h(SO)}$	Data output hold time	Slave mode 2 V < V_{DD} < 3.6 V	8	-	-	ns
$t_{h(MO)}$		Master mode	1.5	-	-	ns

1. Evaluated by characterization – Not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 22. SPI timing diagram - slave mode and CPHA = 0

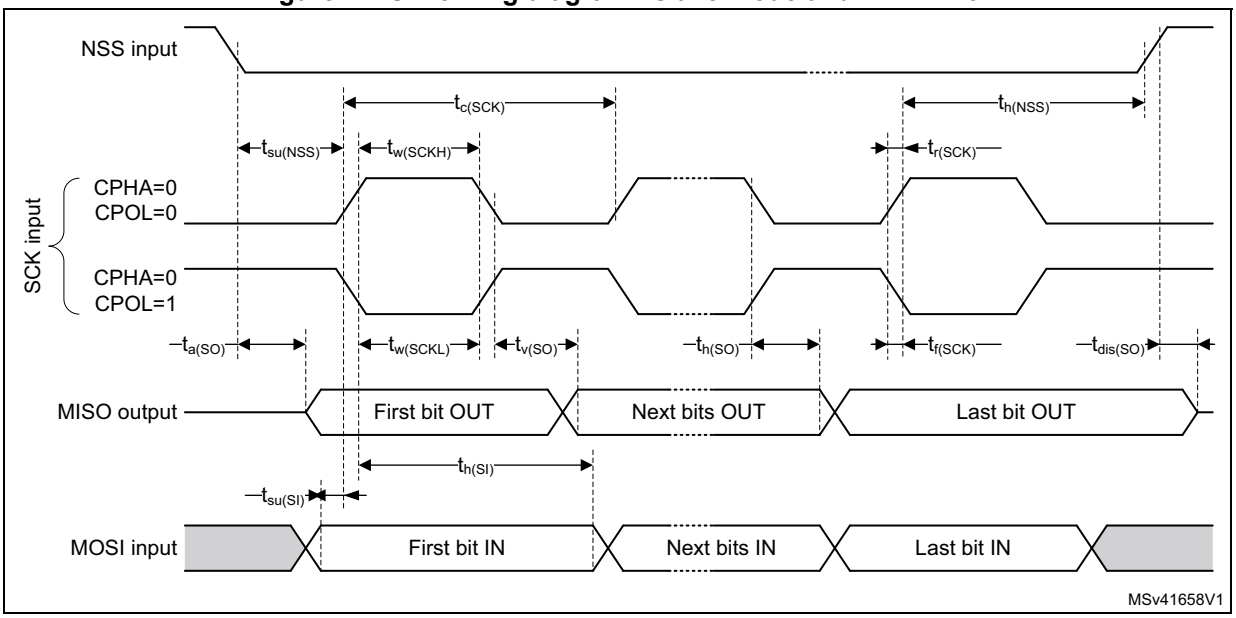
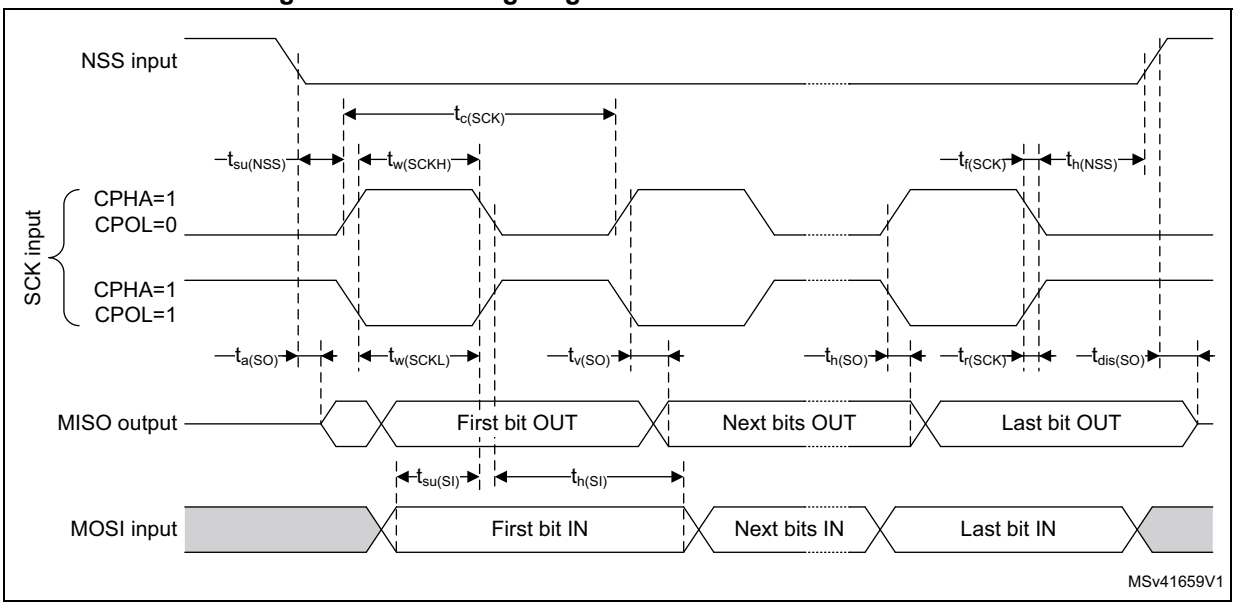
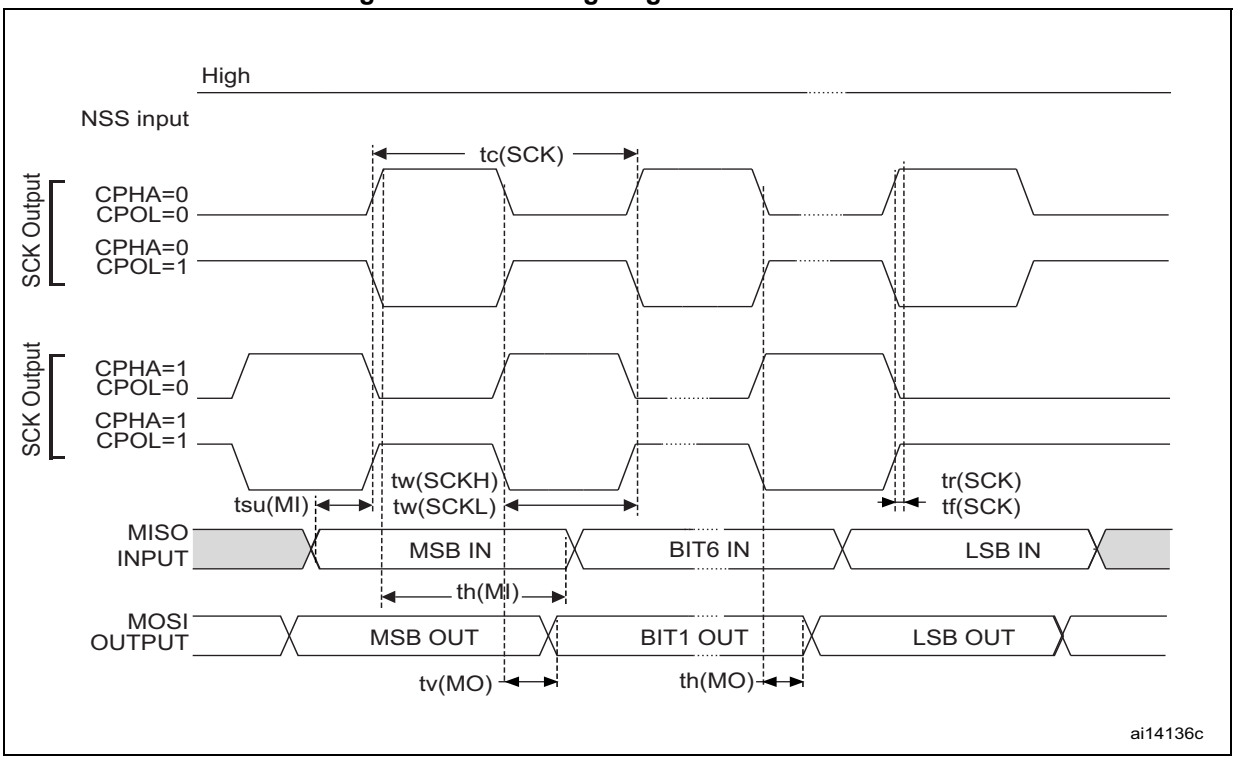


Figure 23. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at 0.5 V_{DD} and with external C_L = 30 pF.

Figure 24. SPI timing diagram - master mode



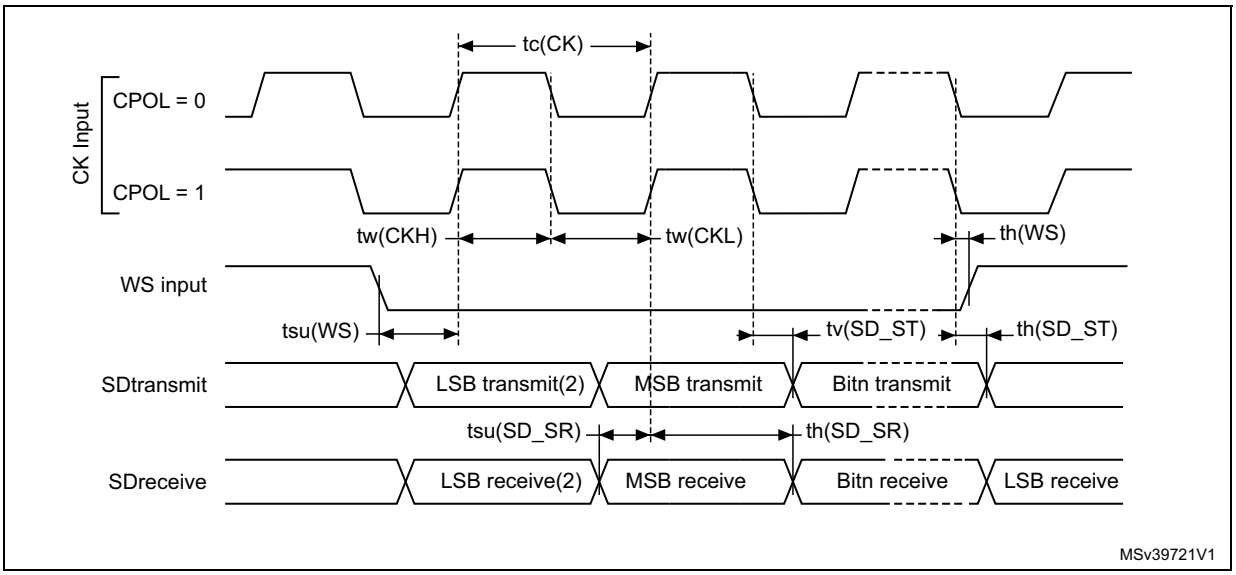
1. Measurement points are done at 0.5 V_{DD} and with external C_L = 30 pF.

Table 62. I²S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	-	-	48	MHz
f_{CK}	I2S clock frequency	Master TX	-	12	MHz
		Master RX	-	12	
		Slave TX	-	15	
		Slave RX	-	48	
$t_{v(WS)}$	WS valid time	Master mode	-	5	ns
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	3.5	-	
$t_{h(WS)}$	WS hold time	Slave mode	1	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	5	-	
$t_{su(SD_SR)}$		Slave receiver	2.5	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	1.5	-	ns
$t_{h(SD_SR)}$		Slave receiver	1	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	19,5	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	5	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	2.5	-	

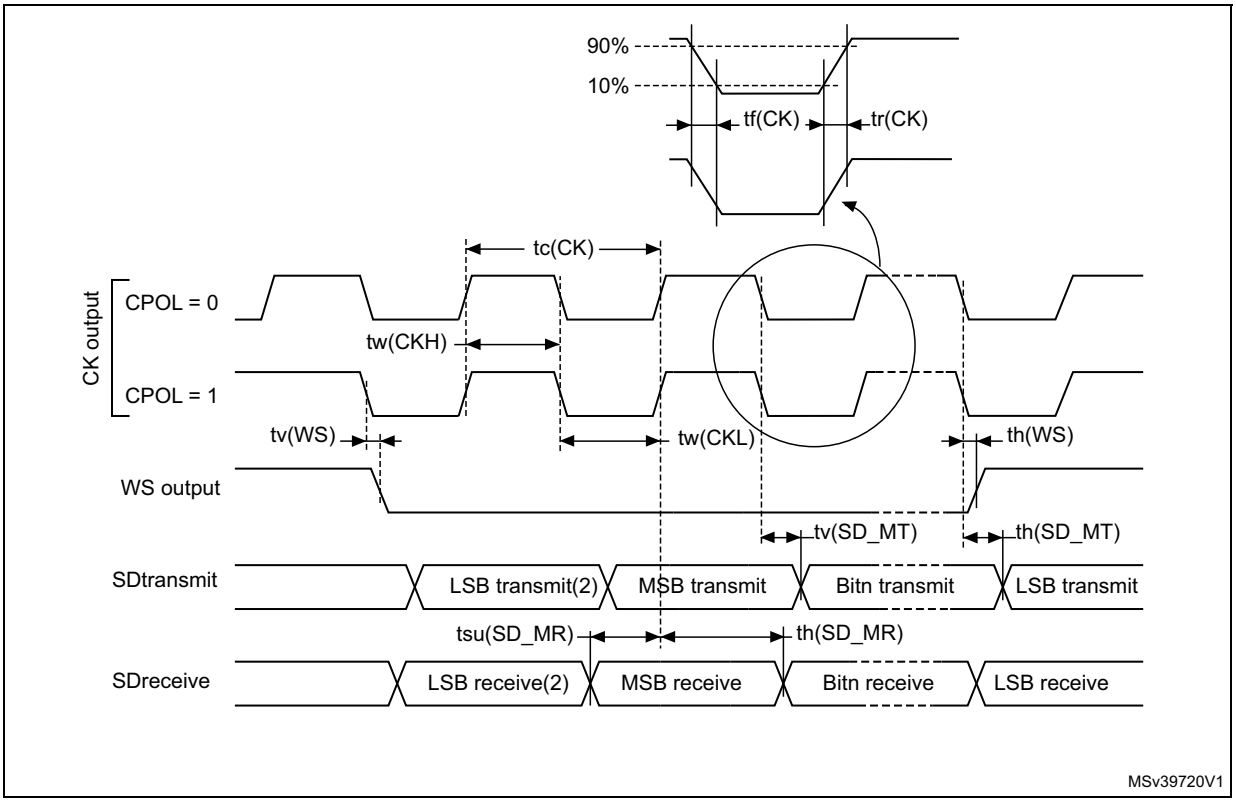
1. Evaluated by characterization – Not tested in production.

Figure 25. I²S slave timing diagram (Philips protocol)



1. Measurement points are done at CMOS levels: 0.3 V_{DDIO1} and 0.7 V_{DDIO1}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 26. I²S master timing diagram (Philips protocol)



1. Evaluated by characterization – Not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USART (SPI mode) characteristics

Unless otherwise specified, the parameters given in *Table 63* for USART are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 23: General operating conditions*. The additional general conditions are:

- OSPEEDRy[1:0] set to 10 (output speed)
- capacitive load C = 30 pF
- measurement points at CMOS levels: 0.5 x V_{DD}

Refer to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, and RX for USART).

Table 63. USART (SPI mode) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	6.0	MHz
		Slave receiver mode	-	-	16.0	
		Slave transmitter	-	-	16.0	
$t_{su(NSS)}$	NSS setup time	Slave mode	T_{ker}(1) + 1	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	
$t_{w(CKH)}$	CK high time	Master mode	1 / f_{CK} / 2 - 1	1 / f_{CK} / 2	1 / f_{CK} / 2 + 1	
$t_{w(CKL)}$	CK low time					
$t_{su(MI)}$	Data input setup time	Master mode	16	-	-	
$t_{su(SI)}$		Slave mode	1.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	0	-	-	
$t_{h(SI)}$		Slave mode	0	-	-	
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < VDD < 3.6 V	-	12.0	19	
		Slave mode 2.0 V < VDD < 3.6 V	-	12.0	13	
$t_{v(MO)}$		Master mode	-	2.0	4	
$t_{h(SO)}$	Data output hold time	Slave mode	9.5	-	-	
$t_{h(SO)}$		Master mode	0.5	-	-	

1. T_{ker} is the *usart_ker_ck_pres* clock period

Figure 27. USART timing diagram in SPI master mode

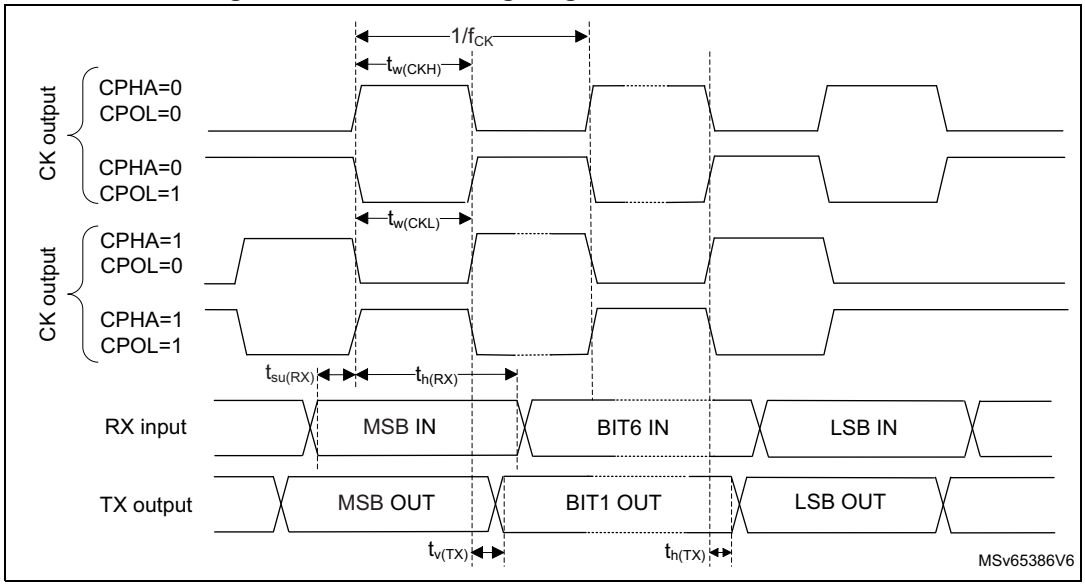
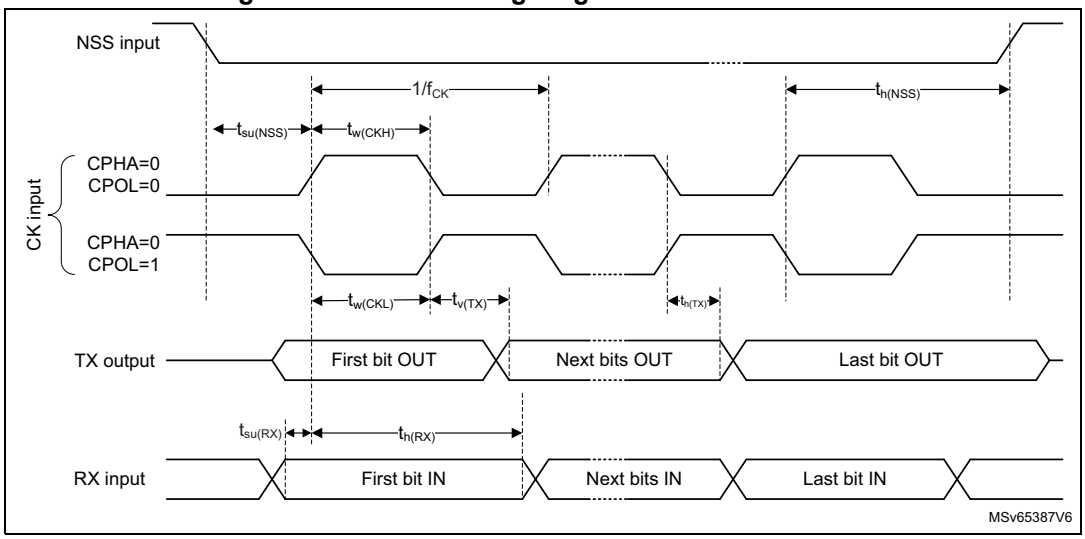


Figure 28. USART timing diagram in SPI slave mode



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 Device marking

Refer to technical note “Reference device marking schematics for STM32 microcontrollers and microprocessors” (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

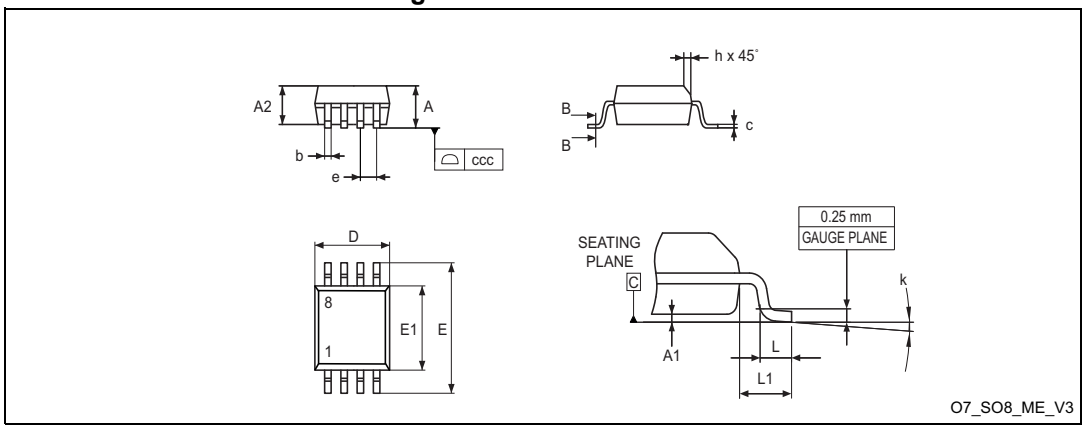
Parts marked as “ES”, “E” or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

6.2 SO8N package information (O7)

This SO8N is an 8-lead, 4.9 x 6 mm, plastic small outline, 150 mils body width, package.

Figure 29. SO8N -Outline



1. Drawing is not to scale.

Table 64. SO8N -Mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.750	-	-	0.0689
A1	0.100	-	0.250	0.0039	-	0.0098

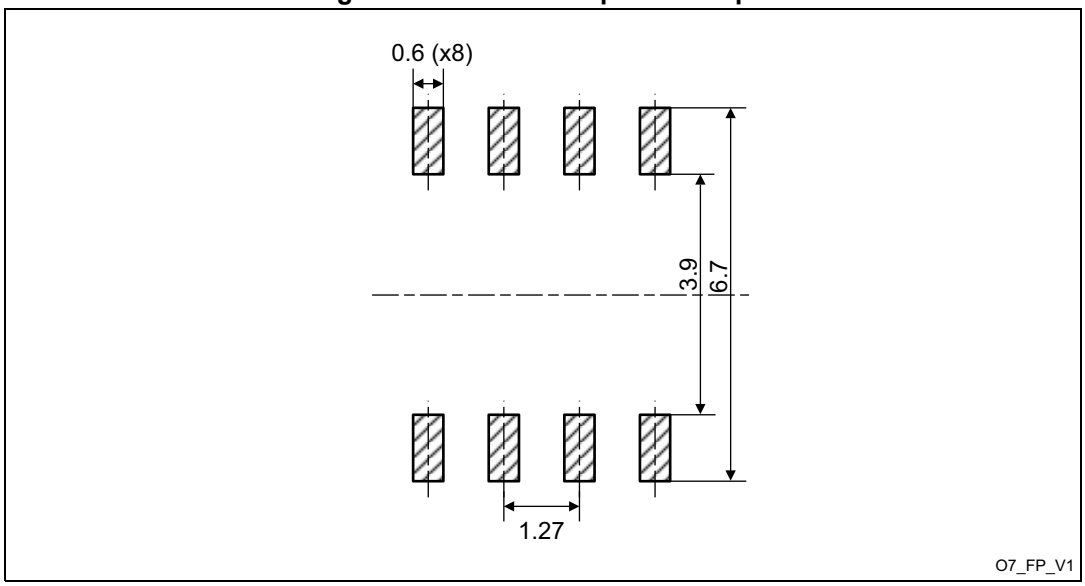
Table 64. SO8N -Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A2	1.250	-	-	0.0492	-	-
b	0.280	-	0.480	0.0110	-	0.0189
c	0.100	-	0.230	0.0039	-	0.0091
D[2]	4.800	4.900	5.000	0.1890	0.1929	0.1969
E	5.800	6.000	6.200	0.2283	0.2362	0.2441
E1[3]	3.800	3.900	4.000	0.1496	0.1535	0.1575
e	-	1.270	-	-	0.0500	-
h	0.250	-	0.500	0.0098	-	0.0197
k	0°	-	8°	0°	-	8°
L	0.400	-	1.270	0.0157	-	0.0500
L1	-	1.040	-	-	0.0409	-
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
   Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side
3. Dimension “E1” does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25 mm per side.

Note: The package top may be smaller than the package bottom. Dimensions D and E1 are determinated at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interleads flash, but including any mismatch between the top and bottom of plastic body. Measurement side for mold flash, protusions or gate burrs is bottom side.

Figure 30. SO8N - Footprint example

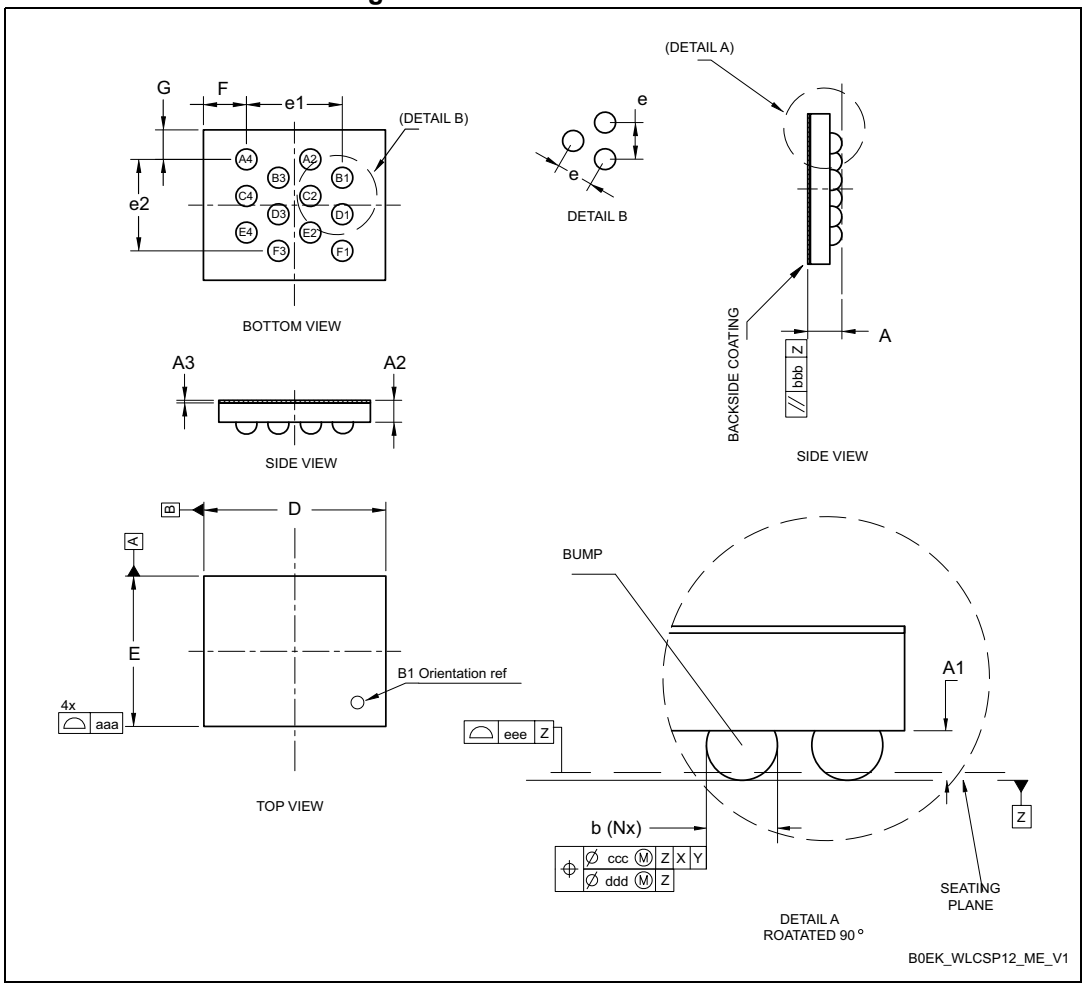


1. Dimensions are expressed in millimeters.

6.3 WLCSP12 package information (B0EK)

This WLCSP is a 12-ball, 1.70 x 1.42 mm, 0.35 mm pitch, wafer level chip scale package

Figure 31. WLCSP12 – Outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.

Table 65. WLCSP12 – Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.49	-	-	0.0193
A1	-	0.17	-	-	0.0067	-
A2	-	0.29	-	-	0.0114	-
A3[3]	-	0.025	-	-	0.0098	-
Ø b[4]	0.21	0.24	0.27	0.0083	0.0094	0.0106
D	1.68	1.70	1.72	0.0661	0.0669	0.0677
E	1.41	1.42	1.43	0.0555	0.0559	0.0563
e	-	0.35	-	-	0.0138	-
e1	-	0.909	-	-	0.0358	-
e2	-	0.875	-	-	0.0344	-
F[5]	-	0.409	-	-	0.0161	-
G[5]	-	0.282	-	-	0.0111	-
N	12					
aaa	-	-	0.10	-	-	0.0039
bbb	-	-	0.10	-	-	0.0039
ccc[6]	-	-	0.10	-	-	0.0039
ddd[7]	-	-	0.05	-	-	0.0020
eee	-	-	0.05	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Back side coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
5. Calculated dimensions are rounded to the 3rd decimal place
6. Bump position designation per JESD 95-1, SPP-010. The tolerance of position that controls the location of the pattern of balls with respect to datums X and Y. For each ball there is a cylindrical tolerance zone ccc perpendicular to datum Z and located on true position with respect to datums X and Y as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone.
7. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone ddd perpendicular to datum Z and located on true position as defined by e. The axis perpendicular to datum Z of each ball must lie within this tolerance zone. Each tolerance zone ddd in the array is contained entirely in the respective zone ccc above. The axis of each ball must lie simultaneously in both tolerance zones

Figure 32. WLCSP12 – Footprint example

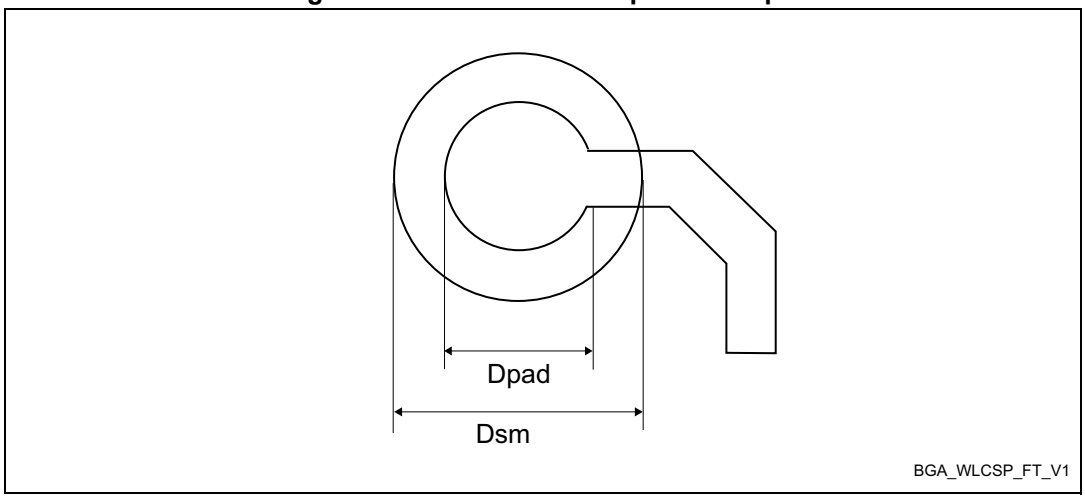


Table 66. WLCSP12 - Example of PCB design rules

Dimension	Recommended values
Pitch	0.35 mm
Dpad	0.200 mm
Dsm	0.275 mm
Stencil thickness	0.08 mm

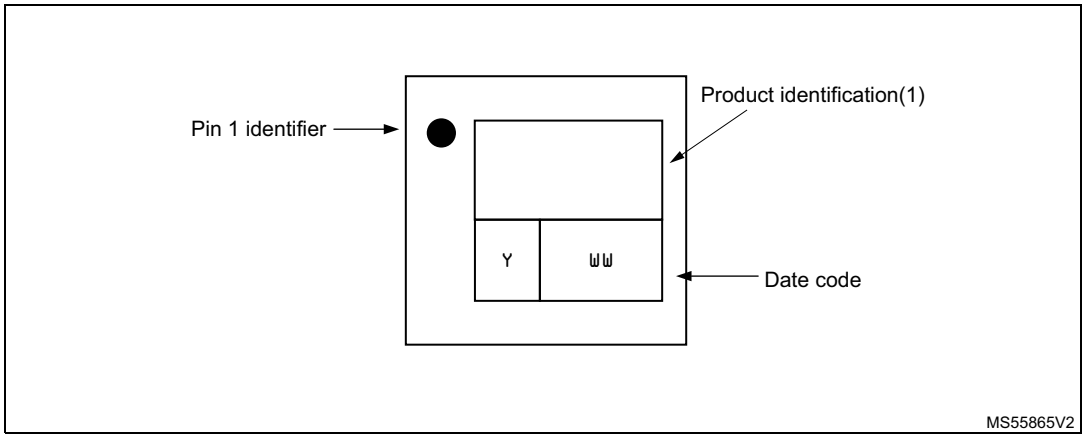
Marking example

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks that identify the parts throughout supply chain operations, are not indicated below.

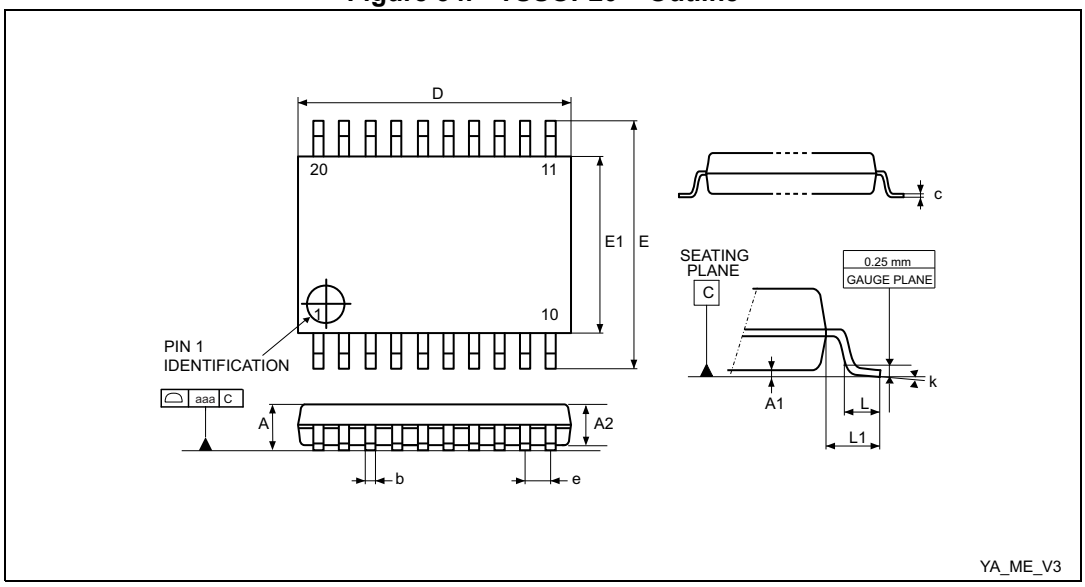
Figure 33. WLCSP12 package marking example



6.4 TSSOP20 package information (YA)

TSSOP20 is a 20-lead, 6.5 x 4.4 mm thin small-outline package with 0.65 mm pitch.

Figure 34. TSSOP20 – Outline



1. Drawing is not to scale.

Table 67. TSSOP20 – Mechanical data

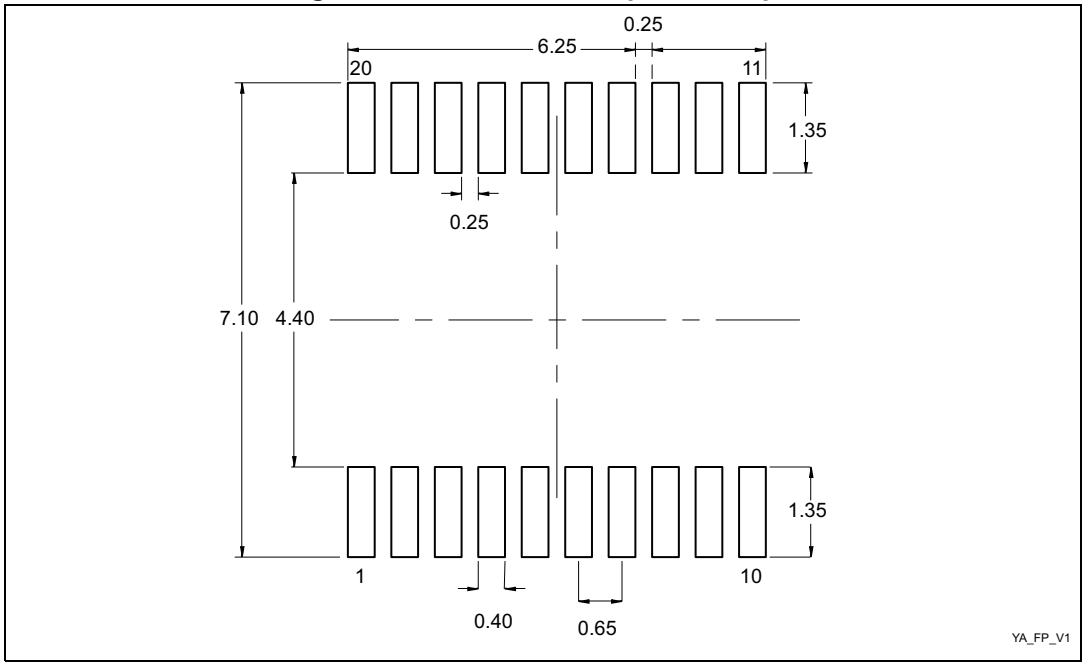
Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118

Table 67. TSSOP20 – Mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

Figure 35. TSSOP20 – Footprint example

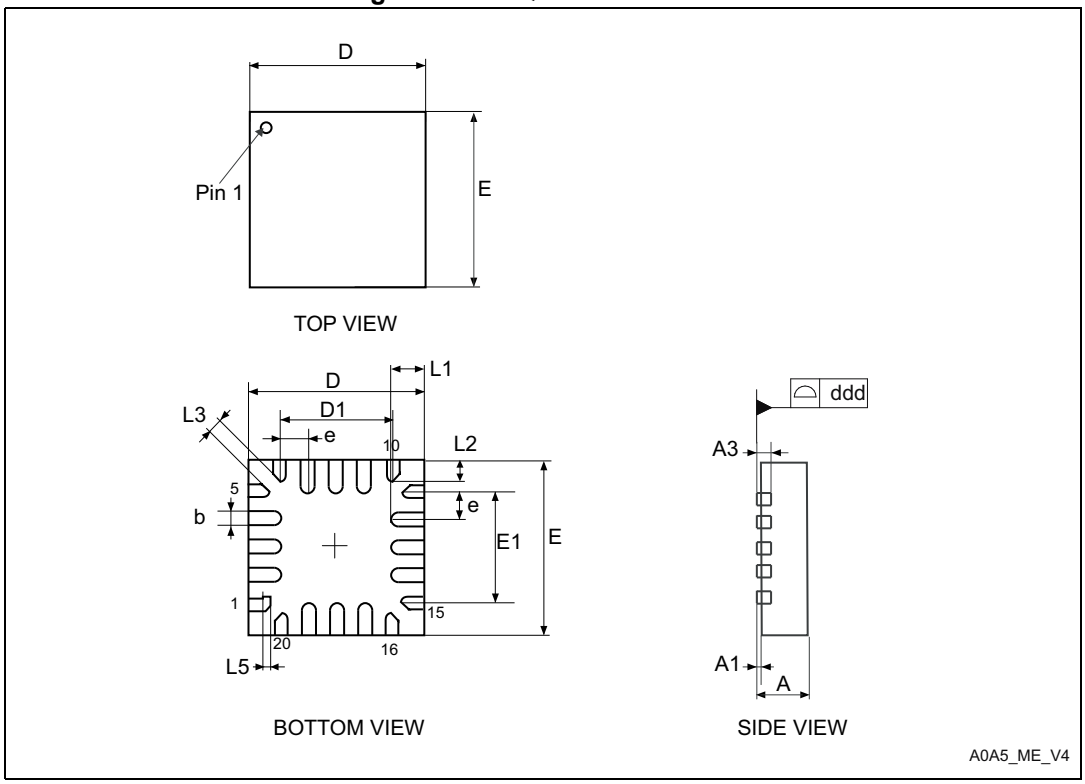


1. Dimensions are expressed in millimeters.

6.5 UFQFPN20 package information (A0A5)

UFQFPN20 is a 20-lead, 3 x 3 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 36. UFQFPN20 – Outline



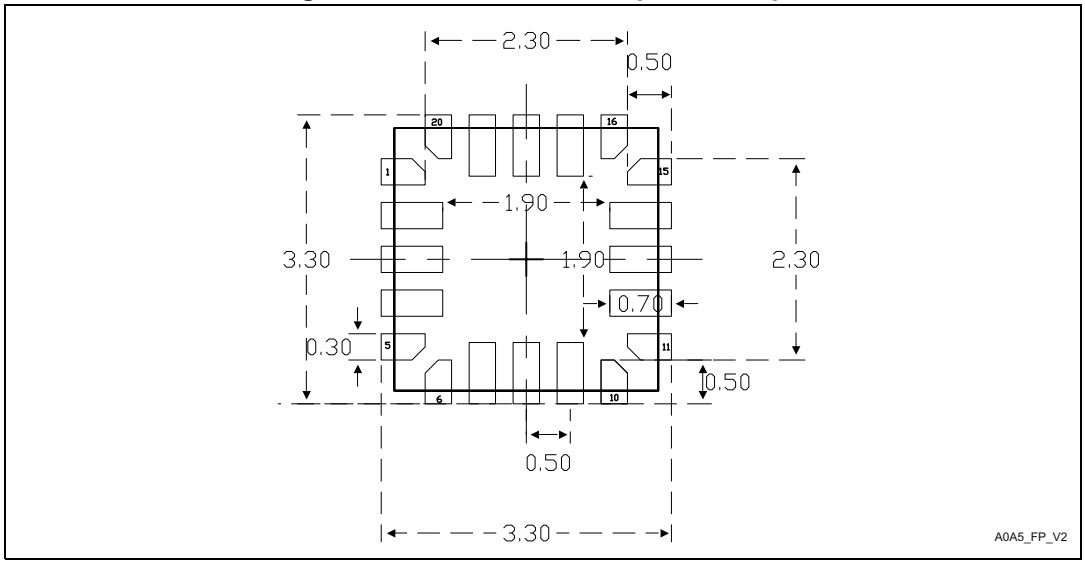
1. Drawing is not to scale.

Table 68. UFQFPN20 – Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.060	-
D	2.900	3.000	3.100	0.1142	0.1181	0.1220
D1	-	2.000	-	-	0.0790	-
E	2.900	3.000	3.100	0.1142	0.1181	0.1220
E1	-	2.000	-	-	0.0790	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. UFQFPN20 – Footprint example



1. Dimensions are expressed in millimeters.

6.6 Thermal characteristics

The operating junction temperature T_J must never exceed the maximum given in *Table 23: General operating conditions*.

The maximum junction temperature in °C that the device can reach if respecting the operating conditions, is:

$$T_J(max) = T_A(max) + P_D(max) \times \Theta_{JA}$$

where:

- $T_A(max)$ is the maximum operating ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D = P_{INT} + P_{I/O}$,
  - P_{INT} is power dissipation contribution from product of I_{DD} and V_{DD}
  - $P_{I/O}$ is power dissipation contribution from output ports where
    $P_{I/O} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIO1} - V_{OH}) \times I_{OH})$, taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 69. Thermal characteristics

Symbol	Parameter	Package[1]	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	UFQFPN20	76.4	°C/W
		TSSOP20	88.7	
		WLCSP12	148	
		SO8N	100	
Θ_{JB}	Thermal resistance junction-board	UFQFPN20	30	°C/W
		TSSOP20	54.6	
		WLCSP12	116.3	
		SO8N	56	
Θ_{JC}	Thermal resistance junction-case	UFQFPN20	31	°C/W
		TSSOP20	25.9	
		WLCSP12	10.6	
		SO8N	46	

1. Refer to *Section 6: Package information* for package dimensions

6.6.1 Reference documents

[1] *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)* (JESD51-2A), JEDEC, January 2008. Available from www.jedec.org.

7 Ordering information

Example STM32 C 011 F 6 P 6 xyy

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

C = general-purpose

Device subfamily

011 = STM32C011

Pin count

J = 8
D = 12
F = 20

Flash memory size

4 = 16 Kbytes
6 = 32 Kbytes

Package type

U = UFQFPN
Y = WLCSP
P = TSSOP
M = SO␣N

Temperature range

6 = -40 to 85°C (105°C junction)
7 = -40 to 105°C (125°C junction)
3 = -40 to 125°C (130°C junction)

Options

TR = tape and reel packing
= tray packing
other = 3-character ID incl. custom flash memory code and packing information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact your nearest ST sales office.

8 Important security notice

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9 Revision history

Table 70. Document revision history

Date	Revision	Changes
30-Mar-2022	1	Initial release
14-Sep-2022	2	Fixed typo errors.
9-Dec-2022	3	Updated: – *Table 2*, *Table 20*, *Table 27*, *Table 28*, *Table 29*, *Table 30*, *Table 36*, *Table 40*, *Table 55* – *Figure 4*, *Figure 9*, *Figure 20*, *Figure 21* – title of *Figure 3* and *Figure 4*
15-Jan-2024	4	Updated: – Cover page – Section *Features*, *Section 1: Introduction* (added reference to reference manual and errata sheet), *Section 3.5: Boot modes*, *Section 3.7.1: Power supply schemes*, *Section 3.9: Clocks and startup*, *Section 3.15.1: Advanced-control timer (TIM1)* *Section 3.18: Universal synchronous/asynchronous receiver transmitter (USART)*, *Section 5.2: Absolute maximum ratings*, *Section : USART (SPI mode) characteristics*, *Section 5.3.6: Wake-up time from low-power modes*, section *I/O system current consumption*, section *General input/output characteristics*, section *USART (SPI mode) characteristics*, *Section 5.3.17: Timer characteristics*, and *Section 6: Package information* – *Table 7*, *Table 12*, *Table 20*, *Table 27*, *Table 44*, *Table 45*, *Table 50*, *Table 56*, *Table 63*, – *Figure 1*, *Figure 2*, *Figure 18*, *Figure 21*, *Figure 22*, *Figure 23* Added: – *Section 6.6: Thermal characteristics* – *Figure 27* and *Figure 28*

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