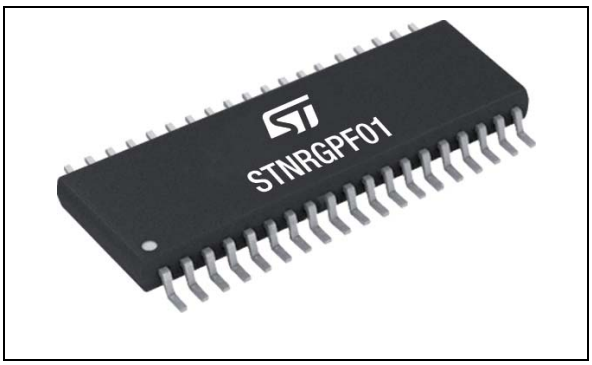
STNRGPF01

Three-channel interleaved CCM PFC digital controller

Datasheet - production data



Features

- Interleaved boost PFC
- Up to 3 interleaved channels
- CCM, fixed frequency
- Average current control, cycle-by-cycle
- Inrush current control
- Burst mode support
- Overcurrent and thermal protection
- Soft start-up
- Flexible phase-shedding strategy
  - High operating frequency with small PFC inductor, suitable for high power-density applications
  - Low ripple current (input/output)
  - Simpler integration with other applications
- Flexible design customization to meet specific customer needs
- Firmware
  - Turnkey solution for quick design
  - eDesign Suite graphical user interface (GUI) for application configuration
- Embedded memory data retention 15 years with ECC
- Communication interfaces
  - UART asynchronous protocol for bootloader support
- Operating temperature: -40 °C to 105 °C

Applications

- Suitable for welding, industrial motors, UPS, battery chargers, power supplies, air conditioners

Table 1. Device summary

Order code	Packing
STNRGPF01	Tube
STNRGPF01TR	Tape and reel

This is information on a product in full production. www.st.com

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1 Description

The STNRGPF01 is a digital controller designed specifically for interleaved PFC boost topologies and intended for use in high power applications.

The controller is capable of driving up to 3 interleaved channels, generating the proper signals in each condition. Moreover, it implements a flexible phase shedding strategy that enables the correct number of PFC channels based on the actual load condition. With this function, the STNRGPF01 is always able to guarantee the highest power efficiency across a wide range of load current requirements.

The device works in CCM at fixed frequency with average current mode control, and implements mixed signal (analog/digital) control. The inner current loop is performed by hardware, ensuring cycle-by-cycle regulation. The outer voltage loop is performed by a digital PI controller with fast dynamic response.

The controller implements several functions: inrush current control, soft start-up, burst mode cooling management and status indicators.

It also features a full set of embedded protections against overvoltage, overcurrent, and thermal faults.

The STNRGPF01 is configured through a visual dedicated software tool (eDesignSuite) to match a wide range of specific applications. Using eDesignSuite, the user can customize the PFC conversion configuration and all the relevant electrical components. As a result, the tool will automatically generate a full schematic which includes a complete list of material and the final binary object code (FW) to be downloaded to the STNRGPF01.

2 STNRGPF01 control architecture

The STNRGPF01 implements mixed signal (analog/digital) control. The inner current loop is performed by hardware and the outer voltage loop is performed by a digital PI controller.

The device performs cascaded control for voltage and current loops to regulate the output voltage by acting on the total average inductor current.

Figure 1. STNRGPF01 control scheme

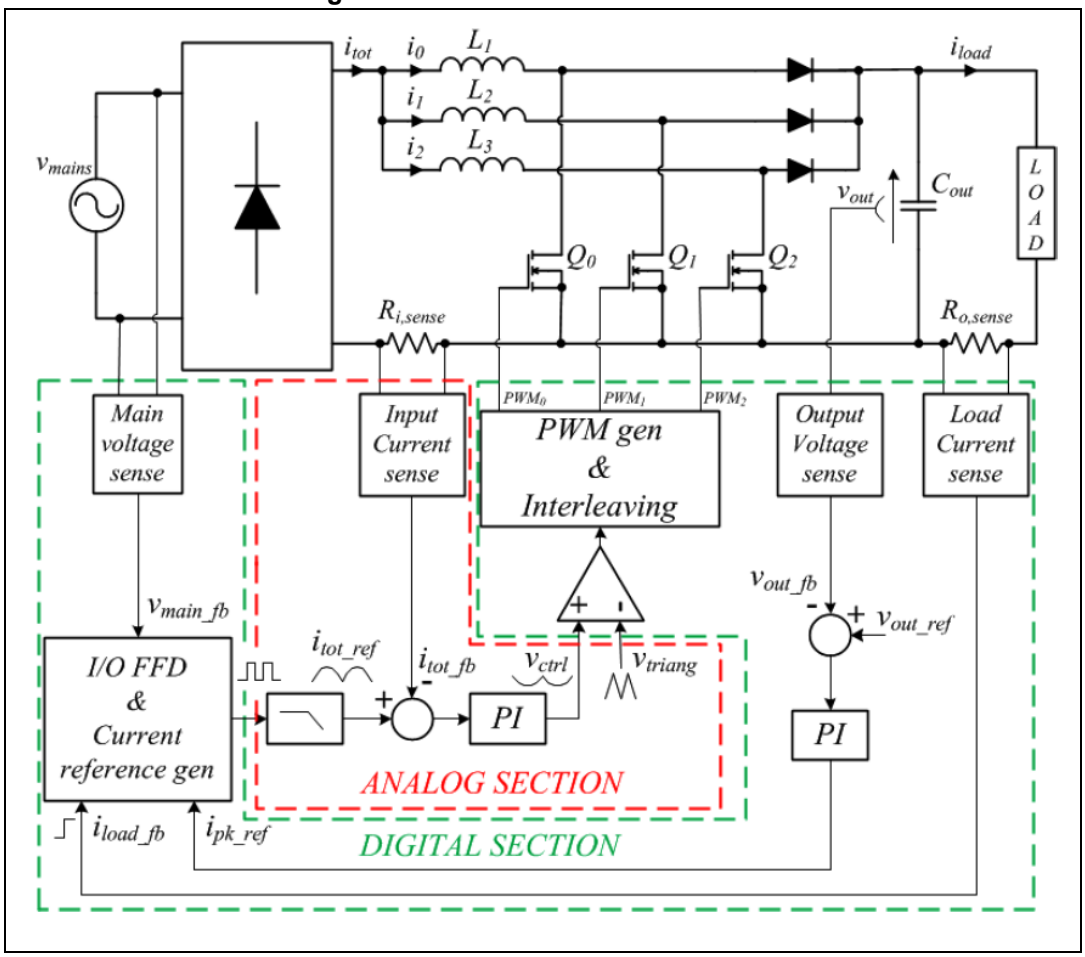


Figure 1 shows the STNRGPF01 control scheme. As can be observed, the difference between the output voltage feedback V_{out_fb} and reference V_{out_ref} is sent to a digital PI controller, which calculates the peak of the input average total current i_{pk_ref}. (internal digital section, green line).

The PFC current reference is internally generated and is output from the I/O FFD block as the PWM signal. After filtering it becomes the total average sinusoidal input current reference i_{tot_ref} for the inner current loop (external analog section, red line). The difference between the current reference i_{tot_ref} and the input current feedback i_{tot_fb} is sent to the analog PI controller.

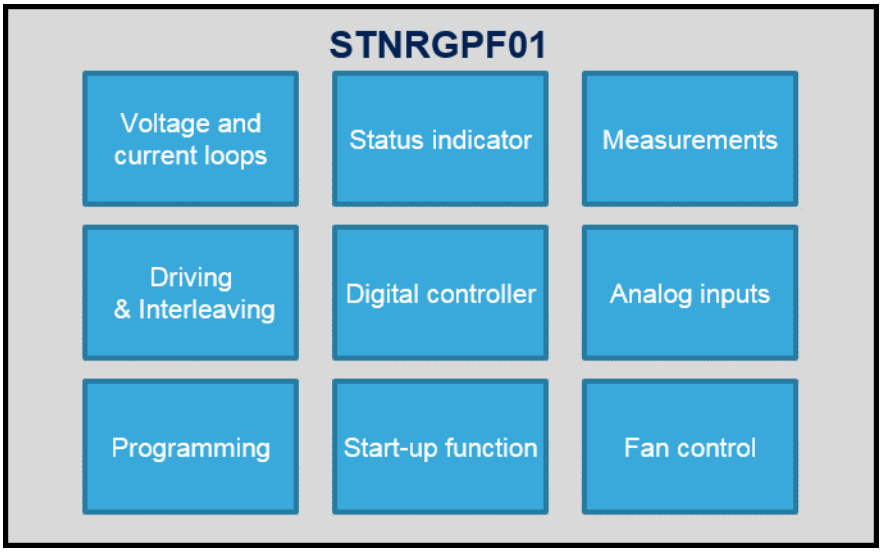
Thus the master PWM signal is generated by comparing the analog PI output V_{ctrl} and a triangular wave V_{triang} at switching frequency. Finally, an interleaving operation is performed and three 120° phase-shifted PWM signals (180° for two channels only) drive the three power switches.

Moreover, the digital section includes the input voltage and load feed-forward for fast transient response when the main voltage changes suddenly or a load step current occurs, preventing large over or undervoltage on the output capacitor C_{out}.

3 STNRGPF01 block diagram

The block diagram of the STNRGPF01 device is shown in *Figure 2*.

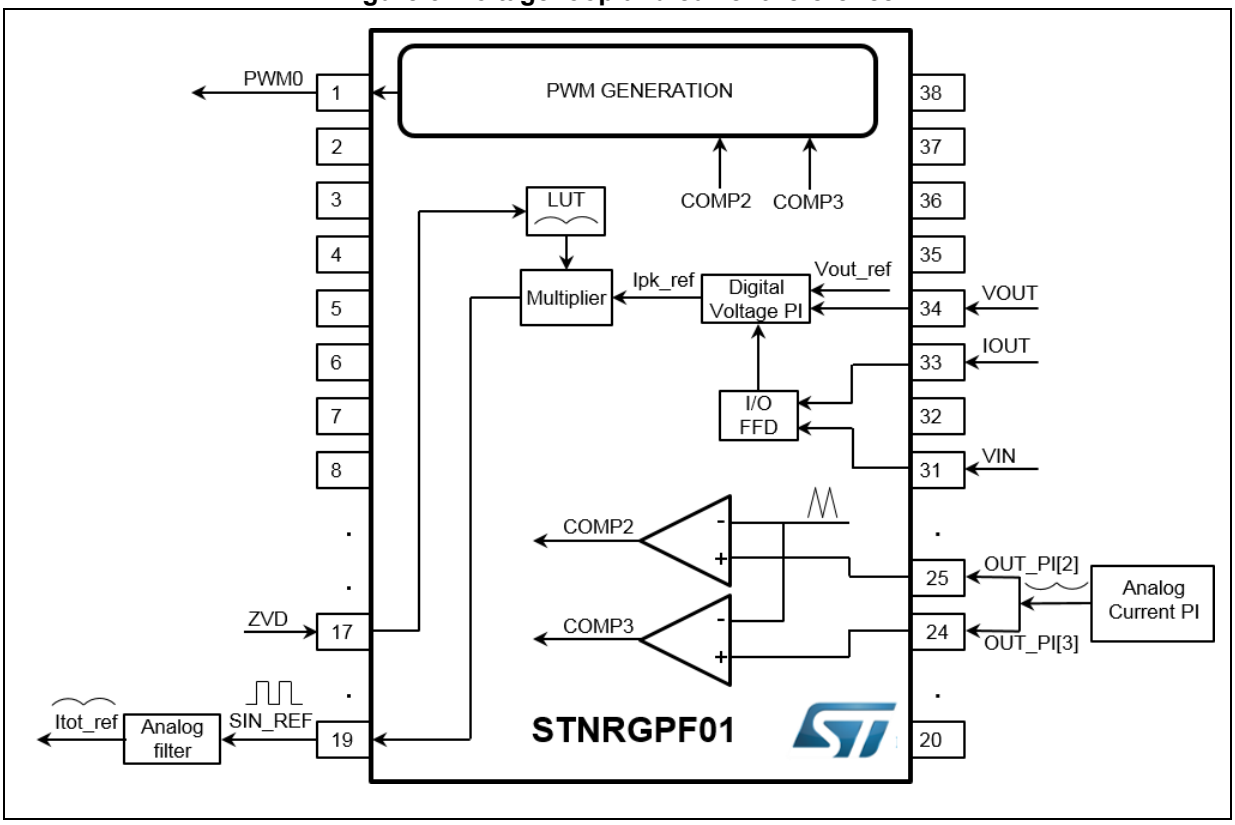
Figure 2. STNRGPF01 block diagram



3.1 Voltage and current loop

The STNRGPF01 implements mixed signal average current control. The task of the digital voltage loop is to regulate the output voltage of the PFC. The VIN and IOUT measurements are used to implement the input/output feed-forward (I/O FFD), so load steps or input voltage variations are quickly compensated for by acting on digital PI output calculations. This function allows keeping the output voltage at the set point value and as constant as possible (see *Figure 3*).

Figure 3. Voltage loop and current reference



The output of the digital PI controller is the peak current reference. In order to obtain a sinusoidal current reference, the I_{pk_ref} is multiplied by a lookup table (LUT). The LUT is synchronized with the input voltage thanks to the ZVD signal (pin 17). The output of the multiplier is a PWM signal with a sinusoidal duty cycle that is configured on pin 19 SIN REF. An analog filter is used to obtain the final sinusoidal current reference for the external current loop (i_{tot_ref}). The analog PI current compares the reference i_{tot_ref} with the total input current feedback (i_{tot_fb}) and generates the duty cycle wave for the PWM modulation. The master PWM signal is obtained by comparing (COMP2,3) the output of the PI current with a triangular wave at switching frequency (see *Figure 6: Analog comparators section* and *Section 3.4: Driving and interleaving*).

3.2 Measurements section

The STNRGPF01 includes 4 input measurement channels. These inputs are defined from pin 31 to pin 34 and they are specified below.

- Pin 31. VIN: RMS input voltage
- Pin 32. Temp: ambient temperature
- Pin 33. IOUT: PFC output current
- Pin 34: VOUT: PFC output voltage

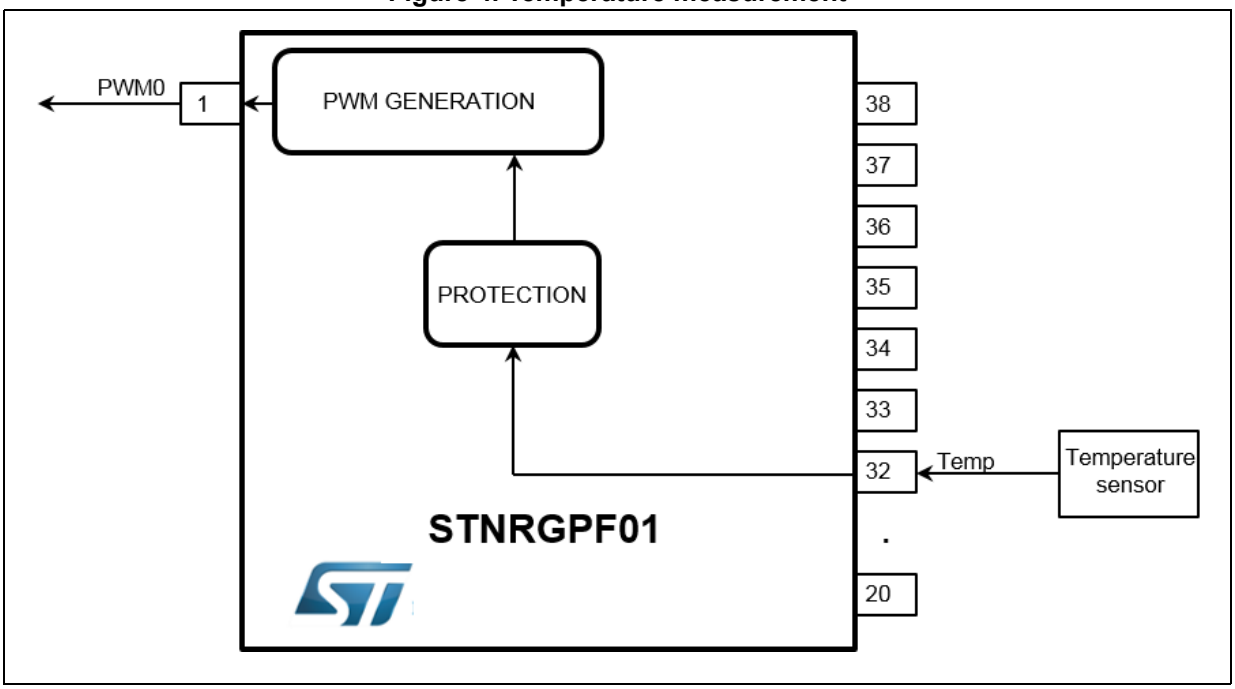
Pin 31, VIN

This is the input of the RMS line voltage and also implements the voltage input feed-forward. The input voltage feed-forward modifies the PI output, compensating rapidly the effect of the line voltage changes. See *Figure 5*.

Pin 32, Temp

This is the input for the board temperature measurement. An external ST temperature sensor, STLM20, measures the board temperature. The PWM activity will be stopped when the temperature exceeds the user-defined threshold. See *Figure 4*.

Figure 4. Temperature measurement



Pin 33, IOUT

Output current sensing. The measurement of this pin voltage allows implementation of the following functions:

- Load feed-forward. The input current reference is modified proportionally to the load, in order to provide a faster response versus the load transient.
- Channel power management. Each channel can be enabled or disabled based on the output current level. For example, up to 30% of the load, only one channel may be enabled, from 30% to 60% of the load, two configuration channels can be selected and at full load all channels may be activated.

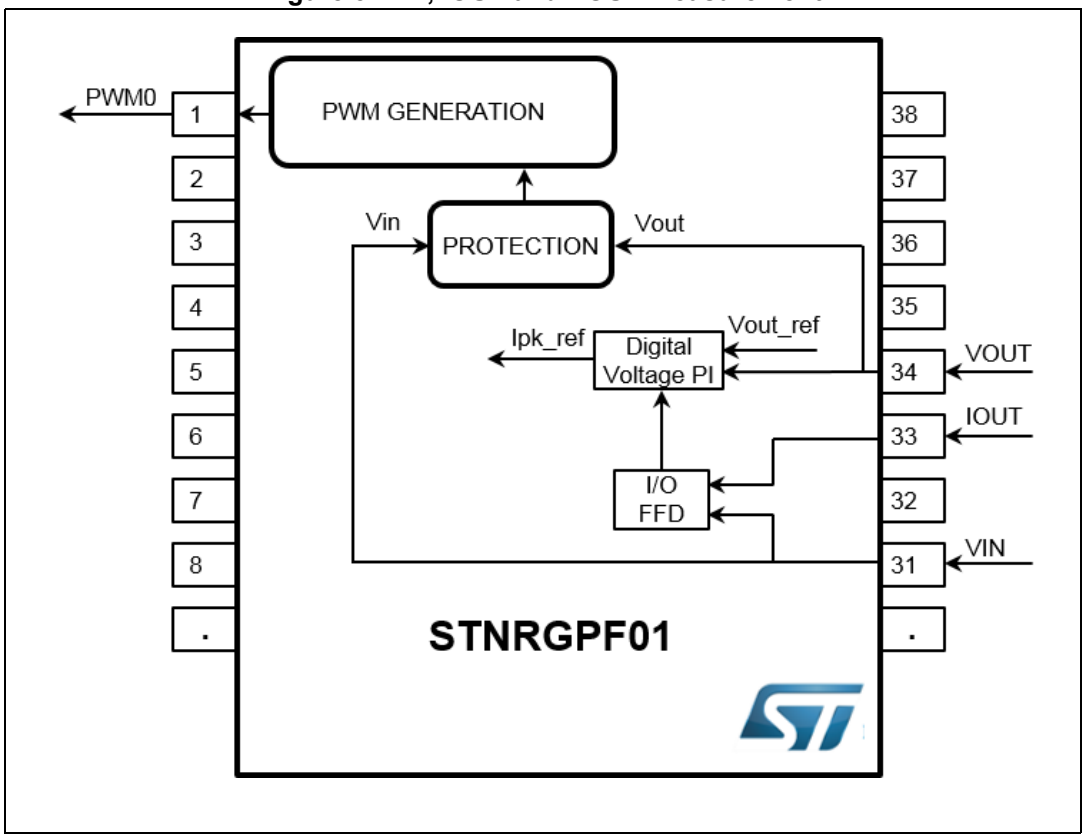
Pin 34, VOUT

Output voltage sensing. This feedback input is connected via a voltage divider to the boost output voltage. This measurement allows implementation of the following functions:

- Output voltage regulation
- Overvoltage protection

In *Figure 5* the block scheme of the VIN, IOUT and VOUT is shown.

Figure 5. VIN, IOUT and VOUT measurement



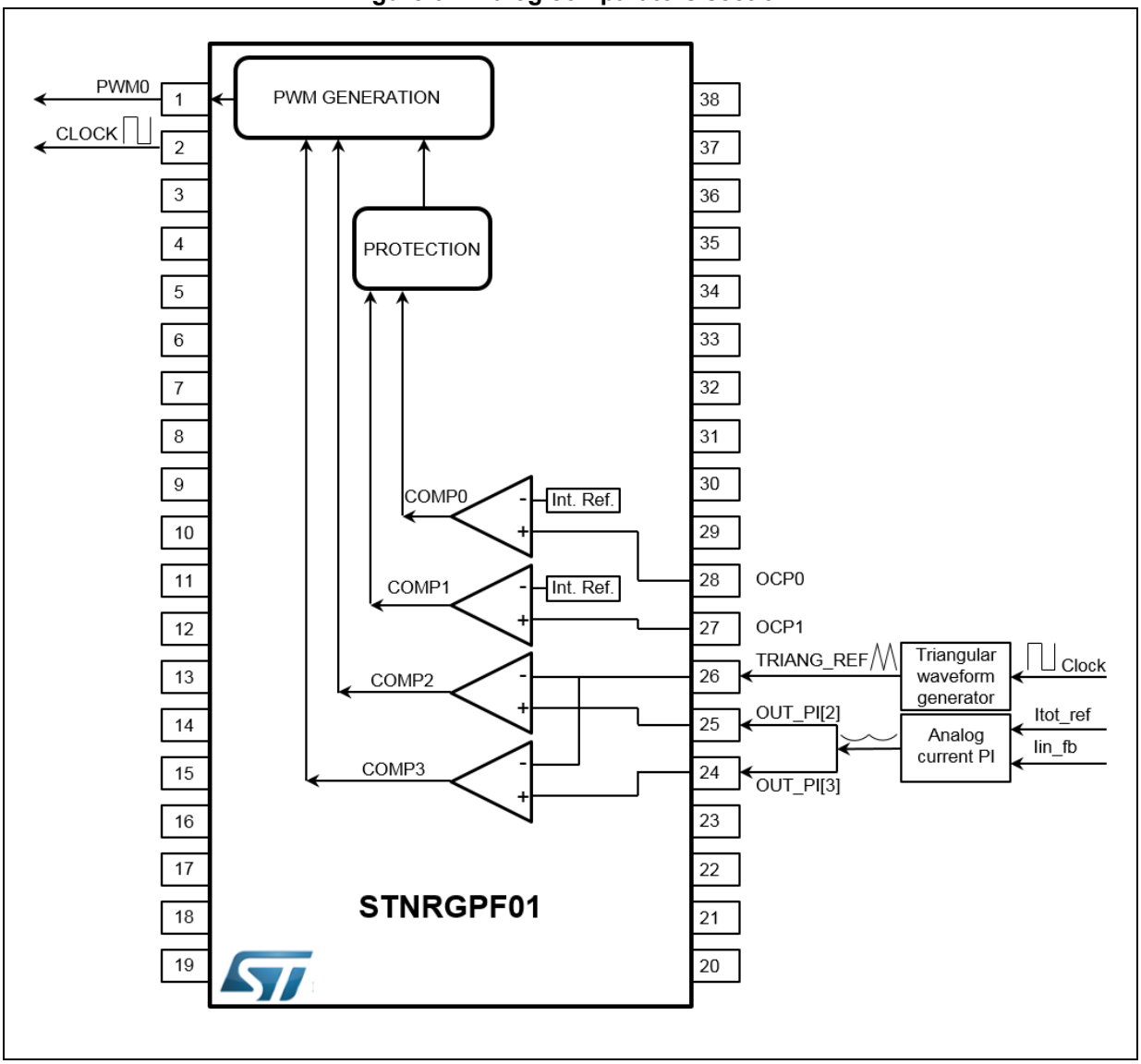
3.3 Analog input section

The STNRGPF01 device includes four fast analog comparators, from COMP0 to COMP3.

COMP3 and COMP2 have external reference voltages and are used to define the duty cycle of the PWM[0] master.

COMP1 and COMP0 have internal reference voltage and are used to implement the overcurrent protection features.

Figure 6. Analog comparators section



The positive inputs of COMP3 and COMP2 are on pin 24 and pin 25. Moreover, these comparators use a common external triangular reference voltage connected to pin 26.

The positive inputs of COMP1 and COMP0 are configured on pin 27 and pin 28.

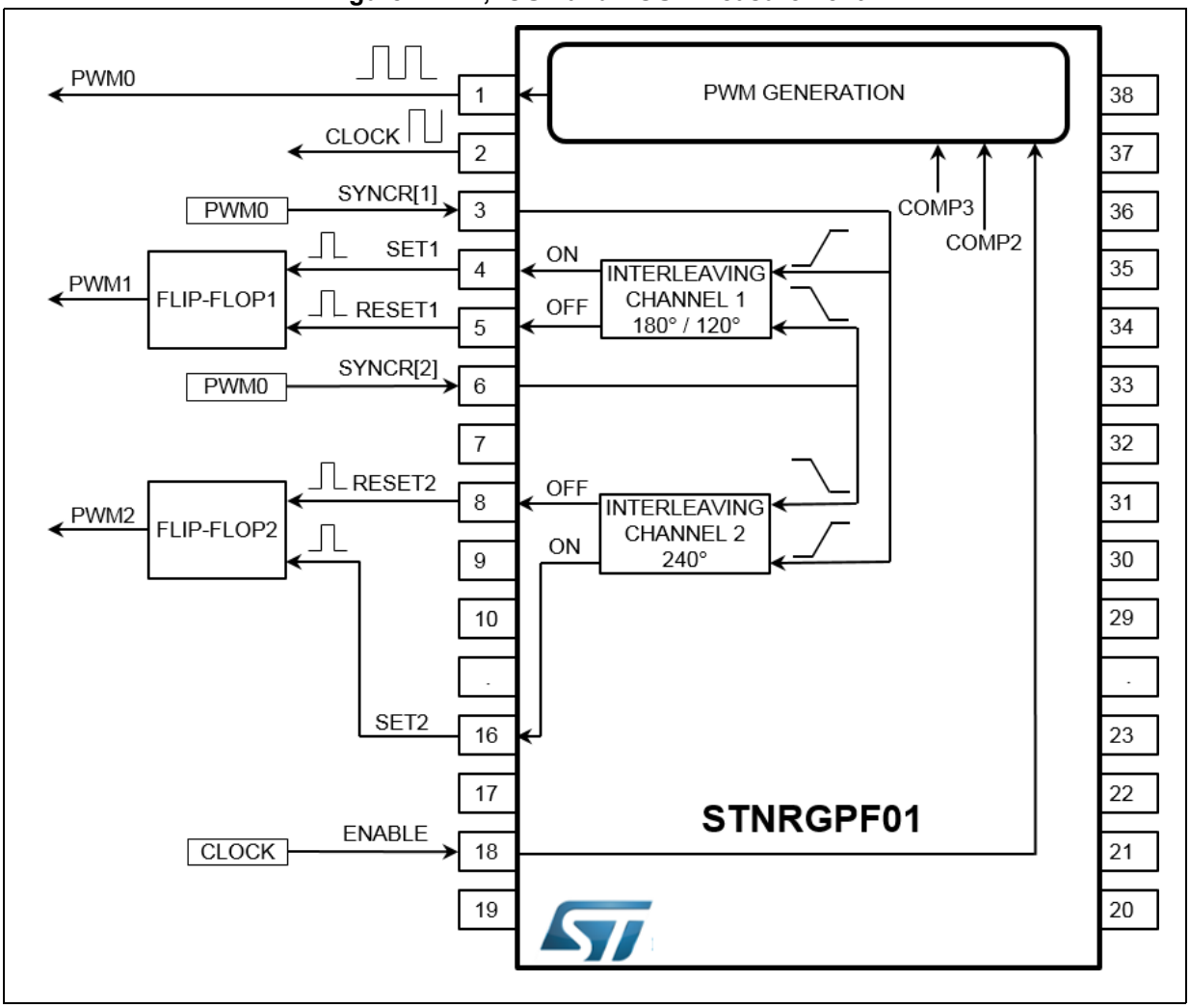
A description of the comparator pins is given below:

- Pin 24 OUT_PI[3]: positive input of the COMP3. It receives the output of the analog PI current.
- Pin 25 OUT_PI[2]: positive input of the COMP2. It receives the output of the analog PI current.
- Pin 26 OSC: negative common input analog COMP2, 3. It receives the reference triangular waveform.
- Pin 27: positive input of the COMP1. It receives the sensing signal of the total input current.
- Pin 28: positive input of the COMP0. It receives the sensing signal of all switch currents. COMP0 stops driving when an overcurrent occurs in any switch.

3.4 Driving and interleaving

The STNRGPF01 PWMs for channel driving are pins: 1, 4, 5, 8 and 16. *Figure 7* shows the configuration for PWM generation.

Figure 7. VIN, IOUT and VOUT measurement



The output level of COMP3 and COMP2 are used to generate the master PWM[0]. The SYNCR[1] and SYNCR[2] inputs are triggered respectively on the rising and falling edge of the PWM[0]. These trigger signals are sent to interleaving blocks which generate the phase shifted (120°/180° and 240°) ON/OFF signals for the other channels.

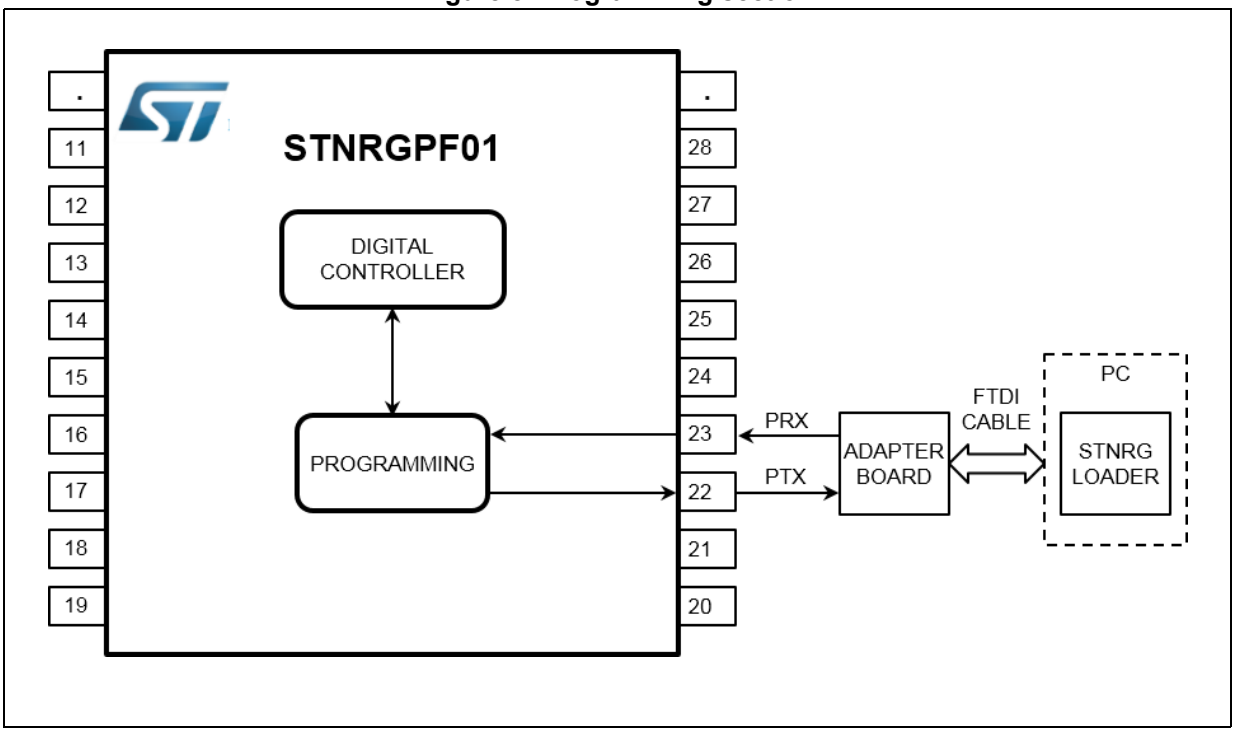
The SET[1], SET[2], RESET[1] and RESET[2] (pins: 4, 5, 8, 16) signals must be connected to external devices (for example two flip-flops) in order to obtain the driving signals PWM1 and PWM2.

The ENABLE input (pin 18) performs a protection function. The connection to the CLOCK signal (pin 2 at switching frequency) prevents undesired commutation of the PWM[0] and consequently on the other channels.

3.5 Programming section

Device programming is done by using a PC with dedicated loader software (STNRG LOADER), an FTDI cable and an adapter board (see *Figure 8*).

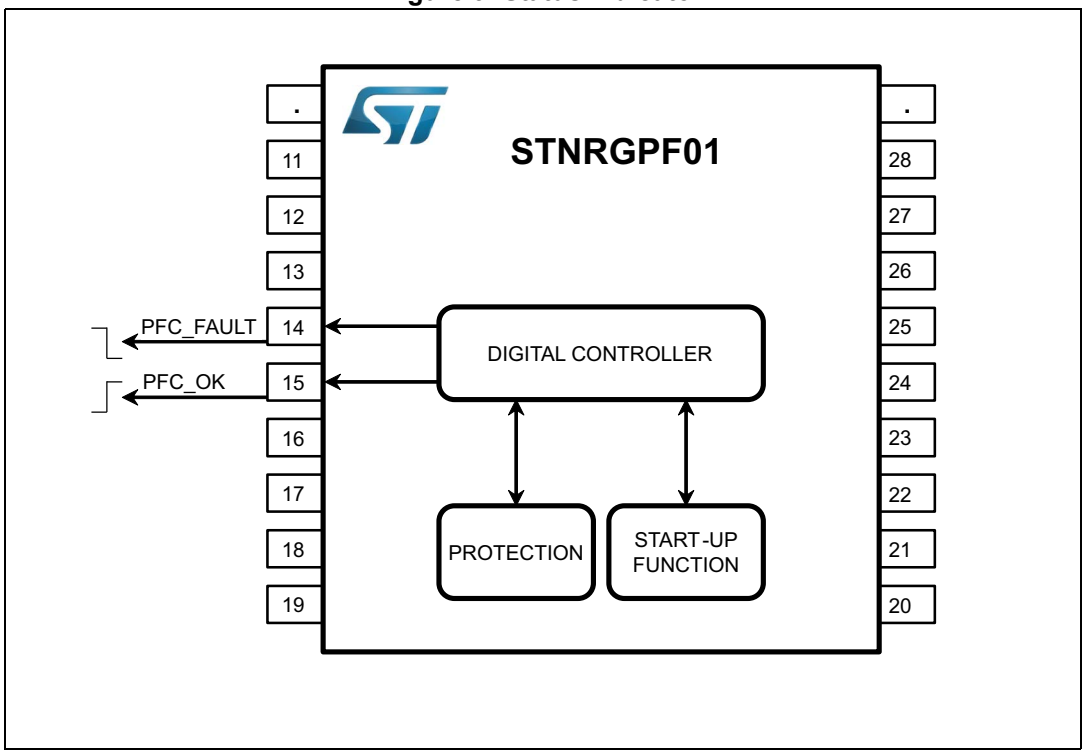
Figure 8. Programming section



3.6 Status indicator

The STNRGPF01 device includes two pins to identify the running or fault status. These functions are defined on pin 14 and pin 15 (see *Figure 9*).

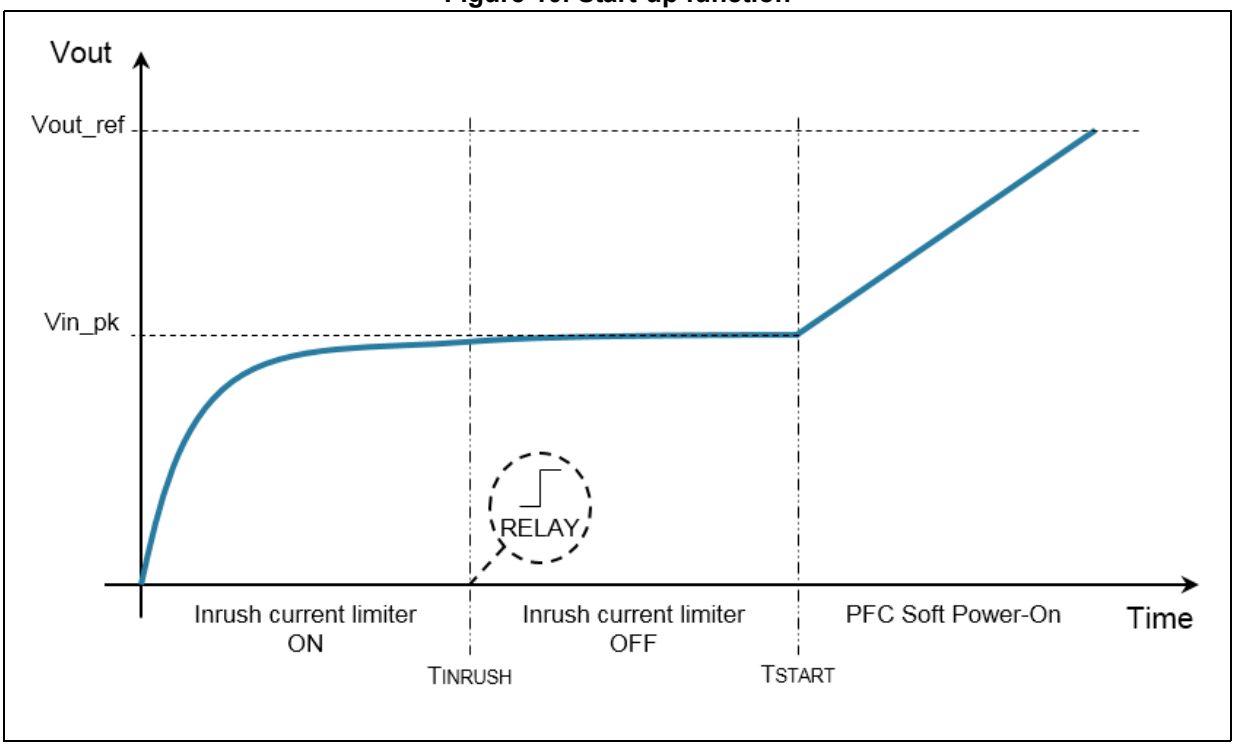
Figure 9. Status indicator



3.7 Start-up function

The start-up function is divided into two logical parts. The first is the inrush current limiter and the second part a PFC soft power-on. In *Figure 10* the timing of this function is shown.

Figure 10. Start-up function



3.7.1 Inrush current limiter

The device includes the possibility to perform the inrush current limiter function. Pin 21 gives a CMOS/TTL signal that becomes high after a settable time.

3.7.2 PFC soft power-on

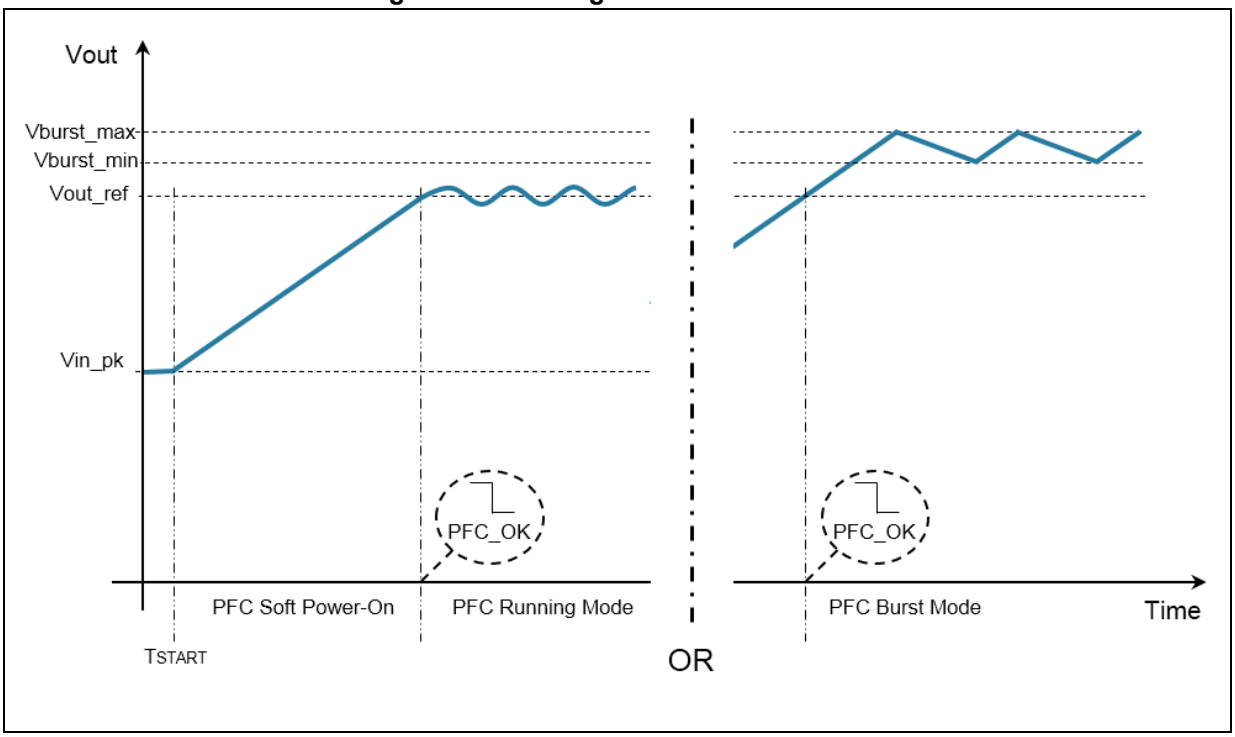
After the inrush current limiter phase the PFC switching activity on the master channel starts using the integrated function named soft power-on. Thanks to a controlled loop regulation the PFC output voltage will increase up to the set point (V_{out_ref}). The soft power-on function will be activated only in the conditions indicated below:

- No load condition. In this case the master channel enters into burst mode regulation. The PFC output voltage will oscillate between two settable levels (V_{burst_min} and V_{burst_max}). See *Figure 11*. These levels can be defined during device customization.
- Light load condition (below 5%). The PFC operates as in the no load condition.
- Load condition (down to 10%). In this case the PFC enters in the run mode and the output voltage will be regulated to the nominal value V_{out_ref}. See *Figure 11*.

When the PFC output voltage is controlled (burst mode or run mode - see conditions 1, 2, and 3) the soft power-on function will be completed and the PFC_OK pin will be activated.

At the end of this phase the PFC is ready to work at the full load.

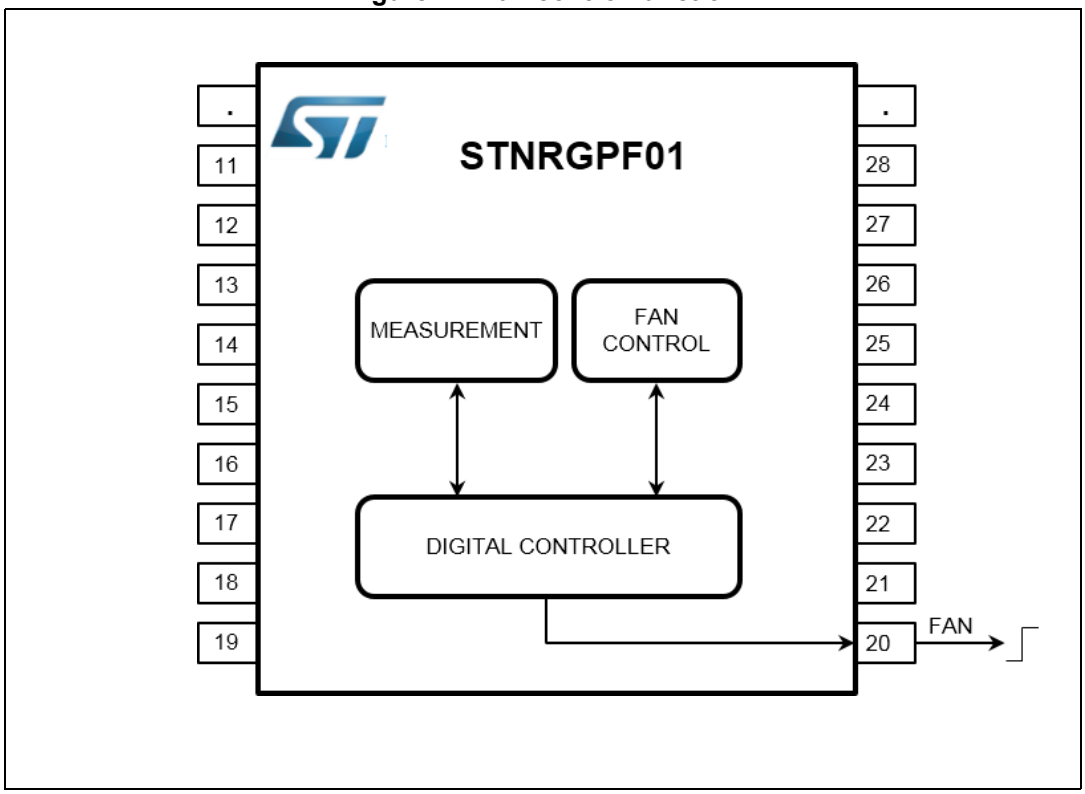
Figure 11. Running mode or burst mode



3.8 Fan control

The device offers the possibility to implement a fan control function. The customer defines the power level for activation of this function. Pin 20 provides a CMOS/TTL signal that becomes high for a power level higher than the specified threshold. See *Figure 12*.

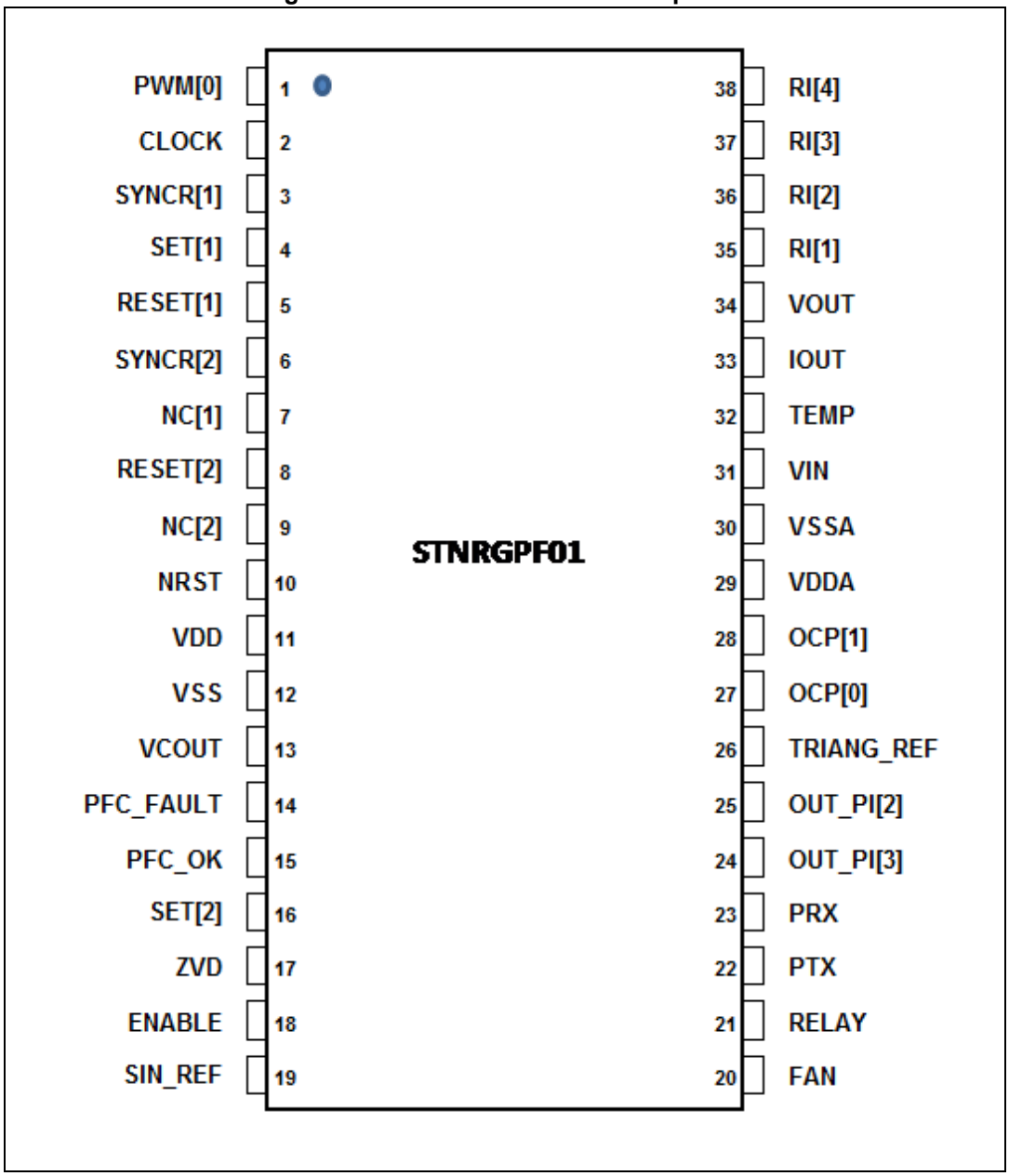
Figure 12. Fan control function



4 Pinout and pin description

4.1 Pinout

Figure 13. STNRGPF01 - TSSOP38 pinout



4.2 Pin description

Table 2. Pin description

No.	Type(1)	Name	Pin description
1	OP	PWM[0]	This pin generates the PWM[0] for the master channel CH0.
2	O	CLOCK	This pin generates a PWM signal at selected working frequency with a duty cycle of 50%. This signal is used to generate triangular waveforms at switching frequency by means of an external op-amp. The CLOCK signal is also used to implement protection against undesired commutations.
3	I	SYNCR[1]	This pin receives the PWM[0] signal in order to synchronize the other channels. The rising edge of the PWM[0] signal is used to trigger ON the slave channels CH1 and CH2.
4	OP	SET[1]	This pin generates a pulse in order to set to ON the CH1 channel with the right out-of-phase. This out-of-phase will be 120° electrical degrees when three channels are activated and 180° when only two channels work. This pin is connected to a SET pin of an external flip-flop in order to start the conduction of the CH1.
5	OP	RESET[1]	This pin generates a pulse in order to set OFF the CH1 channel with the right out-of-phase. This out-of-phase will be 120° electrical degrees when three channels are activated and 180° when only two channels work. This pin is connected to a RESET pin of an external flip-flop in order to stop the conduction of the CH1.
6	I	SYNCR[2]	This pin receives the PWM[0] signal in order to synchronize the other channels. The falling edge of the PWM[0] signal is used to trigger OFF the slave channels CH1 and CH2.
7	NC	NC[1]	Reserved
8	OP	RESET[2]	This pin generates a pulse in order to set OFF the CH2 channel with out-of-phase of 240°. This pin is connected to a RESET pin of an external flip-flop in order to stop the conduction of the CH2.
9	NC	NC[2]	Reserved
10	I/O	NRST	Reset
11	PS	VDD	Supply voltage
12	PS	VSS	Ground
13	PS	VCOUT	Supply voltage of the digital section. An external capacitor must be connected to the VCOUT pin.
14	O	PFC_FAULT	During normal operation this pin is high. If a fault condition occurs it is forced low.
15	O	PFC_OK	When the PFC has completed the start-up procedure, this pin is forced low. During the start-up phase or when in fault condition, this pin is high.
16	OP	SET[2]	This pin generates a pulse in order to set ON the CH2 channel with out-of-phase of 240°. This pin is connected to a SET pin of an external flip-flop in order to start the conduction of the CH2.
17	I	ZVD	This pin receives a square wave signal synchronized with input AC voltage. The rising edge of the square wave signal is used by the STNRGPF01 to detect the ZVD instant.
18	I	ENABLE	This pin receives the CLOCK signal in order to avoid undesired commutation.

Table 2. Pin description (continued)

No.	Type(1)	Name	Pin description
19	OP	SIN_REF	This pin generates a PWM signal with the sinusoidal duty cycle. This PWM signal must be filtered in order to have the current sinusoidal reference that is synchronized with input voltage mains.
20	O	FAN	It generates a CMOS/TTL signal that is low until the PFC output power is below a threshold defined during device customization.
21	O	RELAY	It generates a CMOS/TTL signal. This signal becomes high after a settable time defined during device customization. It is useful to perform the inrush current limiter function.
22	O	PTX	Programming data transmit
23	I	PRX	Programming data receive
24	AI	OUT_PI[3]	Positive input of the internal analog comparator 3. It receives the out of the analog PI current.
25	AI	OUT_PI[2]	Positive input of the internal analog comparator 3. It receives the out of the analog PI current.
26	AI	TRIANG REF	Negative input analog comparators 3 and 2. It receives the voltage triangular waveform.
27	AI	OCP[0]	Input overcurrent protection
28	AI	OCP[1]	Inductor overcurrent protection
29	PS	VDDA	Analog supply voltage
30	PS	VSSA	Analog ground
31	MI	VIN	This pin measures the RMS input voltage.
32	MI	TEMP	This pin measures the ambient board temperature. This measurement is performed using the STLM20 device, which gives an output voltage proportional to temperature.
33	MI	IOUT	This pin measures the PFC output current.
34	MI	VOUT	This pin measures the PFC output voltage.
35	RI	RI[1]	Reserved. This pin must be pulled down by means a 10 kΩ resistor.
36	RI	RI[2]	Reserved. This pin must be pulled down by means a 10 kΩ resistor.
37	RI	RI[3]	Reserved. This pin must be pulled down by means a 10 kΩ resistor.
38	RI	RI[4]	Reserved. This pin must be pulled down by means a 10 kΩ resistor.

1. In *Table 3* a legend describing pin type is provided.

Table 3. Pin identification legend

Type	Pin identification
OP	PWM driver
O	Digital output
I	Digital input
I/O	Digital bidirectional
PS	Power supply
AI	Analog input
MI	Measure input

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}. V_{DDA} and V_{DD} must be connected to the same voltage value. V_{SS} and V_{SSA} must be connected together with the shortest wire loop.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with the ambient temperature at T_A = 25 °C and T_A = T_A max. (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated according to each table specific notes and are not tested in production.

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} and V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested. For the measurement section the accuracy is determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

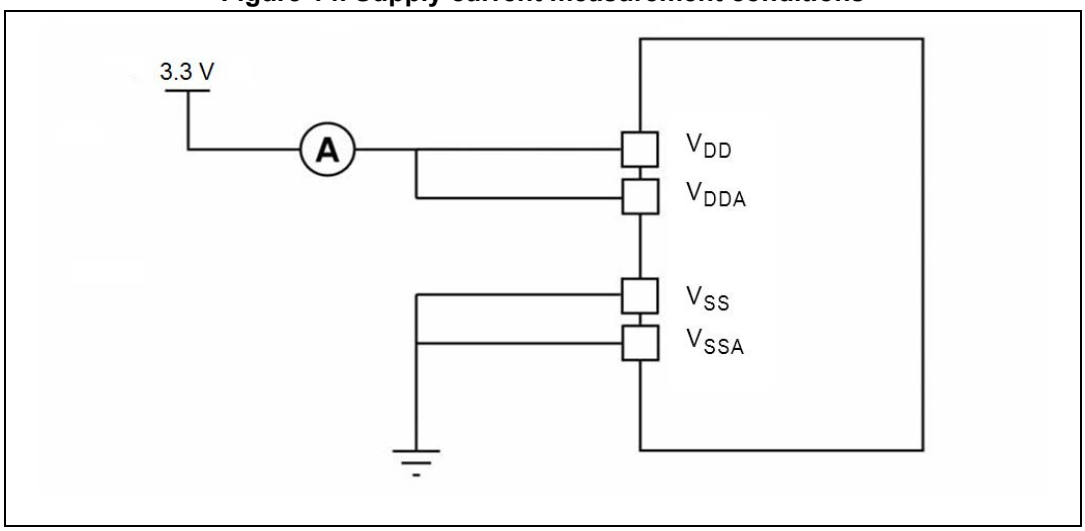
5.1.3 Typical curves

Unless otherwise specified, all typical curves are given as design guidelines only and are not tested.

5.1.4 Typical current consumption

For typical current consumption measurements, V_{DD} and V_{DDA} are connected as shown in *Figure 14*.

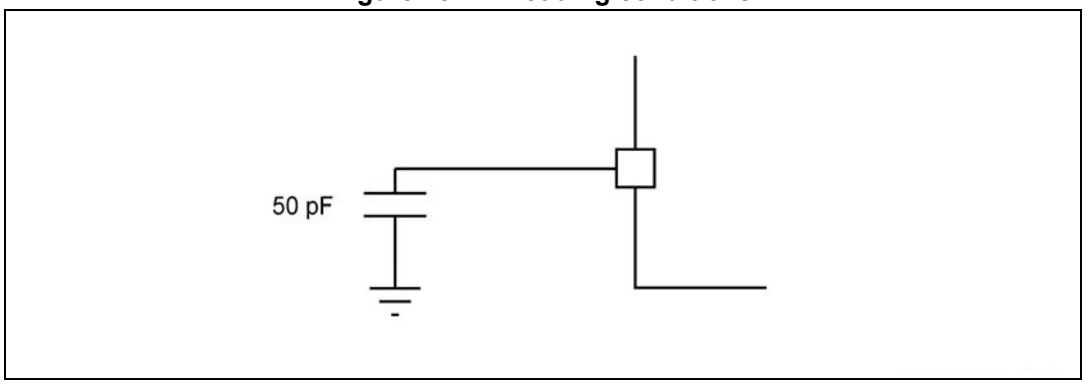
Figure 14. Supply current measurement conditions



5.1.5 Loading capacitors

The loading conditions used for pin parameter measurement are shown in *Figure 15*.

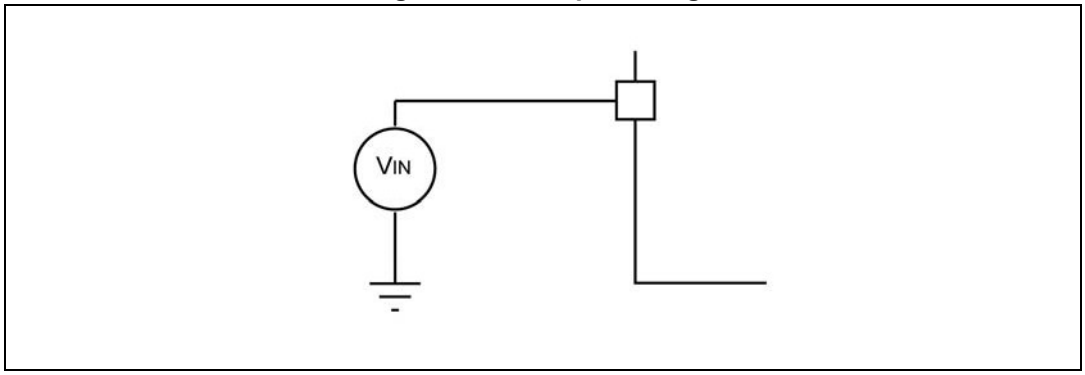
Figure 15. Pin loading conditions



5.1.6 Pin output voltage

The input voltage measurement on a pin is described in *Figure 16*.

Figure 16. Pin input voltage



5.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

Table 4. Voltage characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DDX} - V_{SSX}	Supply voltage(1)	-0.3	6.5	V
V_{IN}	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
V_{DD} - V_{DDA}	Variation between different power pins	-	50	mV
V_{SS} - V_{SSA}	Variation between all the different ground pins(3)	-	50	
V_{ESD}	Electrostatic discharge voltage	Refer to *Table 15 on page 33*.		

1. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. V_{SS} and V_{SSA} signals must be interconnected together with a short wire loop.

Table 5. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDDX}	Total current into VDDX power lines(2)	100	mA
I_{VSSX}	Total current out of VSSX power lines(2)	100	
I_{IO}	Output current sunk by any I/Os and control pin	Ref. to *Table 12 on page 28*	
	Output current source by any I/Os and control pin		
$I_{INJ(PIN)}$(3), (4)	Injected current on any pin	± 4	
$I_{INJ(TOT)}$(3), (4), (5)	Sum of injected currents	± 20	

1. Data based on characterization results, not tested in production.
2. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
4. Negative injection disturbs the analog performance of the device.
5. When several inputs are submitted to a current injection, the maximum $I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with the $I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 6. Thermal characteristics

Symbol	Ratings	Max.	Unit
TSTG	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

5.3 Operating conditions

The device must be used in operating conditions that respect the parameters listed in *Table 7*. In addition, a full account must be taken for all physical capacitor characteristics and tolerances.

Table 7. General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD1}, V_{DDA1}	Operating voltages	-	3	-	5.5	V
V_{DD}, V_{DDA}	Nominal operating voltages	-	-	5	-	
V_{COUT}	Core digital power supply	-	-	1.8(1)	-	
	C_{VCOUT}: capacitance of external capacitor(2)	at 1 MHz	470	-	3300	nF
	ESR of external capacitor(1)		0.05	-	0.2	Ω
	ESL of external capacitor(1)		-	-	15	nH
Θ_{JA}(3)	FR4 multilayer PCB	TSSOP38	-	80	-	°C/W
T_A	Ambient temperature	Pd = 100 mW	-40	-	105	°C

1. Internal core power supply voltage.
2. Care should be taken when the capacitor is selected due to its tolerance, its dependency on temperature, DC bias and frequency.
3. To calculate P_{Dmax} (T_A), use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$.

Table 8. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
t_{VDD}	VDD rise time rate	-	2 µs/V	-	1 s/V(2)	
	VDD fall time rate	-	2 µs/V	-	1 s/V(2)	
t_{TEMP}	Reset release delay	V_{DD} rising	-	3	-	ms
V_{IT+}	Power-on reset threshold	-	2.65	2.8	2.98	V
V_{IT-}	Brownout reset threshold	-	2.58	2.73	2.88	
$V_{HYS(BOR)}$	Brownout reset hysteresis	-	-	70	-	mV

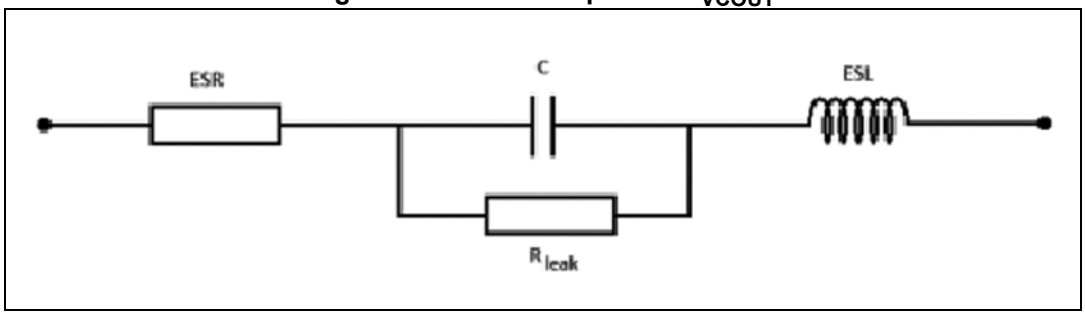
1. Guaranteed by design, not tested in production.
2. The power supply ramp must be monotone.

5.3.1 VCOUT external capacitor

The stabilization of the main regulator is achieved by connecting an external capacitor C_{VCOUT}[(a)] to the VCOUT pin. C_{VCOUT} is specified in *Table 7: General operating conditions*.

Care should be taken to limit the series inductance to less than 15 nH.

Figure 17. External capacitor C_{VCOUT}



5.3.2 Supply current characteristics

The STNRGPF01 current consumption is declared based on, for example, an application where the application firmware is loaded and running.

Table 9. Supply current characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.(1)	Unit
V_{DD}/V_{DDA} SECTION: current consumption						
$IDD_{(RUN)}$	Total current consumption	V_{DD}/V_{DDA} = 5 V	-	28	34	mA

1. Test conditions:
   Data based on characterization results not tested in production.
   Temperature operating: T_A = 25 °C.
   Device in the run mode.

a. ESR is the equivalent series resistance and ESL is the equivalent inductance.

5.3.3 Memory characteristics

Flash program and memory/data E^2PROM.

General conditions: T_A = -40 °C to 105 °C.

Table 10. Flash program memory/data E^2PROM

Symbol	Parameter	Conditions	Min.(1)	Typ.(1)	Max.(1)	Unit
t_{PROG}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)	-	-	6	6.6	ms
	Fast programming time for 1 block (128 bytes)	-	-	3	3.3	
t_{ERASE}	Erase time for 1 block (128 bytes)	-	-	3	3.3	
N_{WE}	Erase/write cycles(2) (program memory)	T_A = 25 °C	10 K	-	-	Cycles
	Erase/write cycles(2)(data memory)	T_A = 85 °C	100 K	-	-	
		T_A = 105 °C	35 K	-	-	
t_{RET}	Data retention (program memory) after 10 K erase/write cycles at T_A = 25 °C	T_{RET} = 85 °C	15	-	-	Years
	Data retention (program memory) after 10 K erase/write cycles at T_A = 25 °C	T_{RET} = 105 °C	11	-	-	
	Data retention (data memory) after 100 K erase/write cycles at T_A = 85 °C	T_{RET} = 85 °C	15	-	-	
	Data retention (data memory) after 35 K erase/write cycles at T_A = 105 °C	T_{RET} = 105 °C	6	-	-	
I_{DDPRG}	Supply current during program and erase cycles	-40 ºC ≤ T_A ≤ 105 ºC	-	2	-	mA

1. Data based on characterization results, not tested in production.
2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

5.3.4 Input/output specifications

The STNRGPF01 device includes three different I/O types:

- Normal I/Os (O or I)
- Fast I/O (OP)
- High speed I/O (CLOCK)

The STNRGPF01 I/Os are designed to withstand the current injection. For the negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA.

5.3.5 I/O port pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. Unused input pins should not be left floating.

Table 11. Voltage DC characteristics

Symbol	Description	Min.(1)	Typ.	Max.(1)	Unit
V_{IL}	Input low voltage	-0.3	-	0.3 x V_{DD}	V
V_{IH}	Input high voltage(2)	0.7 x V_{DD}	-	V_{DD}	
V_{OL1}	Output low voltage at 5 V(3), (4)	-	-	0.5	
V_{OL3}	Output low voltage high sink at 5 V(2), (5)	-	-	0.6	
V_{OH1}	Output high voltage at 5 V(3), (4)	V_{DD} - 0.5	-	-	
V_{OH3}	Output high voltage high sink at 5 V(2), (5)	V_{DD} - 0.6	-	-	
H_{VS}	Hysteresis input voltage(6)	0.1 x V_{DD}	-	-	
R_{PU}	Pull-up resistor	30	45	60	kΩ

1. Data based on characterization result, not tested in production.
2. Input signals can't be exceeded V_{DDX} (V_{DDX} = V_{DD}, V_{DDA}).
3. The parameter applicable to signals on pins 14, 15, 20, 21, 22 and 23.
4. The parameter applicable to signals on pins 1, 4, 5, 8 16 and 19.
5. The parameter applicable to the signal on pin 2.
6. Applicable to pins 3, 6, 7, 17 and 18.

Table 12. Current DC characteristics

Symbol	Description	Min.	Typ.	Max.(1)	Unit
I_{OL1}	Standard output low level current at 5 V and V_{OL1}(2), (3)	-	-	3	mA
I_{OLhs1}	High sink output low level current at 5 V and V_{OL3}(2), (4)	-	-	7.75	
I_{OH1}	Standard output high level current at 5 V and V_{OH1}(2), (3)	-	-	3	
I_{OHhs1}	High sink output high level current at 5 V and V_{OH3}(2), (4)	-	-	7.75	
I_{LKg}	Input leakage current digital - analog $V_{SS} \le V_{IN} \le V_{DD}$(5)	-	-	± 1	µA
$I_{_Inj}$	Injection current(6), (7)	-	-	± 4	mA
$\Sigma I_{_Inj}$	Total injection current sum of all I/O and control pins)(6)	-	-	± 20	

1. Data based on characterization result, not tested in production.
2. The parameter applicable to signals on pins 14, 15, 20, 21, 22 and 23.
3. The parameter applicable to signals on pins1, 4, 5, 8 16 and 19.
4. The parameter applicable to the signal on pin 2.
5. Applicable to pins 3, 6, 7, 17 and 18.
6. Maximum value must never be exceeded.
7. Negative injection current on pins 31, 32, 33 and 34 must be avoided. It has impact on the measurement section.

5.3.6 Typical output level curves

This section shows the typical output voltage level curves measured on a single output pin for the three-pad family present in the STNRG device.

Normal I/Os

These pads are associated with the O type pins.

Figure 18. V_{OH} normal pin

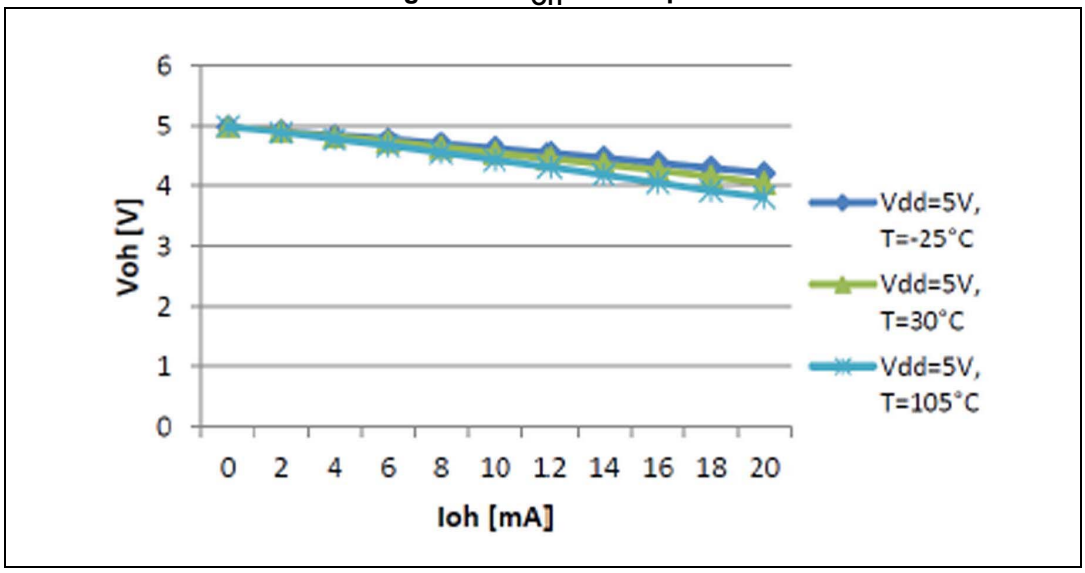
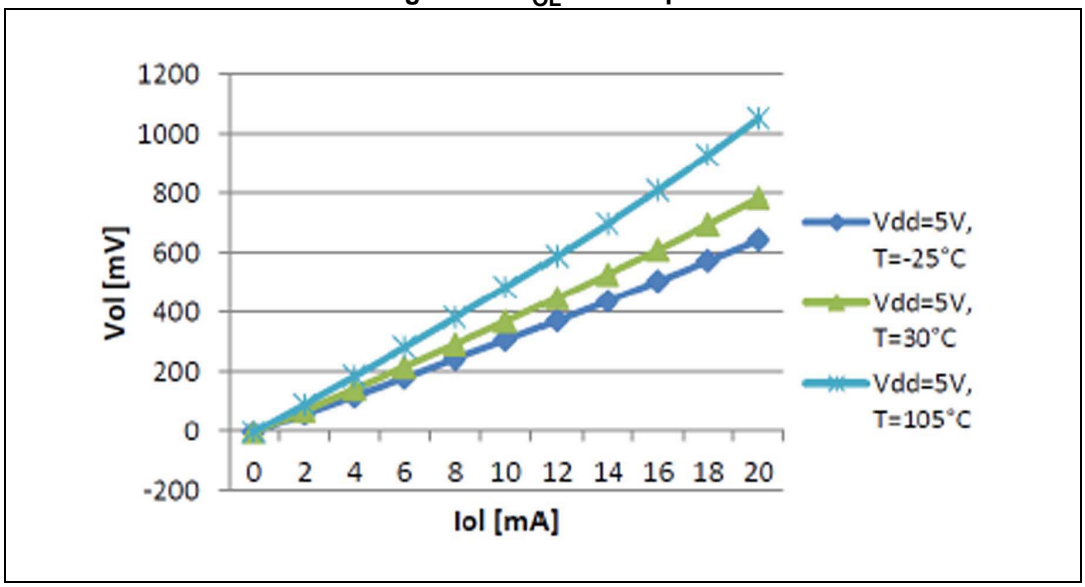


Figure 19. V_{OL} normal pin



Fast I/Os

These pads are associated with the OP type pins.

Figure 20. V_{OH} fast I/Os pins

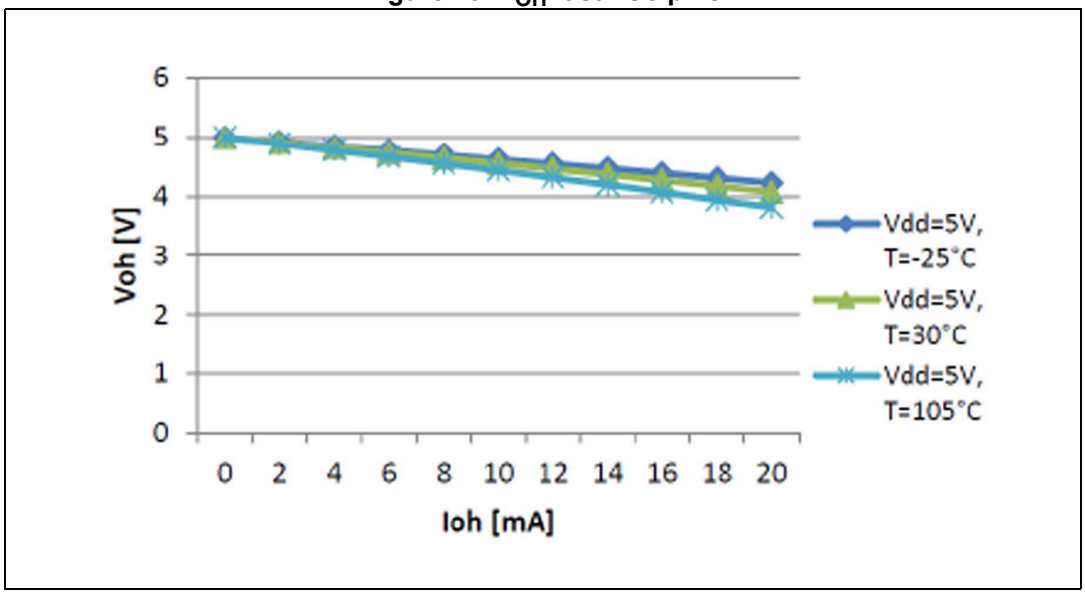
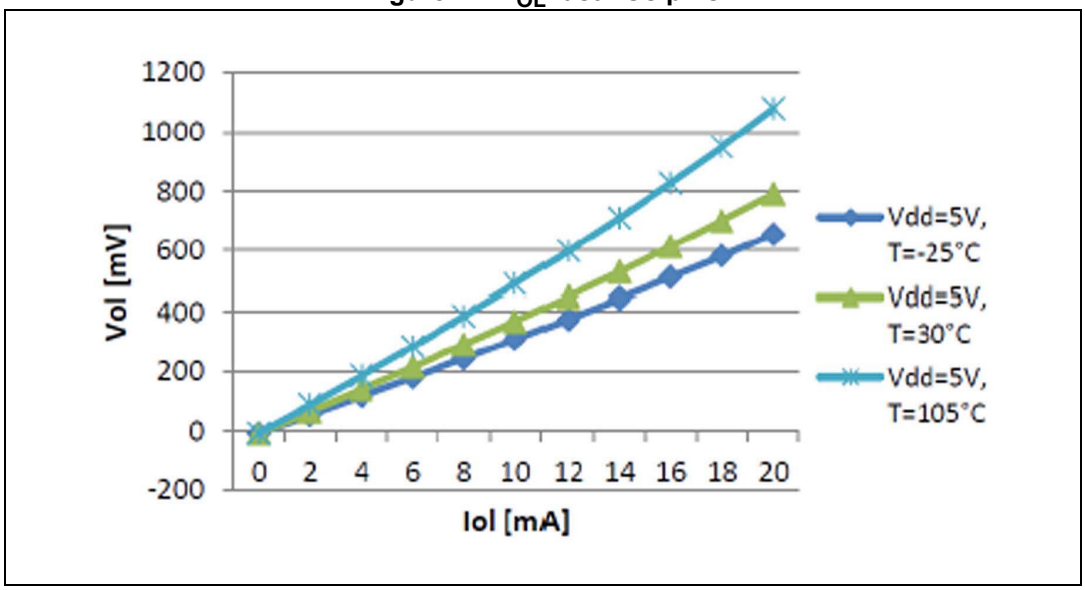


Figure 21. V_{OL} fast I/Os pins



Output CLOCK

This pad is associated with the OUTPUT CLOCK pin.

Figure 22. V_{OH} CLOCK pin

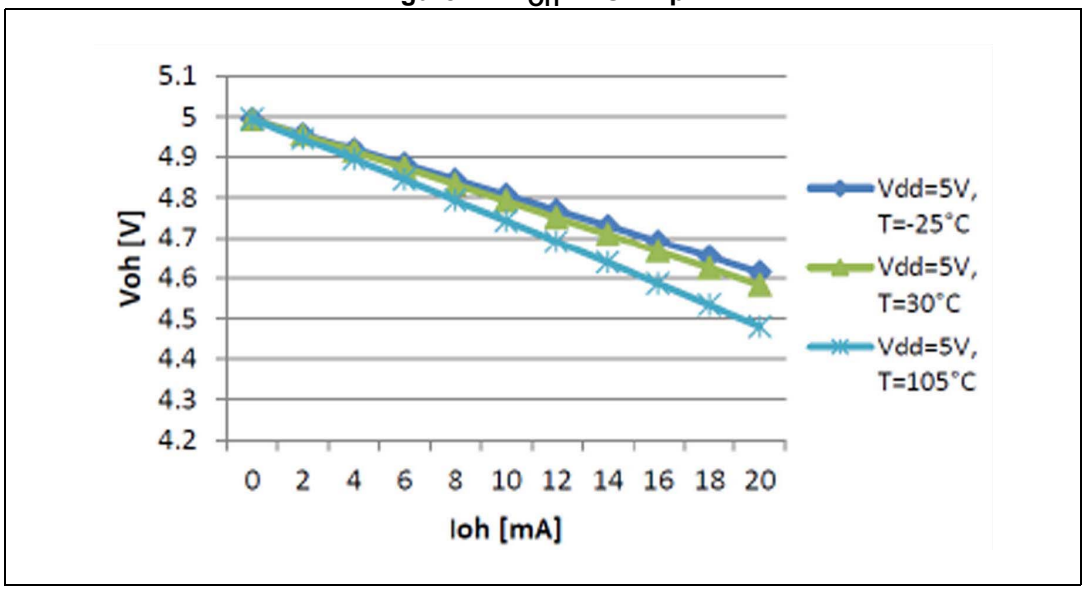
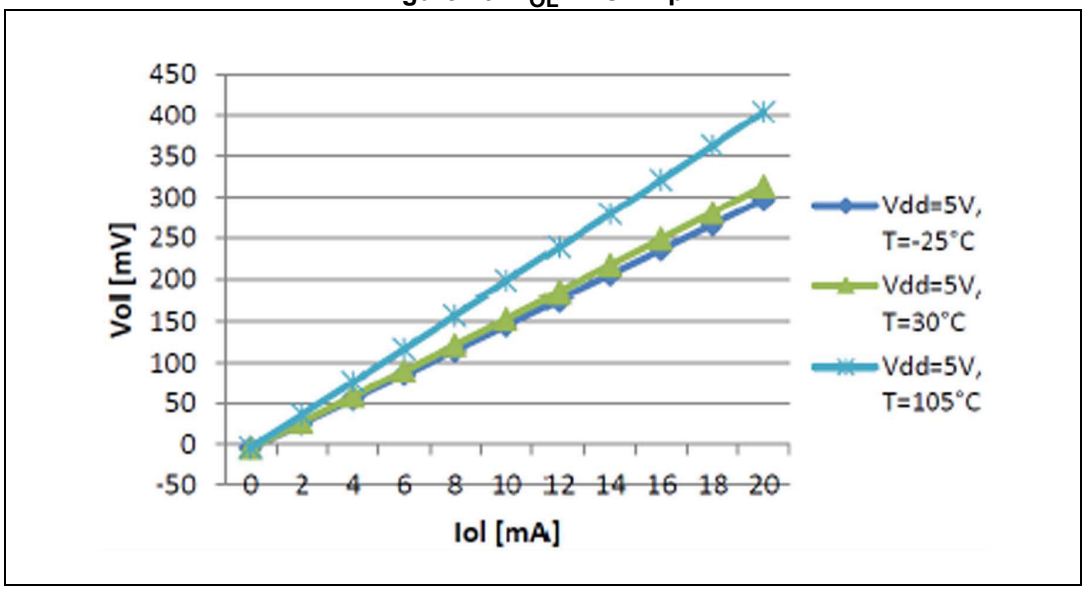


Figure 23. V_{OL} CLOCK pin



5.3.7 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 13. NRST pin characteristics

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)	-	-0.3	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)	-	0.7 x V_{DD}	-	V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL} = 2 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)	-	30	40	60	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)	-	-	-	75	ns
$t_{INFP(NRST)}$	NRST not input filtered pulse(3)	-	500	-	-	
$t_{OP(NRST)}$	NRST output filtered pulse(3)	-	15	-	-	µs

1. Data based on characterization results, not tested in production
2. The RPU pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

5.4 Analog input characteristics

5.4.1 Measurement section

Subject to general operating conditions for V_{DDA} and T_A unless otherwise specified.

It applies to the [MI] class.

Table 14. Measurement pin characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RIN	Input impedance	-	1	-	-	M
VIN	Measurement range	-	0	-	1.25(1)	V
Vref	Measure reference voltage(2)	-	-	1.25	-	

1. Maximum input analog voltage cannot exceed V_{DDA}.
2. Reference voltage at T_A = 25 °C.

5.4.2 Analog section

In *Table 15* analog comparator characteristics are reported.

It applies to the [AI] class.

Table 15. Analog comparator characteristics

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max(1)	Unit
V_{CPP01}	Comparator CP0,1 positive input voltage range	-40 °C ≤ T_A ≤ 105 °C	0	-	1.23(2)	V
V_{CPP23}	Comparator CP2,3 positive input voltage range	-40 °C ≤ T_A ≤ 105 °C	0	-	2(3)	V
V_{CPM23}	Comparator CP2,3 negative external input voltage range	-40 °C ≤ T_A ≤ 105 °C	0	-	2(3)	V
C_{IN}	Input capacitance	-	-	3	-	pF
V_{offset}	Comparator offset error	-	-	-	15	mV
t_{COMP}	Comparison delay time	-	-	-	50(4)	ns

1. Data based on characterization results, not tested in production.
2. Maximum analog input voltage for comparators CP0 and CP1.
3. Maximum analog input voltage for comparators CP2 and CP3.
4. The overdrive voltage is ± 50 mV.

5.5 EMC characteristics

5.5.1 Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device [3 parts * (n + 1) supply pin].

Table 16. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to JEDEC/JESD22-A114E	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to ANSI/ESD STM 5.3.1 ESDA	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	T_A = 25 °C, conforming to JEDEC/JESD-A115-A	200	

1. Data based on characterization results, not tested in production.

5.5.2 Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD78 IC latch-up standard.

Table 17. Electrical sensitivity

Symbol	Parameter	Conditions	Level
LU	Static latch-up class	T_A = 105 °C	A

6 Thermal data

The STNRG functionality cannot be guaranteed when the device, in operation, exceeds the maximum chip junction temperature (T_{Jmax}).

Equation 1

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta J_A)$$

Where:

T_{Amax} is the maximum ambient temperature in °C

Θ_{JA} is the package junction to ambient thermal resistance in °C/W

P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)

P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins where:

$$P_{I/Omax} = (V_{OL} \times I_{OL}) + \Sigma [(V_{DD} - V_{OH}) \times I_{OH}],$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at the low and high level.

Table 18. Package thermal characteristics

Symbol	Parameter	Value	Unit
JA	TSSOP38 - thermal resistance junction to ambient(1)	80	°C/W

1. Thermal resistance is based on the JEDEC JESD51-2 with the 4-layer PCB in natural convection.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 TSSOP38 package information

Figure 24. TSSOP38 package outline

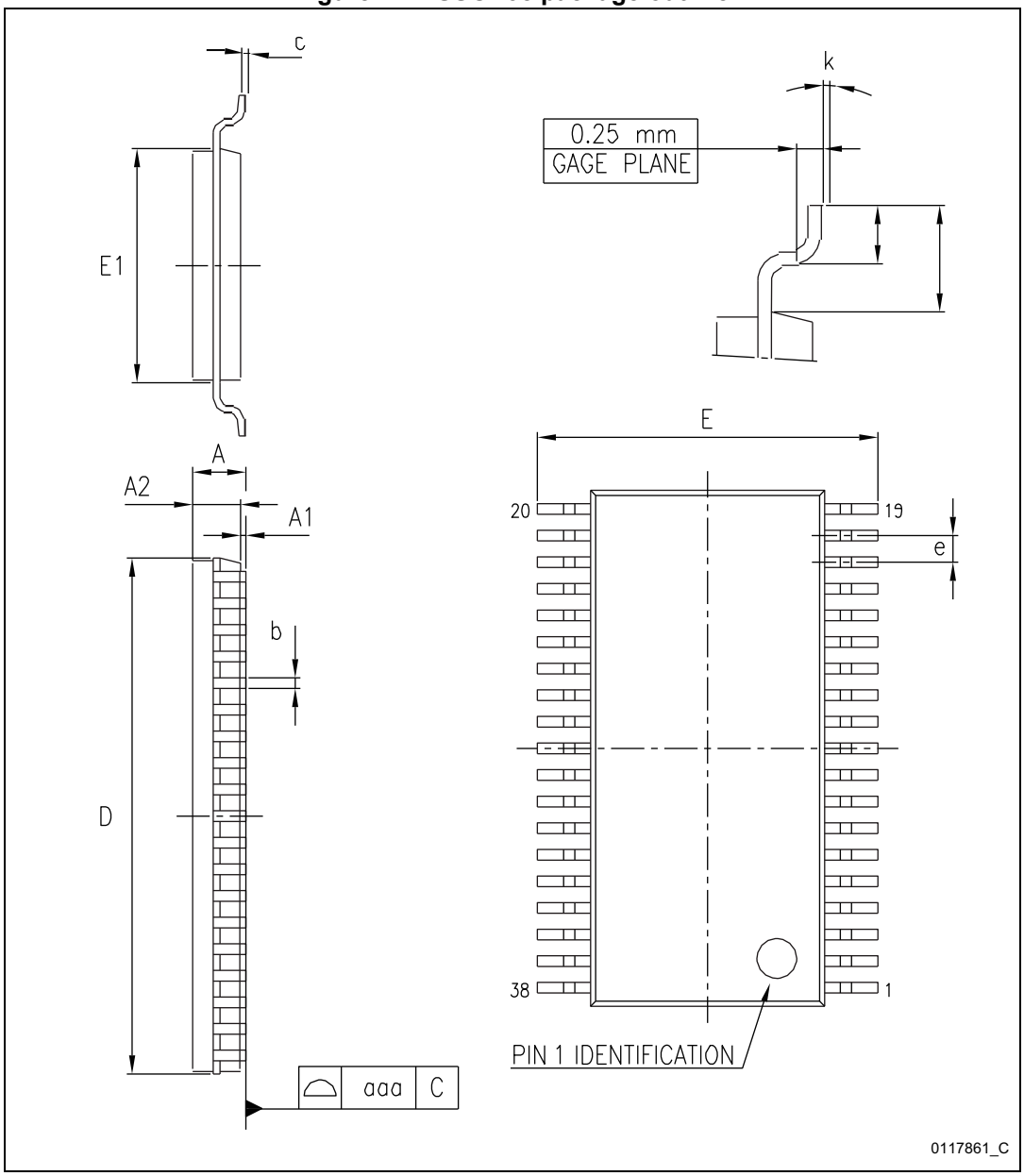


Table 19. TSSOP38 package mechanical data(1)

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.17	-	0.27
c	0.09	-	0.20
D(2)	9.60	9.70	9.80
E	6.20	6.40	6.60
E1(2)	4.30	4.40	4.50
e	-	0.50	-
L	0.45	0.60	0.75
L1	-	1.00	-
k	0	-	8
aaa	-	-	0.10

1. “TSSOP” stands for “Thin Shrink Small Outline Package”.
2. “Dimensions “D” and “E1”do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

8 STNRGPF01 development tools

The development tools for the STNRGPF01 are provided by:

- **eDesign Suite**
  This tool uses a graphical user interface to guide customers step-by-step to implementation of a solution in accordance with their specifications.
  The tool gives users the ability to navigate through an interactive and hierarchical schematic, providing additional information like Bode diagrams for both the current and the voltage loop, power loss calculation, bill of material, and easy shortcuts for datasheets and product folder web pages.
  The final output of this process is a complete design, with a binary file that contains the optimized firmware for that specific application, which can be uploaded to the STNRGPF01 device using the UART serial communication port.
- **STNRG LOADER**
  This tool permits the user to download the binary code from the eDesign Suite.

9 Ordering information

Table 20. Ordering information

Order codes	Package	Packaging
STNRGPF01	TSSOP38	Tube
STNRGPF01TR		Tape and reel

10 Revision history

Table 21. Document revision history

Date	Revision	Changes
23-Feb-2017	1	Initial release.
14-Apr-2017	2	Replaced “PWM0” by “PWM[0]”, “SET1” by “SET[1]”, “SET2” by “SET[2]”, “RESET1” by “RESET[1]”, “RESET2” by “RESET[2]”, “OCP” by “OCP[0]”, “OCP1” by “OCP[1]” and “C_{VOUT}” by “C_{VCOUT}” in the whole document. Updated *Figure 13 on page 18* (replaced by new figure). Added “NC[1]”, “NC[2]”, “RI[1]”, “RI[2]”, “RI[3]”, “RI[4]” in *Table 2 on page 19*. Replaced “VOUT” by “VCOUT” in *Table 2 on page 19*, *Table 7 on page 25* and *Section 5.3.1 on page 26*. Minor modifications throughout document.

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