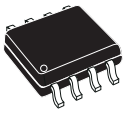
TSC2020, TSC2021, TSC2022

Datasheet

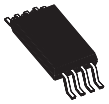
100 V, precision, bidirectional current sense amplifier



SO8



MiniSO8



TSSOP8

Maturity status link
TSC2020, TSC2021, TSC2022

Features

- Wide common-mode voltage: -4 to 100 V
- High common-mode rejection CMR: 100 dB min.
- Offset voltage: ±150 µV max.
- Offset drift: 0.5 µV/°C max.
- Enhanced PWM rejection
- 2.7 to 5.5 V supply voltage
- Internal fixed gain
  - TSC2020: 20 V/V
  - TSC2021: 50 V/V
  - TSC2022: 100 V/V
- Gain error: 0.3% max.
- Gain drift: 3.5 ppm/°C max.
- SO8, MiniSO8 and TSSOP8 packages
- AEC-Q100 qualified

Applications

- High-side/low-side current sensing
- Battery management system
- 48 V power distribution
- 48 V power tools
- Motor control
- Automotive

Description

TSC2020, TSC2021 and TSC2022 are a series of precision bidirectional current sense amplifier. They can sense current via a shunt resistor over a wide range of common-mode voltages, from -4 to +100 V, whatever the supply voltage is. It is able to sense very low drop voltages, minimizing measurement error.

TSC2020, TSC2021 and TSC2022 are current sense amplifiers that may be used for various functions like precision current measurement, overcurrent protection, current monitoring, and feedback loops. These devices fully operate over the supply voltage range of 2.7 to 5.5 V, and over an ambient temperature range of -40 to 125 °C.

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1 Block diagram and pin description

Figure 1. **Block diagram**

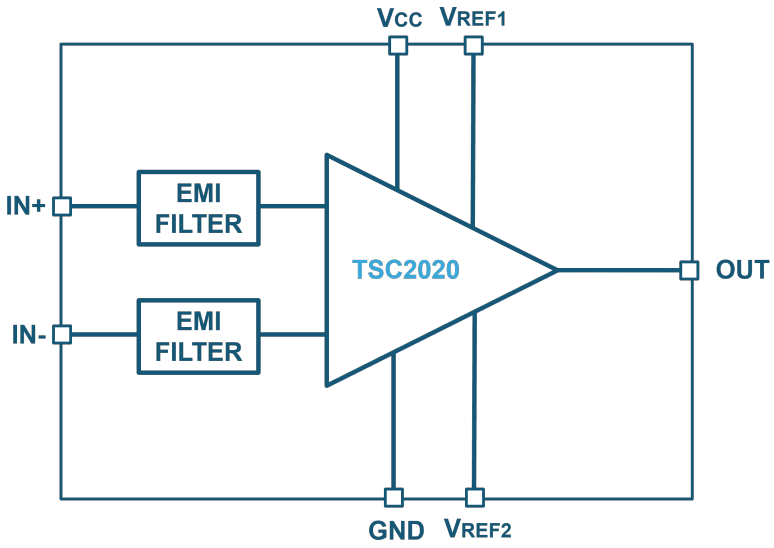

Figure 2. **Pin connections (top view)**

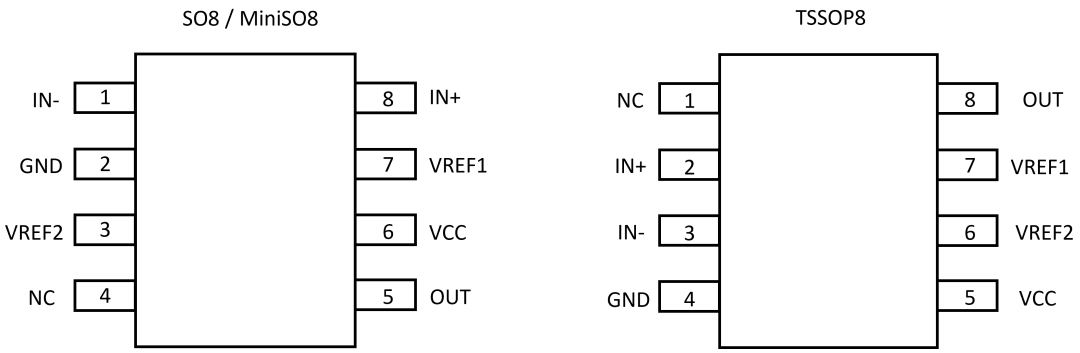

Table 1. **Pin description**

SO8/MiniSO8	TSSOP8	Pin name	Description
1	3	IN-	Negative input
2	4	GND	Ground
3	6	VREF2	Reference voltage 2
4	1	NC	Not connected
5	8	OUT	Output
6	5	VCC	Supply voltage
7	7	VREF1	Reference voltage 1
8	2	IN+	Positive input

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2 Absolute maximum ratings and operation conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	-0.3 to 5.8	V
V_{ICM}	Common-mode voltage on input pins	-10 to 105	V
V_{DIF}	Differential voltage between input pins (IN+, IN-)	±70	V
V_{REF1}, V_{REF2}, V_{OUT}	Voltage present on pins REF1, REF2, and OUT	GND - 0.3 to V_{CC} + 0.3	V
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature	-65 to 150	°C
ESD	Human body model (HBM) (2)	2000	V
	Charged device model (CDM) (3) SO8 MiniSO8 TSSOP8	 750 1000 500	V
RTH_{JA}	Thermal resistance junction to ambient (4)(5) SO8 MiniSO8 TSSOP8	 125 190 120	°C/W

1. *All voltage values, except the differential voltage, are with respect to the network ground terminal.*
2. *According to JEDEC standard JESD22-A114F.*
3. *According to ANSI/ESD STM 5.3.1.*
4. *Short-circuits can cause excessive heating and destructive dissipation.*
5. *The RTHs are typical values.*

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 5.5	V
V_{ICM}	Common-mode voltage on input pins	-4 to +100	V
V_{REF}	Output offset adjustment range	0 to V_{CC}	V
T	Operating free-air temperature range	-40 to 125	°C

3 Electrical characteristics

Table 4. Electrical characteristics - V_{CC} = 2.7 V, V_{ICM} = 48 V, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
I_{CC}	Current consumption	V_{ICM} = -4 to 100 V		1.7	2.3	mA
		Tmin < T < Tmax			2.3	
Input						
|Vos|	Offset voltage (RTI) (1)	V_{ICM} = 12 V, V_{REF} = 1.35 V			150	µV
		Tmin < T < Tmax			200	
		V_{ICM} = 48 V, V_{REF} = 1.35 V			400	
		Tmin < T < Tmax			500	
|ΔVos/ΔT|	Offset drift vs. temperature	V_{ICM} = 12 V, Tmin < T < Tmax			0.5	µV/°C
		V_{ICM} = 48 V, Tmin < T < Tmax			1	
CMR	Common-mode rejection	V_{ICM} = - 4 to 100 V, DC mode	100	112		dB
		Tmin < T < Tmax	100			
I_{IB}	Input bias current	V_{ICM} = 12 V, Vsense = 0		100	130	µA
		Tmin < T < Tmax			140	
		V_{ICM} = 48 V, Vsense = 0		200	230	
		Tmin < T < Tmax			240	
|Vsense|	Vsense operating range with Eg ≤ 0.3% (2)	TSC2020			123.8	mV
		Tmin < T < Tmax			123.6	
		TSC2021			49.1	
		Tmin < T < Tmax			48.8	
		TSC2022			24.1	
		Tmin < T < Tmax			23.9	
Output						
G	Gain	TSC2020		20		V/V
		TSC2021		50		
		TSC2022		100		
Eg	Gain error	TSC2020		0.01	0.3	%
		ΔV_{OUT} = 100 mV to (V_{CC} - 100 mV)			0.35	
		Tmin < T < Tmax				
		TSC2021		0.01	0.4	
		ΔV_{OUT} = 100 mV to (V_{CC} - 100 mV)			0.4	
		Tmin < T < Tmax				
		TSC2022		0.01	0.42	
		ΔV_{OUT} = 100 mV to (V_{CC} - 100 mV)			0.42	
		Tmin < T < Tmax				
ΔEg/ΔT	Gain error drift	Tmin < T < Tmax			3.5	ppm/°C
NLE	Linearity error	V_{ICM} = - 4 to 100 V		0.01		%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC} - V_{OH}	Drop voltage output high	Isource = 0.2 mA		11	25	mV
		Tmin < T < Tmax			35	
		Isource = 2 mA		115	150	
		Tmin < T < Tmax			200	
V_{OL}	Output voltage low	Isink = 0.2 mA		24	40	
		Tmin < T < Tmax			55	
		Isink = 2 mA		200	240	
		Tmin < T < Tmax			390	
I_{OUT}	Output current	Sink mode	8	12.5	18	mA
		Tmin < T < Tmax	5		24	
		Source mode	10	14.5	25	
		Tmin < T < Tmax	5		30	
Reg Load	Load regulation	I_{OUT} = -5 to +5 mA		0.2	1.5	$\frac{mV}{mA}$
C_L	Maximum capacitive load	No sustained oscillation		1		nF
Offset adjustment						
RT	V_{REF} gain	OUT/V_{REF} gain for either V_{REF} pin		0.5		V/V
Acc	Accuracy, RT	One V_{REF} pin connected to V_{CC}, the other to GND		0.2		%
Dynamic performances						
BW	Small signal -3 dB bandwidth	R_L = 10 kΩ, C_L = 100 pF	350	650		kHz
		Tmin < T < Tmax	350			
SR	Slew rate	C_L = 100 pF				V/µs
		TSC2020, Vsense = 108 mV	1.1	1.8		
		TSC2020, Tmin < T < Tmax	1			
		TSC2021, Vsense = 43 mV	1.5	2.4		
		TSC2021, Tmin < T < Tmax	1.4			
		TSC2022, Vsense = 22 mV	1.9	3		
		TSC2022, Tmin < T < Tmax	1.8			
E_N	Spectral density (RTI) (1)	f = 1 kHz		63		nV/√Hz

1. *RTI stands for "Related to input."*
2. *Vsense = (Vin+) – (Vin-).*

Table 5. Electrical characteristics - V_{CC} = 5 V, V_{ICM} = 48 V, T = 25 °C (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power supply						
I_{CC}	Current consumption	V_{ICM} = -4 to 100 V		1.8	2.4	mA
		Tmin < T < Tmax			2.4	
Input						
|Vos|	Offset voltage (RTI) (1)	V_{ICM} = 12 V, V_{REF} = 2.5 V			150	µV
		Tmin < T < Tmax			200	
		V_{ICM} = 48 V, V_{REF} = 2.5 V			400	
		Tmin < T < Tmax			500	
|ΔVos/ΔT|	Offset drift vs. temperature	V_{ICM} = 12 V, Tmin < T < Tmax			0.5	µV/°C
		V_{ICM} = 48 V, Tmin < T < Tmax			1	
CMR	Common-mode rejection	V_{ICM} = -4 to 100 V, DC mode	100	112		dB
		Tmin < T < Tmax	100			
SVR	Supply voltage rejection	V_{CC} = 2.7 to 5.5 V	100	118		dB
		Tmin < T < Tmax	100			
I_{IB}	Input bias current	V_{ICM} = 12 V, Vsense = 0		100	130	µA
		Tmin < T < Tmax			140	
		V_{ICM} = 48 V, Vsense = 0		200	230	
		Tmin < T < Tmax			240	
Vsense	Vsense operating range with Eg ≤ 0.3% (2)	TSC2020			238.5	mV
		Tmin < T < Tmax			238.2	
		TSC2021			94.9	
		Tmin < T < Tmax			94.7	
		TSC2022			47.1	
		Tmin < T < Tmax			46.8	
Output						
G	Gain	TSC2020		20		V/V
		TSC2021		50		
		TSC2022		100		
Eg	Gain error	TSC2020		0.01	0.3	%
		ΔV_{OUT} = 100 mV to (V_{CC} - 100 mV)			0.35	
		Tmin < T < Tmax				
		TSC2021		0.01	0.4	
		ΔV_{OUT} = 100 mV to (V_{CC} - 100 mV)			0.4	
		Tmin < T < Tmax				
		TSC2022		0.01	0.42	
		ΔV_{OUT} = 100 mV to (V_{CC} - 100 mV)			0.42	
		Tmin < T < Tmax				
ΔEg/ΔT	Gain error drift	Tmin < T < Tmax			3.5	ppm/°C
NLE	Linearity error	V_{ICM} = - 4 to 100 V		0.01		%

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC} - V_{OH}	Drop voltage output	Isource = 0.2 mA		18	35	mV
		Tmin < T < Tmax			45	
		Isource = 2 mA		122	155	
		Tmin < T < Tmax			210	
V_{OL}	Output voltage low	Isink = 0.2 mA		35	50	
		Tmin < T < Tmax			70	
		Isink = 2 mA		217	250	
		Tmin < T < Tmax			400	
I_{OUT}	Output current	Sink mode	8	13.5	20	mA
		Tmin < T < Tmax	5		24	
		Source mode	10	14.5	25	
		Tmin < T < Tmax	5		30	
Reg load	Load regulation	I_{OUT} = -5 to +5 mA		0.2	1.5	$\frac{mV}{mA}$
Offset adjustment						
RT	V_{REF} gain	OUT/V_{REF} gain for either V_{REF} pin		0.5		V/V
Acc	Accuracy, RT	One V_{REF} pin connected to V_{CC}, the other to GND		0.2		%
Dynamic performances						
BW	Small signal -3 dB bandwidth	R_L = 10 kΩ, C_L = 100 pF	450	700		kHz
		Tmin < T < Tmax	450			
SR	Slew rate	C_L = 100 pF				V/µs
		TSC2020, Vsense = 200 mV	1.4	2		
		TSC2020, Tmin < T < Tmax	1.2			
		TSC2021, Vsense = 80 mV	1.7	2.8		
		TSC2021, Tmin < T < Tmax	1.6			
		TSC2022, Vsense = 40 mV	2.4	3.9		
		TSC2022, Tmin < T < Tmax	2.2			
EN	Spectral density (RTI) (1)	f = 1 kHz		53		nV/√Hz

1. *RTI stands for "Related to input."*
2. *Vsense = (Vin+) – (Vin-).*

4 Typical characteristics

TSC2020 is used for typical characteristics, unless otherwise specified.

Figure 3. Input offset production distribution

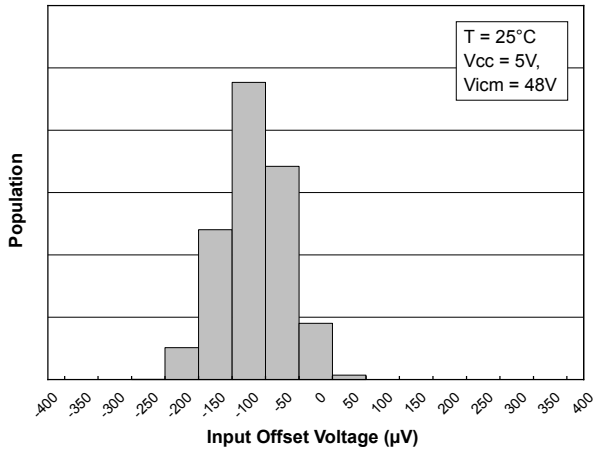

Figure 4. Gain error production distribution

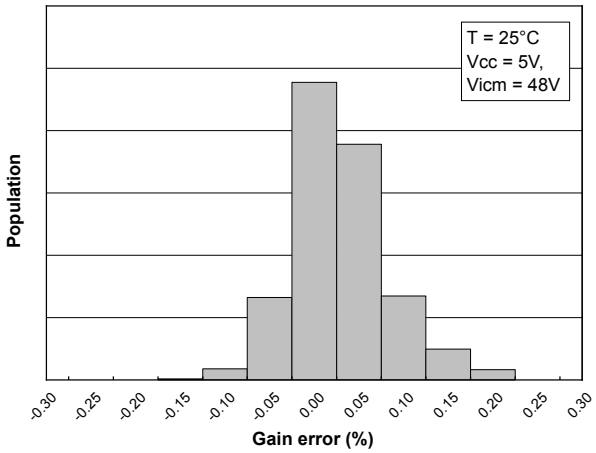

Figure 5. Common-mode rejection ratio production distribution

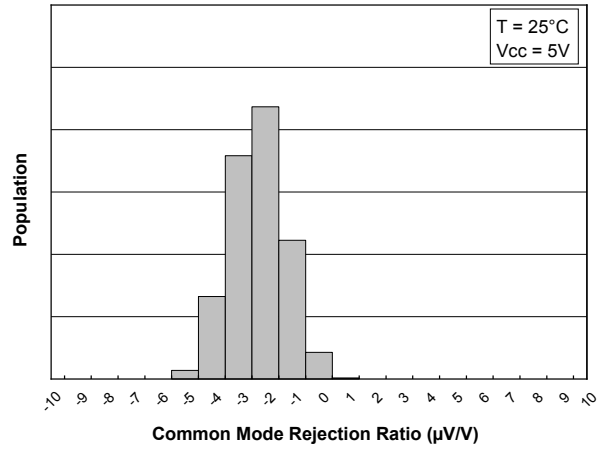

Figure 6. Supply current vs. supply voltage

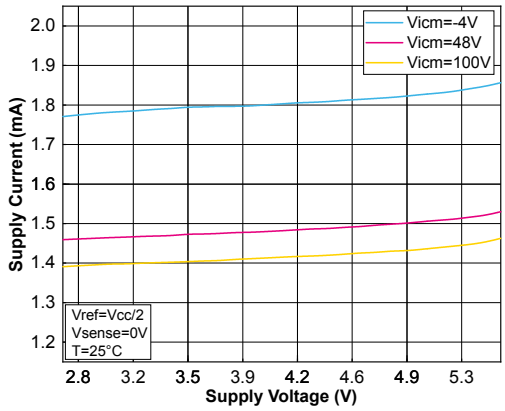

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Figure 7. Supply current vs. input common-mode

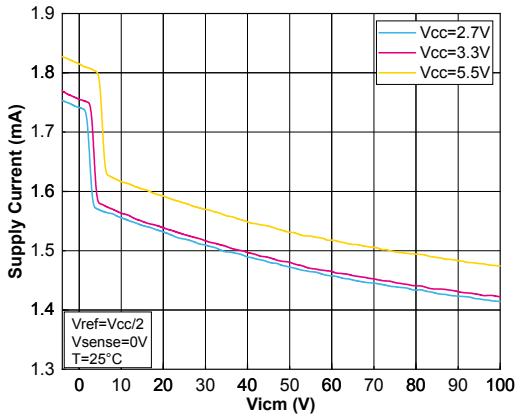


Figure 8. Supply current vs. temperature

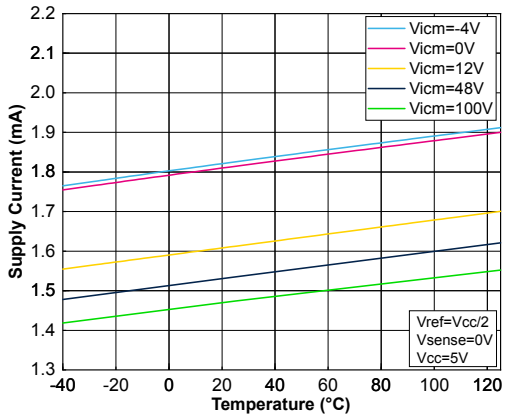


Figure 9. Input bias current vs. input common-mode

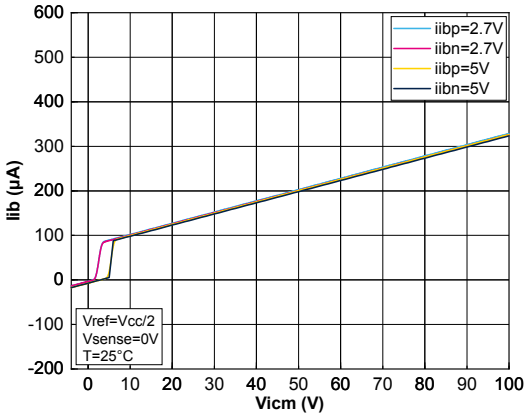


Figure 10. Input bias current vs. temperature

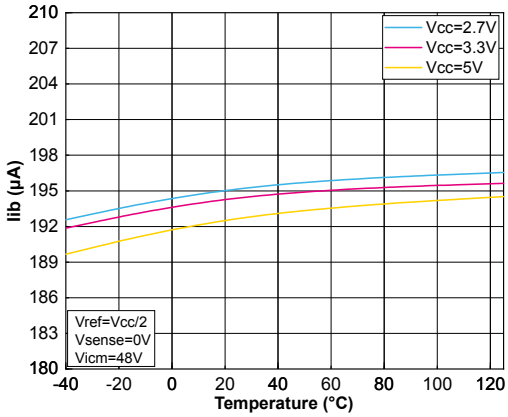


Figure 11. Input bias current vs. input common-mode

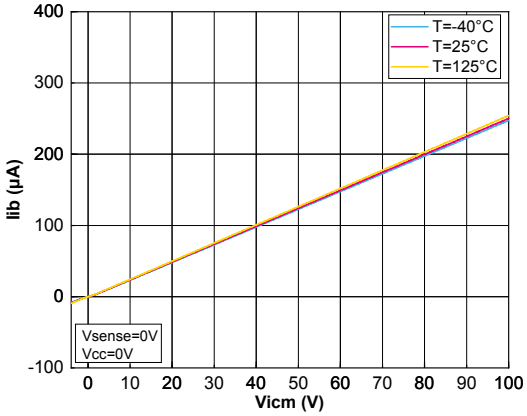


Figure 12. Input bias current vs. Vsense

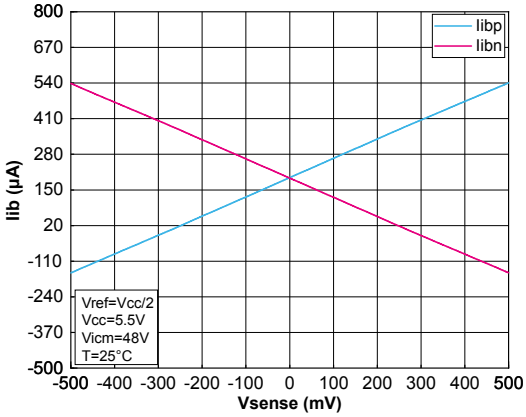


Figure 13. Input offset voltage vs. temperature

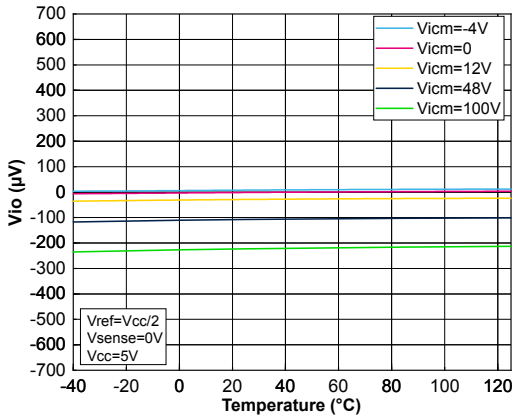


Figure 14. Input offset voltage vs. input common-mode with V_{CC} = 5.5 V

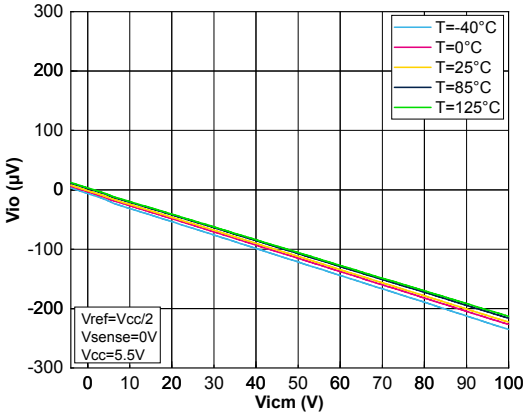


Figure 15. Input offset voltage vs. input common-mode with V_{CC} = 2.7 V

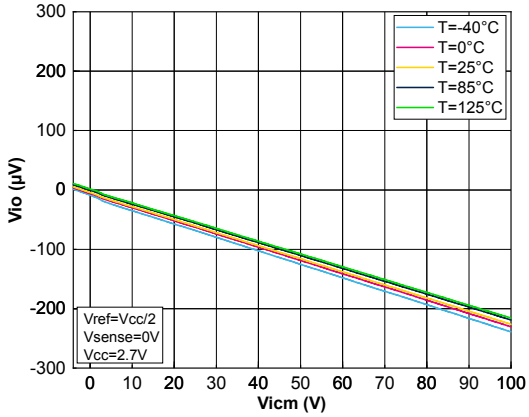


Figure 16. Input offset voltage vs. supply voltage

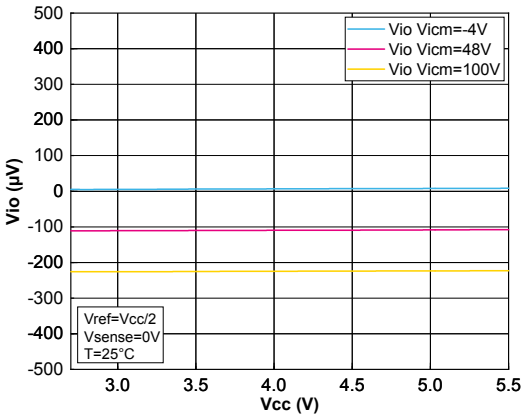


Figure 17. Output current vs. output voltage

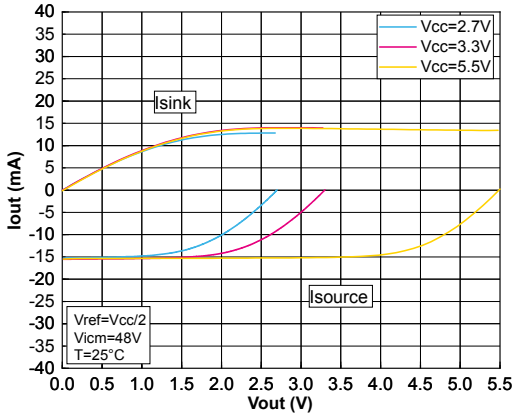


Figure 18. Output current vs. temperature with V_{CC} = 5.5 V

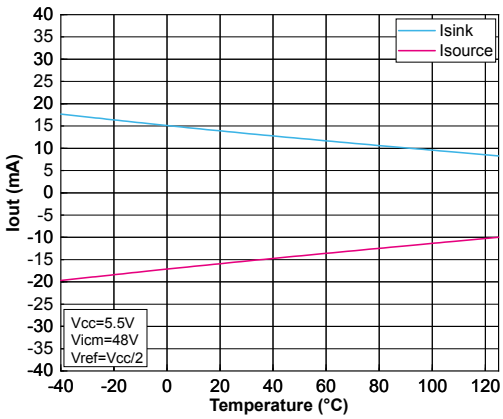


Figure 19. Output current vs. temperature with V_{CC} = 2.7 V

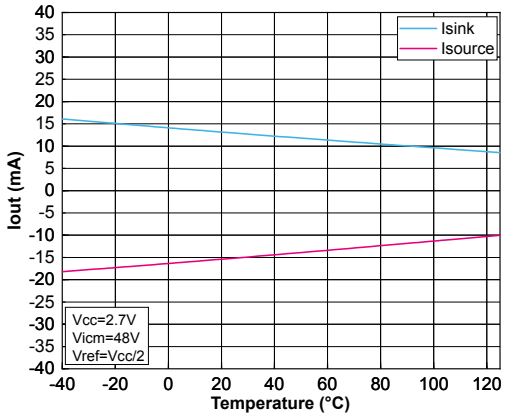


Figure 20. V_{oh} and V_{ol} vs. temperature with V_{CC} = 5.5 V

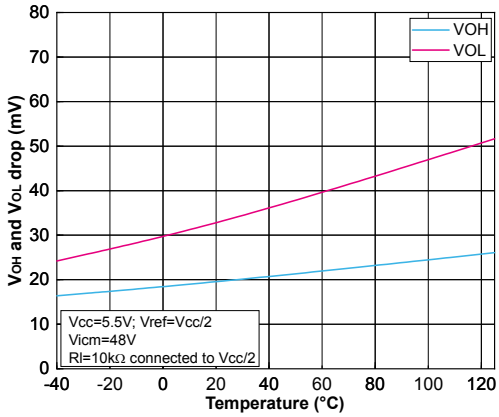


Figure 21. V_{oh} and V_{ol} vs. temperature with V_{CC} = 2.7 V

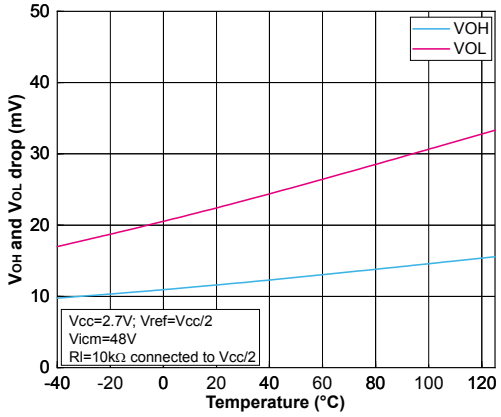


Figure 22. Linearity vs. Vsense with V_{CC} = 5.5 V

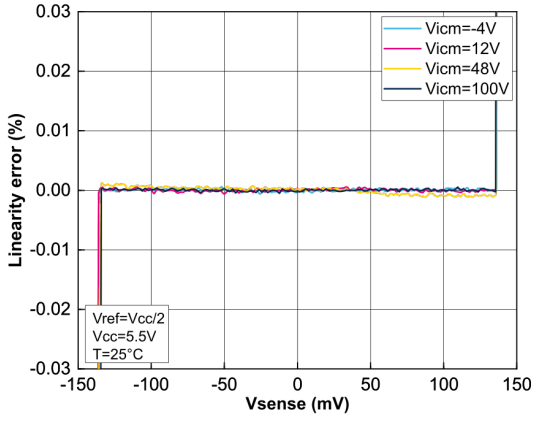


Figure 23. Linearity vs. Vsense

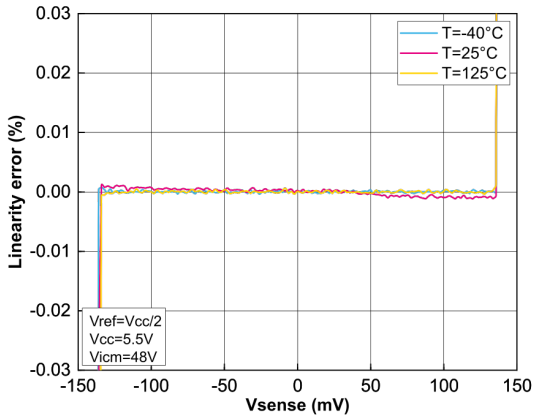


Figure 24. Gain error vs. input common-mode different V_{CC}

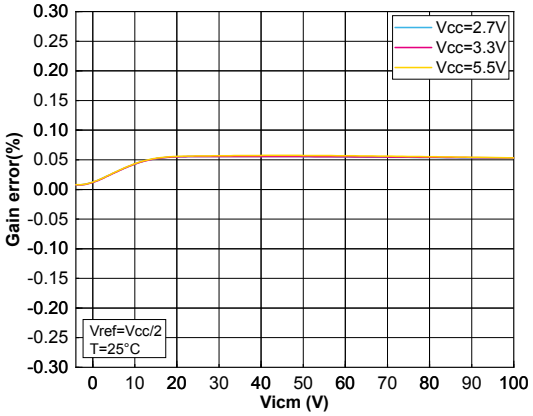


Figure 25. Gain error vs. input common-mode voltage different temperature

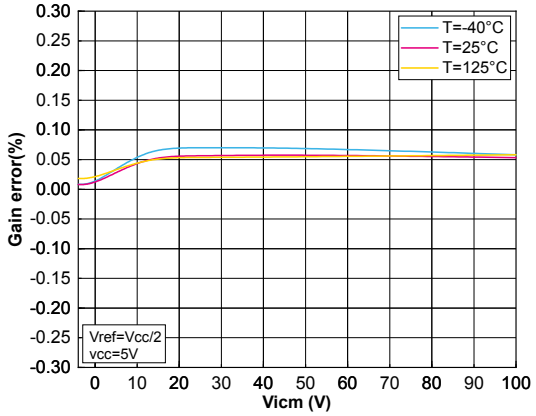


Figure 26. Load regulation with V_{CC} = 5 V

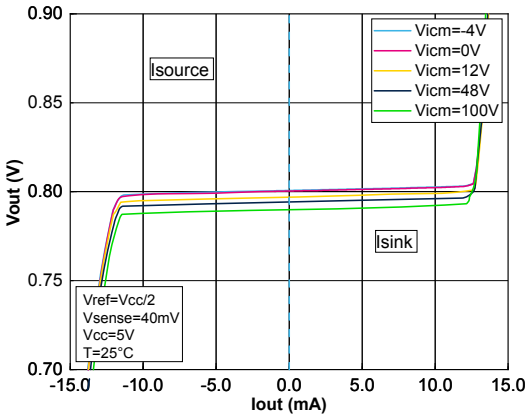


Figure 27. Gain vs. frequency

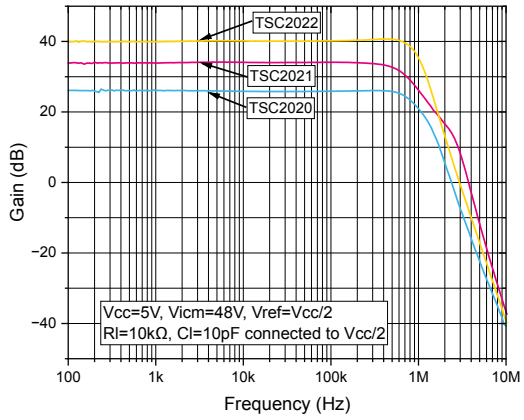


Figure 28. Gain vs. frequency with different capacitive load

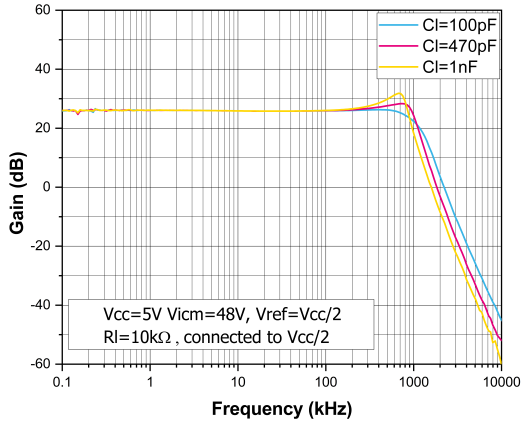


Figure 29. Gain vs. frequency with different capacitive load (TSC2021)

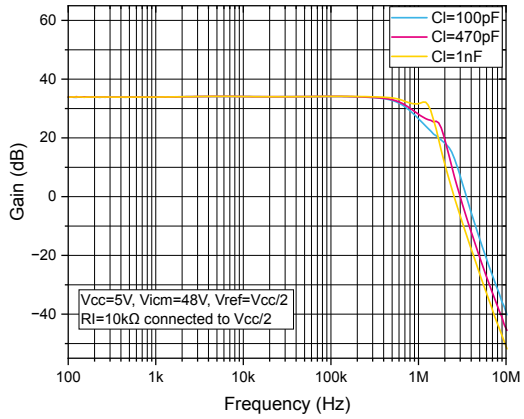


Figure 30. Gain vs. frequency with different capacitive load (TSC2022)

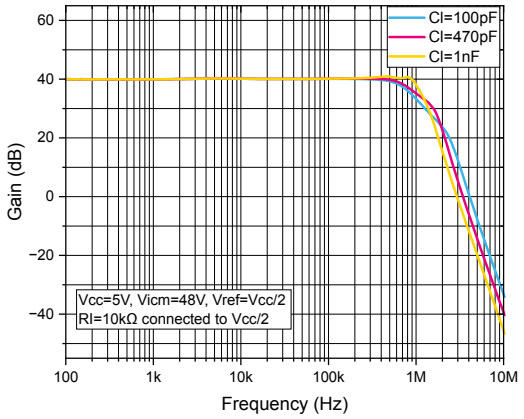


Figure 31. Bandwidth vs. input common-mode

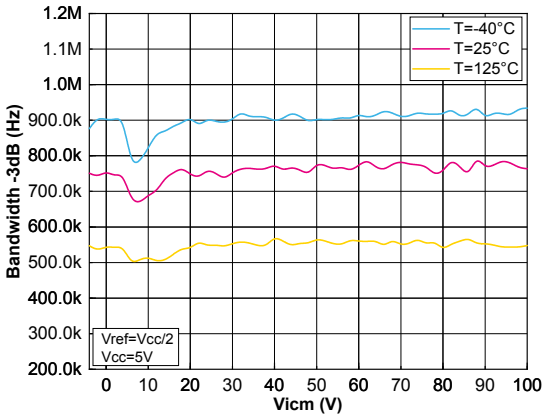


Figure 32. Overshoot vs. capacitive load

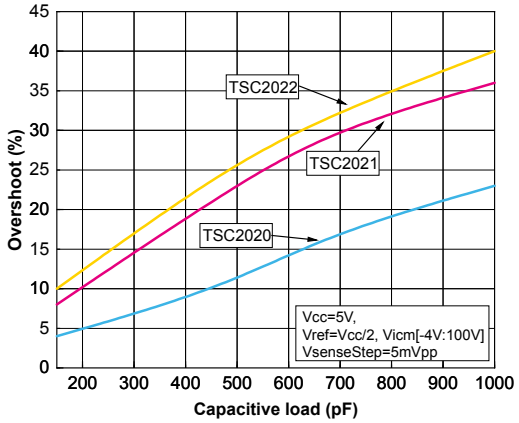


Figure 33. Small signal response with V_{CC} = 5 V

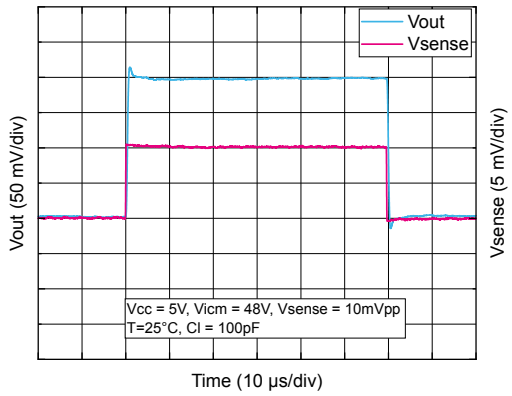


Figure 34. Large signal response with V_{CC} = 5 V

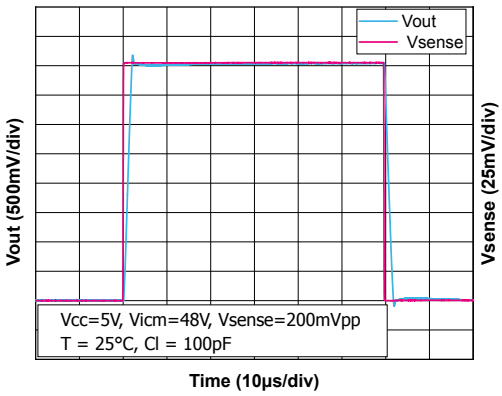


Figure 35. Large signal response with V_{CC} = 5 V (TSC2021)

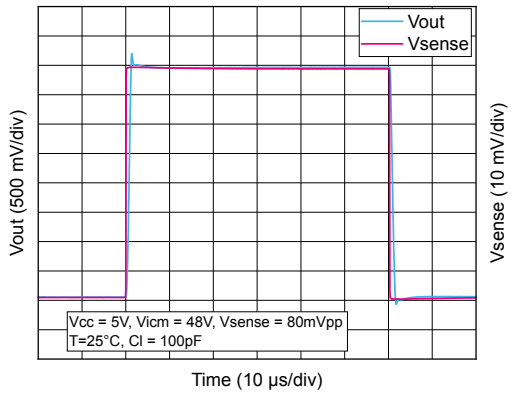


Figure 36. Large signal response with V_{CC} = 5 V (TSC2022)

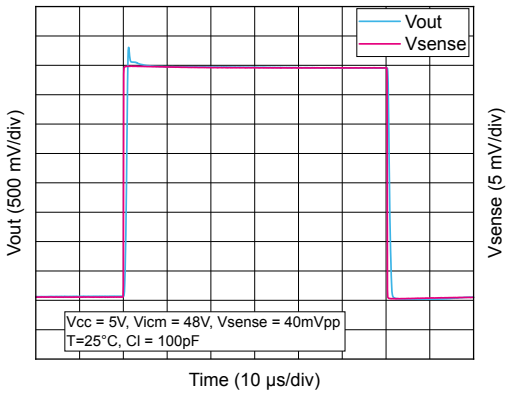


Figure 37. Positive settling time 1% vs. input common-mode

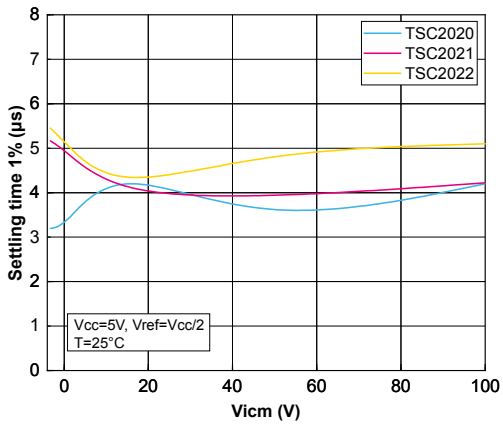


Figure 38. Negative settling time 1% vs. input common-mode

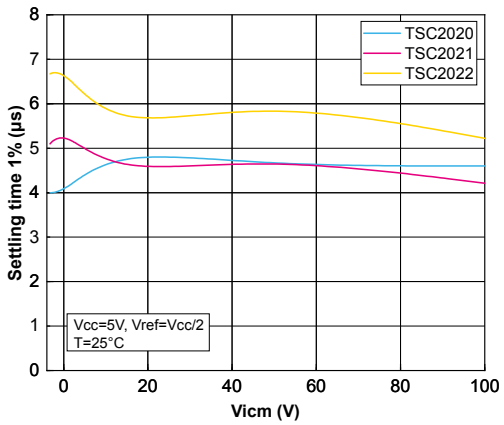


Figure 39. 48 V common-mode positive step response recovery

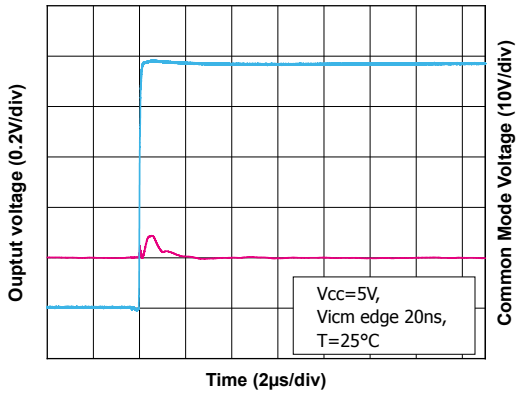


Figure 40. 48 V common-mode negative step response recovery

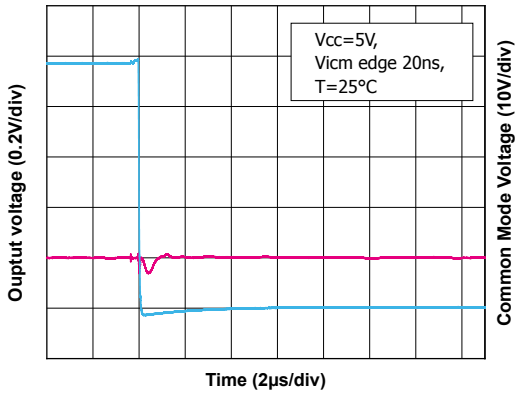


Figure 41. 100 V common-mode positive step response recovery

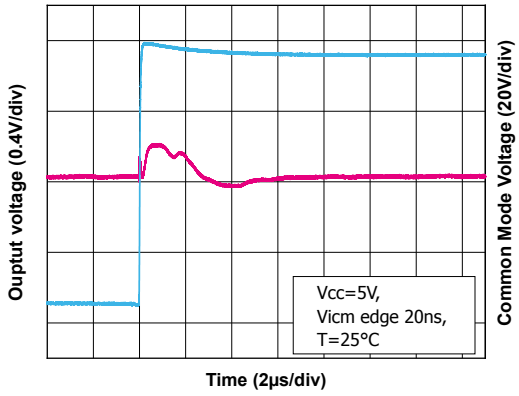


Figure 42. 100 V common-mode negative step response recovery

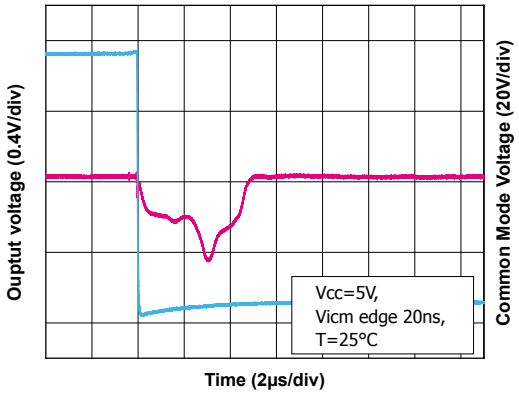


Figure 43. PSRR vs. frequency

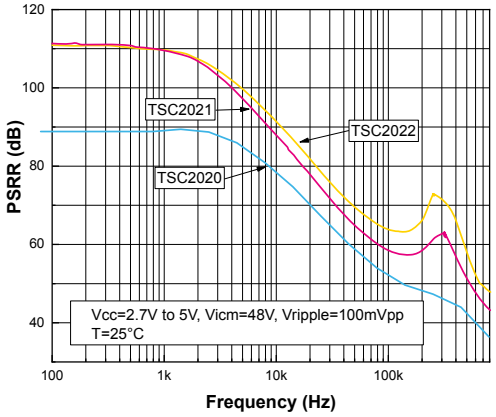


Figure 44. CMRR vs. frequency

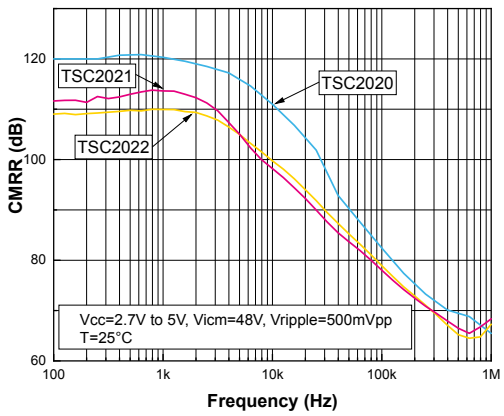


Figure 45. Positive overvoltage recovery

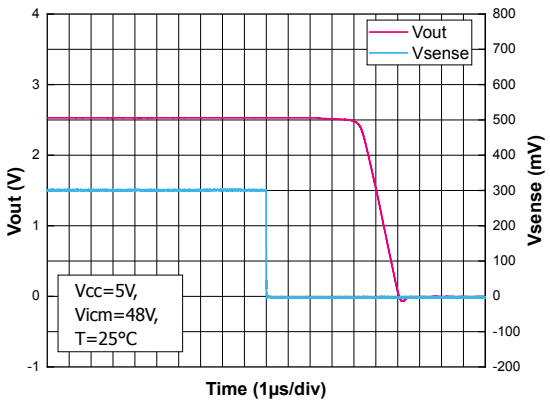


Figure 46. Negative overvoltage recovery

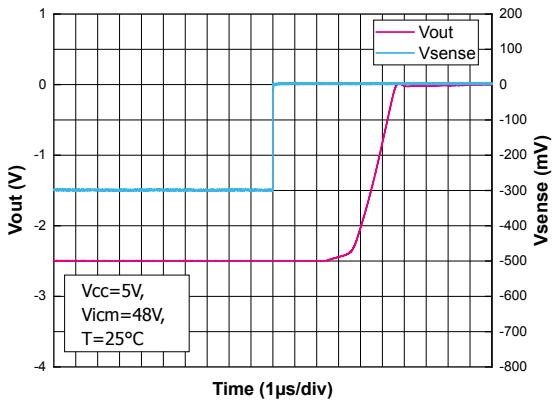


Figure 47. Overvoltage recovery vs input common-mode, V_{CC} = 5 V

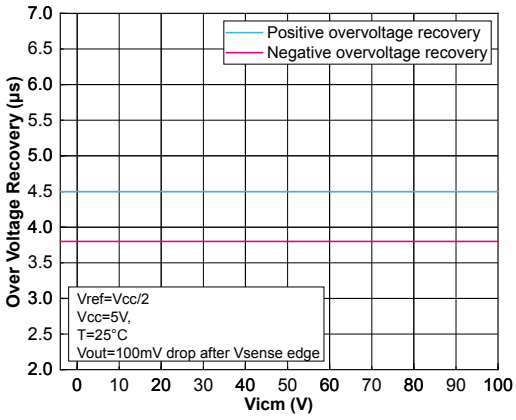


Figure 48. Noise vs. frequency

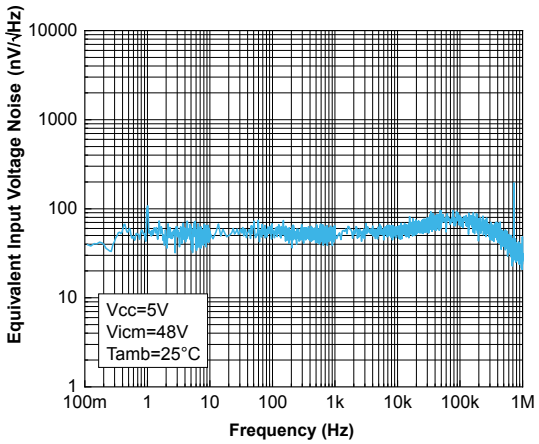


Figure 49. 0.1 Hz to 10 Hz voltage noise

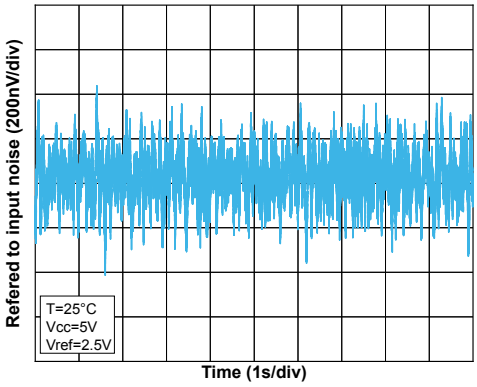


Figure 50. Power up time delay

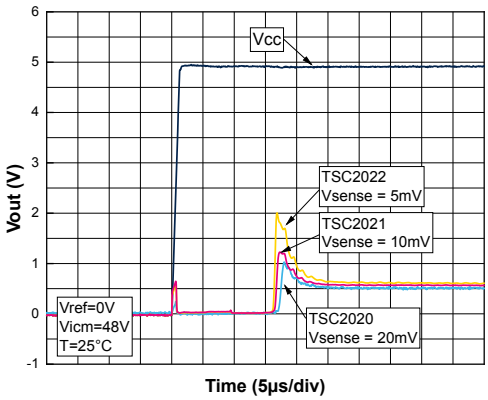
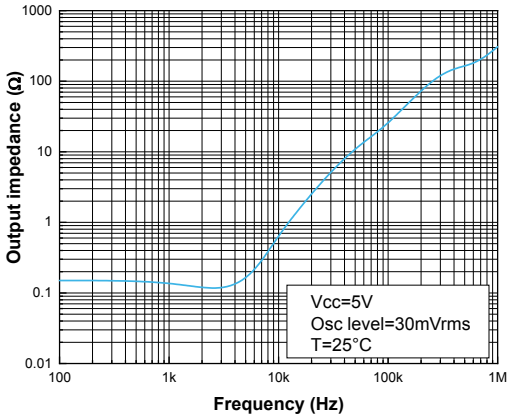


Figure 51. Output impedance vs. frequency



5 Application information

5.1 Overview

The TSC202x family is a current sense amplifier specially designed to accurately measure current by amplifying the voltage across a shunt resistor connected to its input. It is a zero-drift topology, allowing to reach a high CMRR level of 100 dB min. and a high level of input offset voltage of 200 µV at 12 V common mode voltage and over temperature.

Multiple fixed gain versions are available (x20, x50, x100) for design optimization. Thanks to the use of a thin film resistor, the TSC202x offers an extremely precise gain and very high CMRR performance even in a high frequency range. Moreover, there is the possibility to fix the output common mode voltage, allowing the TSC202x to be either used as a unidirectional or bidirectional current sensing amplifier.

The TSC202x provides an extended input common range from -4 V below negative supply voltage, and up to 100 V, allowing either low-side or high-side current sensing, while TSC202x devices can operate from 2.7 to 5.5 V.

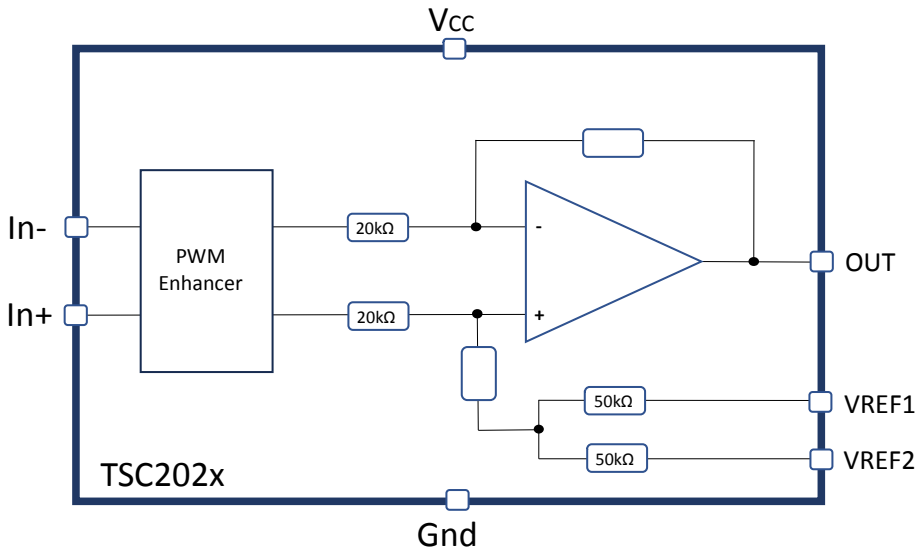
The TSC202x embedded a system to optimize the PWM rejection, allowing to reduce the effect of fast input common mode voltage variation on the output signal.

The parameters are very stable in the full VCC range, and several characterization curves show the TSC2020 device characteristics at 2.7 V and 5.0 V. Additionally, the main specifications are ensured in extended temperature ranges from -40 to 125 °C.

5.2 Theory of operation

The main particularity of the TSC202x is the ability to work with a wide input common mode voltage. It is an excellent device to work with a 48 V application as the TSC202x can support and measure the current online at a voltage up to 100 V without any additional protective components. It is also a good candidate for use in a low-side configuration. And thanks to its ability to work with a negative common mode voltage down to -4 V, it can support, without any additional protection, fast current variation into a shunt, which is always a bit inductive. The TSC202x family embedded a PWM enhancer, allowing it to be used in applications dealing with fast variation of input common mode voltage as motor control or solenoid valve. Its good DC performance makes the TSC202x an excellent device to measure accurately the current. Figure 52. Functional block diagram depicts a global overview of the TSC202x.

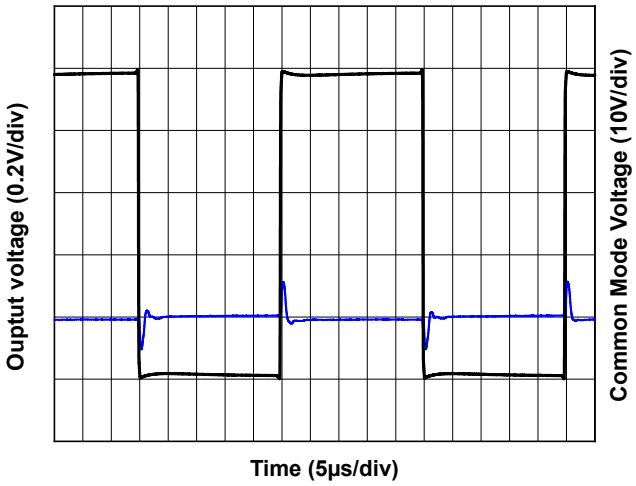
Figure 52. Functional block diagram



5.3 PWM enhancer

The TSC202x current sensing integrates a detection of transient signal on the input common bus to reduce the impact of such an event on the output pin. Such large ΔV/ΔT common mode signals are commonly seen in applications such as motor control when the current sensing is used in inline sensing. See Figure 70 or solenoid drive. Figure 53. Output response to large ΔV/ΔT input common mode signals shows the TSC2020 output voltage response where the input pins are submitted to a 20 kHz PWM with 0 - 48 V amplitude.

Figure 53. Output response to large ΔV/ΔT input common mode signals



The output impact to a fast input common mode variation is typically limited to hundreds mV during less than 3 µs, allowing it to work with a wide range of PWM duty cycle conditions in control motor applications.

5.4 Unidirectional / bidirectional operation

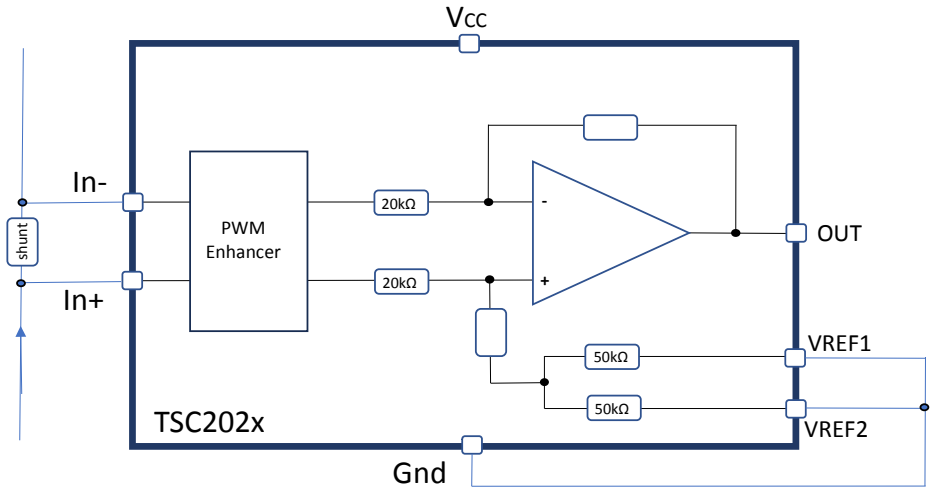
The TSC202x output common mode voltage level can be set thanks to voltages applied on the Vref1 and Vref2 pins. These two pins to set the device either in bidirectional or in unidirectional operation. The voltage applied on those pins must not exceed the V_{CC} range. There is no difference between both reference pins; the voltage can be applied to either one pin or the other without distinction.

- **Unidirectional operation**

Unidirectional mode of operation allows the device to measure the current through a shunt resistor in one direction only. The output reference can be ground or V_{CC} and can be set by using the Vref1 and Vref2 pins for adjustment.

- **Ground referenced**

Figure 54. Output referenced to ground



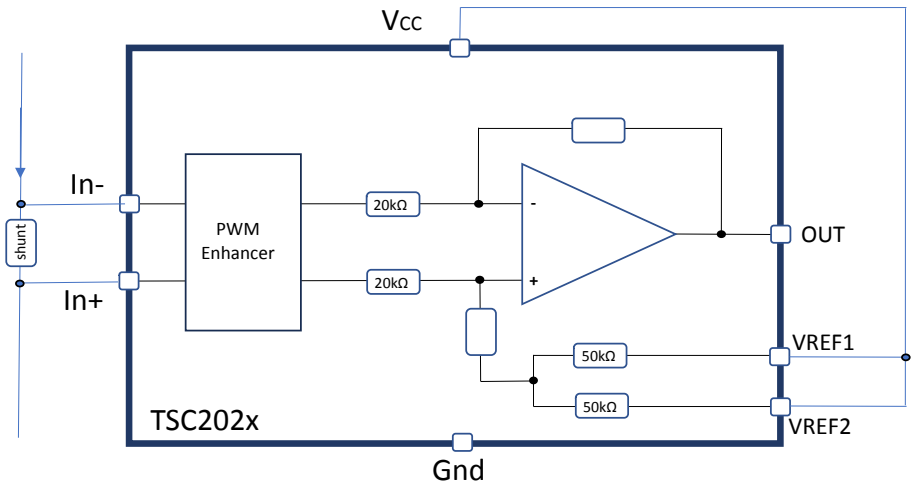
In the configuration described in Figure 54. Output referenced to ground, both the Vref1 pin and Vref2 pin are connected to the ground. The output common mode voltage is then automatically set to Gnd and the output voltage can be expressed as equation (1).

$$Vout = (IN_+ - IN_)*Gain \quad (1)$$

This configuration allows the full-scale output in unidirectional mode. It allows to measure a current flowing into the shunt from IN+ to IN-.

- **V_{CC} referenced**

Figure 55. Output referenced to V_{CC}



In the configuration described in Figure 55. Output referenced to V_{CC}, the Vref1 pin and Vref2 pin are connected to the V_{CC} power supply. The output common mode voltage is then automatically set to V_{CC} voltage and the output voltage can be expressed as equation (2):

$$Vout = (IN_+ - IN_)*Gain + Vcc \quad (2)$$

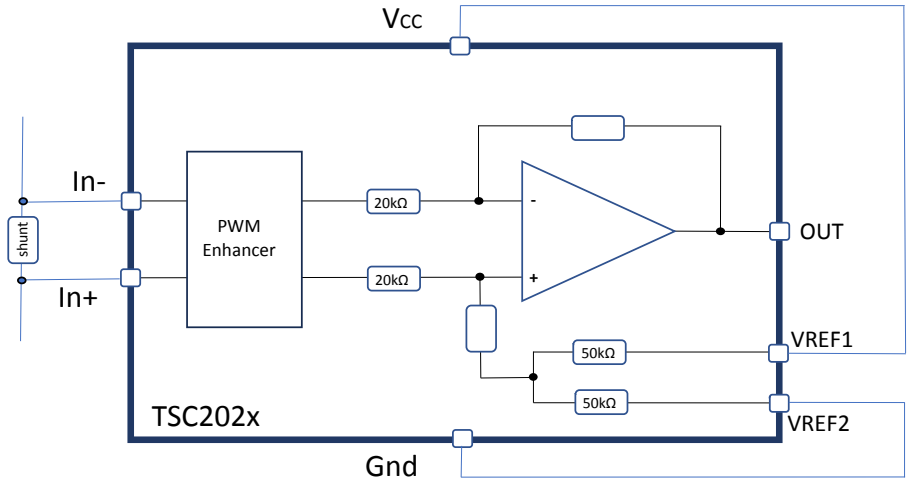
This configuration allows the full-scale output in unidirectional mode to measure a current flowing into the shunt from IN- to IN+.

- **Bidirectional operation**

Bidirectional mode of operation allows the device to measure currents through a shunt resistor in two directions. The output reference can be set anywhere within the power supply range. If the output common mode voltage is set at mid-range, the full-scale current measurement range is equal in both directions. This is achieved by connecting one Vref pin to VCC and the other Vref pin to Gnd as described in Figure 56. Split supply.

- **Split supply**

Figure 56. Split supply

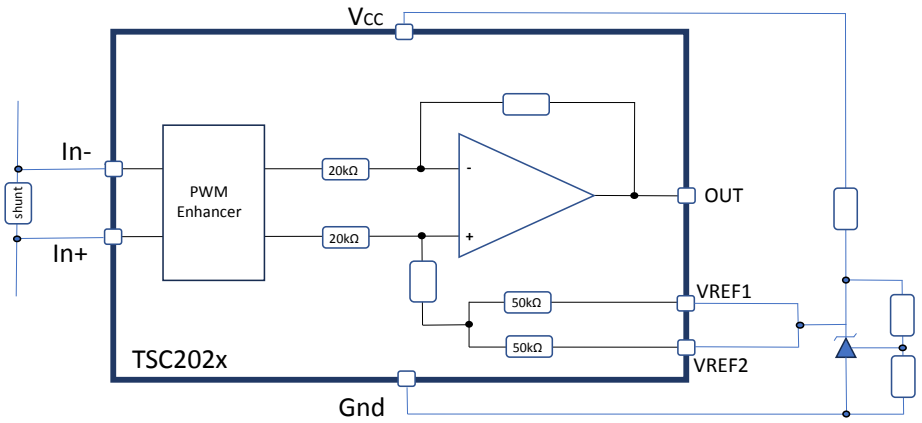


The significant advantage of this configuration is that the TSC202x can be used in bidirectional mode with an output common mode voltage set at the middle of the scale, with an accuracy of 0.2%, without any added external component or power supply. This configuration allows to create a mid-scale offset ratiometric to the power supply. The output voltage can be expressed as equation (3):

$$Vout = (IN_+ - IN_)*Gain + \frac{Vref1 + Vref2}{2} \quad (3)$$

- **External with a reference voltage**

Figure 57. External supply



It can be done by connecting both Vref pins to a voltage reference as described in Figure 57. External supply. Users can set the output in a non-symmetrical configuration, adjusting Vref according to user needs.

In this configuration, the Vref1 pin and Vref2 pin are connected to an adjustable reference voltage TS431. The output common mode voltage is then automatically set to the reference voltage when no current flows through the Rshunt resistance.

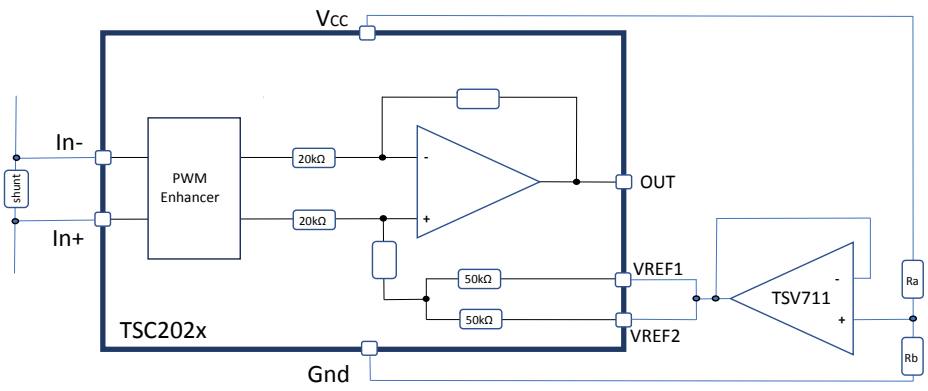
The output voltage can be expressed as equation (4).

$$Vout = (IN_+ - IN_)*Gain + Vref \quad (4)$$

- **External with a divider bridge**

It is recommended to buffer the resistor divider as depicted in Figure 58. Recommended schematic thanks to a precise op amp such as the TSV711.

Figure 58. Recommended schematic



The output voltage can be expressed as equation (6)

$$Vout = (IN_+ - IN_)*Gain + Vcc*\frac{Rb}{Ra + Rb} \quad (5)$$

When the output common mode voltage is supplied by an external power supply, to improve the output voltage measurement, it is recommended to measure the V_{out} differentially with respect to V_{ref} voltage. It provides the best CMRR measurement, the best noise immunity, and a more accurate V_{out} voltage. A decoupling capacitance of 1 nF minimum can be also added to better filter the power supply.

5.5 RSENSE selection

The selection of the shunt resistor is a tradeoff between dynamic range and power dissipation.

Generally, in high current sensing applications, the focus is to reduce the power dissipation (RI²) as much as possible by choosing the smallest value of shunt as $Rsense \leq \frac{Pmax}{Imax^2}$.

In low current applications the Rsense value could be higher, to minimize the impact of the offset voltage of the circuit on the accuracy measurement.

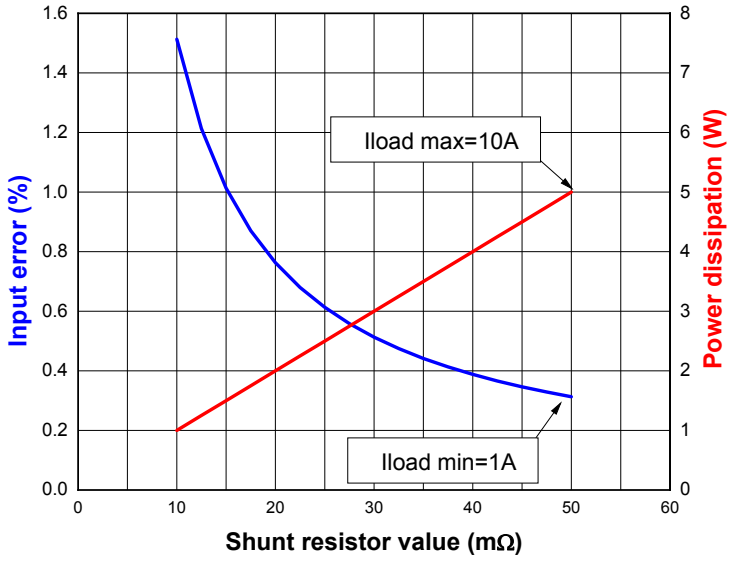
The tradeoff is mainly when a dynamic range of current to measure is large, meaning the ability to measure with the same shunt value low current to high current. Generally, the current full-scale (Imax-Imin) defines the shunt value thanks to the full output voltage range and the TSC202x gain. The TSC202x offers the possibility to work with full-scale ΔV_{out} = 100 mV to V_{cc} - 100 mV with maximum gain accuracy of 0.3%.

At first order, the full current range to measure through Rsense can be defined by equation 7, just by taking the gain error and input offset voltage as inaccuracy parameters:

$$Isense_full_scale*Rsense = \frac{Vcc - 200mV}{TSC_Gain(1 + Eg)} - \left|Vio\right| \quad (6)$$

Figure 59. Tradeoff between shunt resistance, power dissipation, and accuracy shows an example of the tradeoff between power dissipation and accuracy for the TSC2020 current sensing. It is considered a current to measure from 1 A to 10 A through different shunt values from 10 mΩ up to 50 mΩ. The maximum current (10 A) gives an idea of the worst-case power dissipation expected, whereas the lowest current (1 A) gives a first order idea of the error that can be expected on the output.

Figure 59. Tradeoff between shunt resistance, power dissipation, and accuracy



5.6 Input offset voltage drift over temperature

The maximum input offset voltage drift over temperature is defined as the offset variation related to the offset value measured at 25 °C. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using equation 8.

$$\frac{\Delta V_{io}}{\Delta T} = \max \left| \frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C} \right| \quad (7)$$

Where T = -40 °C and 125 °C.

The TSC202x datasheet maximum value is guaranteed by measurements on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.3.

5.7 Error calculation

The principal source of error such as input offset voltage, gain error, common mode rejection ratio, are described separately in the electrical characteristics. This section summarizes the most important error to consider during a design phase.

- **Input offset voltage error**

Equation 9 depicted a first order error calculation just by considering the input offset voltage. In a temperature environment, also taken into consideration is the deviation of the Vio and the error linked to the input offset on the output voltage can be written as equation 9.

$$Vio\ Error = (\pm Vio \pm \Delta Vio/\Delta T) * Gain \quad (8)$$

- **Gain error and shunt resistance accuracy**

$$Gain\ error = Gain(1 + \varepsilon gain) \quad (9)$$

$$Rsense\ error = Gain(1 + \varepsilon Rsense) \quad (10)$$

Where εgain is the gain error 0.35% max. for the TSC202x.

Where εRsense is the shunt resistance error. Shunt resistors from 5 mΩ to 100 mΩ are available with 1% accuracy or better.

- **CMR error**

In the electrical characteristics CMR is specified at one input common mode voltage. So, in order to take into consideration the variation of the input voltage offset depending on the Vicm, the calculus must be done till this known point. Let us take the V_{icm} = 12 V as a reference point.

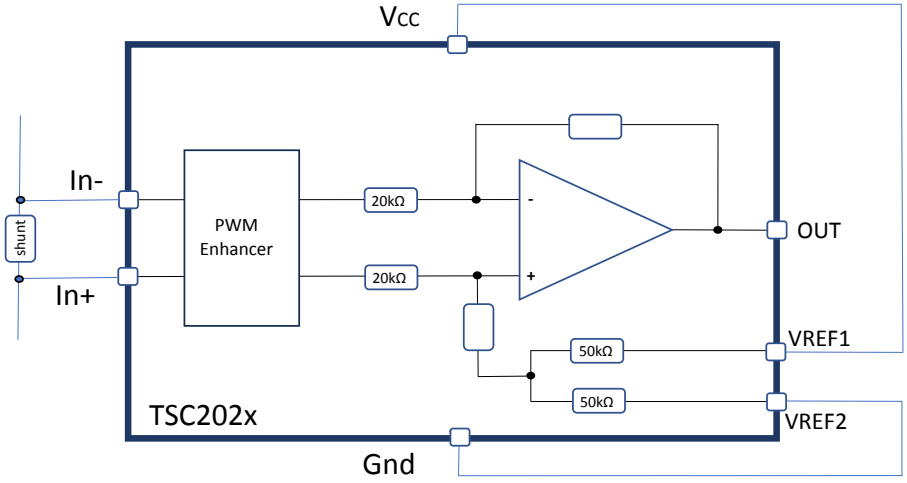
Therefore, the error on V_{out} due to a common mode voltage variation can be written as equation 12:

$$CMR\ error = \pm \frac{Vicm - 12V}{CMR} * Gain \quad (11)$$

- **Output common mode error**

This error can be considered when the output common mode voltage is set as suggested in Figure 60. Schematic for V_{ocm} error, and so by using the internal divider bridge. Otherwise, it is important to consider the error linked to the voltage source applied on the Vref1 pin and Vref2 pin.

Figure 60. **Schematic for V_{ocm} error**



The divider bridge is made by two resistances of 50 kΩ given an output common mode voltage of $\frac{Vref1 + Vref2}{2}$.
Due to a small mismatch of the internal resistance, the error on the output common mode voltage can be described as equation 13:

$$Vocm = \left(\frac{Vref1 + Vref2}{2}\right).(1 + \varepsilon Acc) \quad (12)$$

Where εAcc is the accuracy referred to the output with a typical value of 0.2%.

- **Noise**

Figure 48 expresses the TSC2020 noise referred to input. This device shows that only a white noise density is 53 nV / $\sqrt{Hz}$, overall TSC2020 bandwidth.
Considering that there is no additional filter on the TSC2020 and it is only bandwidth limited, it can be considered that at over 700 kHz, there is an attenuation of the noise with a first order filtering. So, the equivalent noise bandwidth is $700kHz.\frac{\pi}{2}$.

The RMS value of the output noise is the integration of the spectral noise over the bandwidth of interest and can be expressed as equation 14:

$$enRMS = \left(\sqrt{\int_{0.1}^{700000.\frac{\pi}{2}} \left(53.10^{-9}\right)^2 df}\right) * Gain \quad (13)$$

- **Total error**

The maximum total error expected on the output of the device can be considered as the sum of the different source described just above by considering all the maximum parameters of the datasheet. This approach is very pessimistic, and the chance to obtain all the maximum parameter values on a same die is extremely low, even null. To have a good picture of the maximum possible error on the output, total error can be determined by using a simplified statistical approach as the root-sum-of-the-squares (RSS), a method to combine the error terms.
So, the error can be written as equation 15.

$$Error_Rss = \sqrt{(\varepsilon G)^2 + \left(\frac{Vio}{Rshunt.I}\right)^2 + \left(\frac{\frac{Vicm - 12V}{CMRR}}{Rshunt.I}\right)^2 + \left(\frac{Vref.(\varepsilon ref)}{G.Rshunt.I}\right)^2} \quad (14)$$

Note that the input bias currents are not considered in this section, as it has been considered that this current is already integrated in the Vsense. The TSC2020 cannot measure current in the same order as input bias current (several hundreds of µA).

Linearity is not considered in the error calculus as it represents only 0.01% of error and is negligible. Nevertheless, as the gain error has been calculated thanks to the best-fit line approach, it gives the information that the gain error can be relatively constant throughout the linear input range of the TSC2020.

Equation 15 has been described for a temperature of 25 °C. With temperature variation, the DV_{IO}/DT error term must certainly be added. And if the power supply is susceptible to change, the SVR parameter must also be considered. For more information about the expected error on a current sensing output you can refer to the application note AN5849. The shunt accuracy must also be taken into consideration.

- **Example**

Let us take an example to get a better understanding of the maximum total error that can happen on the output of the TSC2020 (x20).

- **Use case:**
  - V_{CC} = 5 V
  - V_{icm} = 24 V
  - V_{ocm} = 2.5 V
  - Temperature = 25 °C
  - I_{load} = 10 A
  - Shunt 5 mΩ

Theoretically, the expected output voltage should be $V_{out} = R_{shunt} * I_{load} * 20 + V_{ocm}$ = 3.5 V.

From the above equations, let us detail all the error terms by using the maximum value of the electrical characteristic (when available). The % error on output in the following table is expressed in reference of $V_{out} - V_{ref}$, so in this typical example: 1 V.

Error source	Calculus	Output voltage error	% error on output
Gain error	$20*5.10^{-3}*10*0.3\%$	3 mV	0.3%
Vio error	$20*150\mu V$	3 mV	0.3%
CMRR error	$20*\frac{24V-12V}{\frac{100}{10^{20}}}$	2.4 mV	0.2%
Vocm error	$2.5*0.2\%$	5 mV	0.5%
Noise	$20*\frac{53nV}{\sqrt{Hz}}\sqrt{700kHz*\frac{\pi}{2}-0.1Hz}$	1.1 mVrms	0.3% (1)

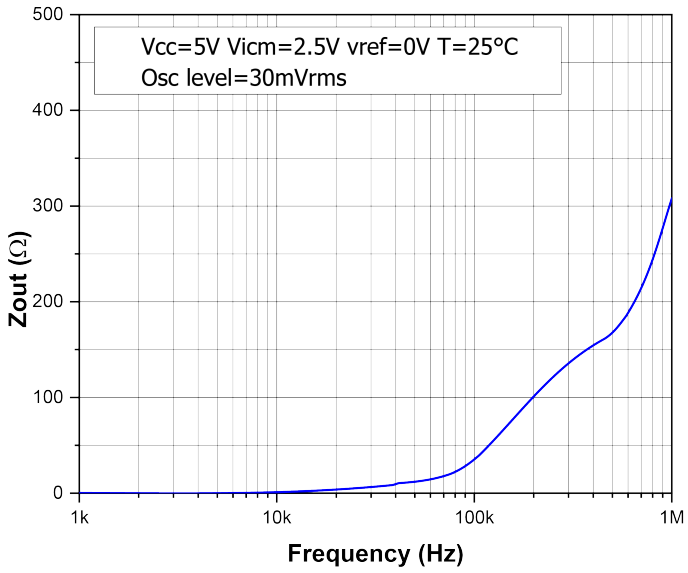
1. *The percentage is based on the voltage peak value and is 3 times the RMS value.*

An error of 0.75% can be expected on the output of the TSC2020 @ 25 °C for a current of 10 A flowing.

5.8 Input filtering

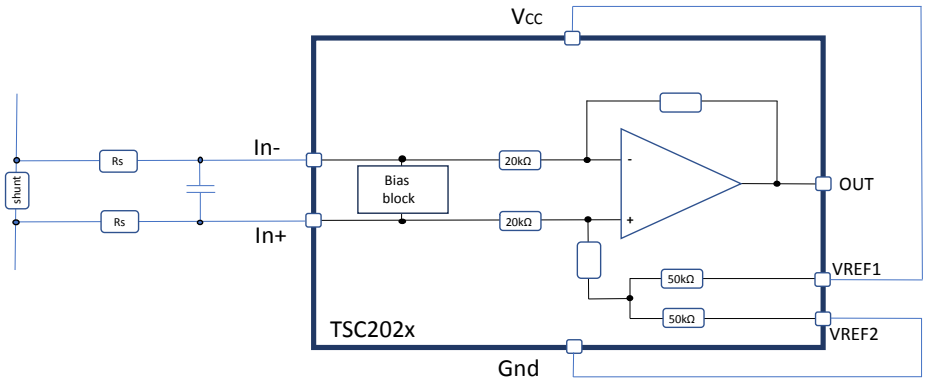
Although the TSC2020 does not require input filtering for good accuracy measurement, depending on application requirements a low-pass filter may be needed. In this case it is always better to filter the TSC2020 output rather than the input pins. Anyway, the TSC2020 output shows a low impedance even in high frequency shown in Figure 61. Zout vs. frequency, and adding an output filter certainly acts to increase the output impedance.

Figure 61. Zout vs. frequency



Adding resistances on the input pins creates an impedance mismatch with the internal bias block, which allows to correctly polarize the input stage when the common mode voltage is higher than the power supply voltage. The block diagram is described in Figure 62. Input filter.

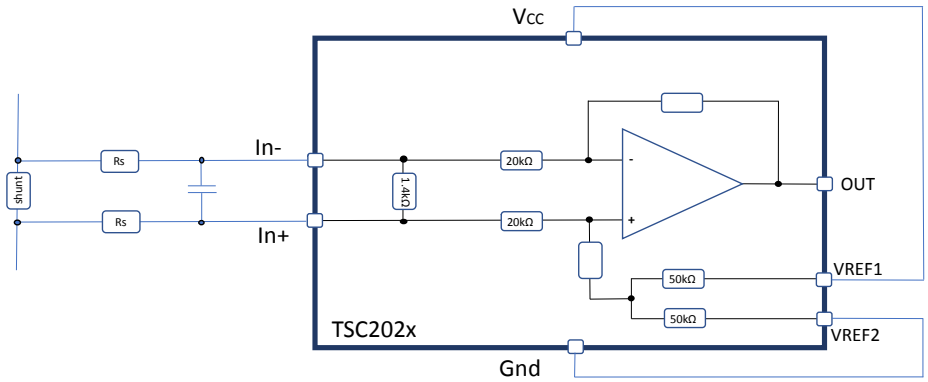
Figure 62. Input filter



When an input differential voltage is applied, this bias block presents a differential impedance of 1.4 kΩ as described by Figure 63. Differential input impedance. This mismatch has a direct impact on the gain accuracy, as described by equation 16.

$$Gain\ error = 1 - \frac{700}{Rs + 700} \quad (15)$$

Figure 63. Differential input impedance



In a second order due to the mismatch of the external serial resistance, an input offset voltage may also be added as depicted by equation 17:

$$\text{Input Offset voltage} = Rs \cdot 2 \cdot \varepsilon\alpha \cdot (Iib) \quad (16)$$

Where εα is the resistance precision.

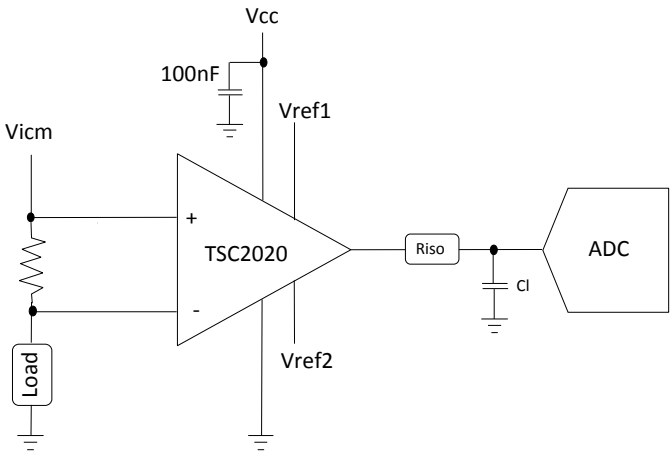
In order to limit error, it is advised to use serial resistance as low as possible on the input. 10 Ω or lower could be a good value.

By using a serial resistance of 10 Ω (±1%) on the input pins of the TSC2020 in a 48 V application (corresponding to an Iib = 200 µA), a gain error of 1.4% can appear and an added input offset of 40 µV.

5.9 Stability

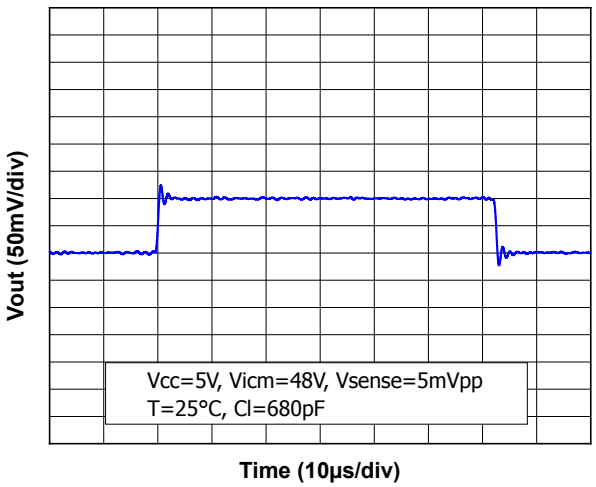
Driving large capacitive Cload can produce gain peaking in the frequency response, with overshoot and ringing in the step response. In order to smooth the output, a serial resistance Riso can be inserted between the TSC2020 output and the capacitive load as depicted by Figure 64. Serial resistance Riso.

Figure 64. Serial resistance Riso



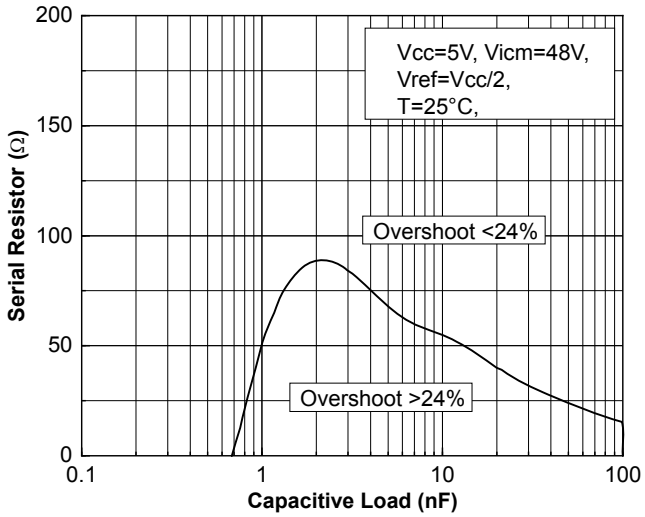
The criteria chosen to ensure the stability of the system is an overshoot lower than 24% to a small input step voltage. Figure 65. Stability criteria overshoot 24% shows the TSC2020 output response, loaded with 680 pF capacitor, to a 5 mV input step. It depicts the stability criteria acceptance with an overshoot lower than 24%.

Figure 65. Stability criteria overshoot 24%



For load capacitance higher than 680 pF, and in order to respect an overshoot lower than 24%, and expecting an output signal as the one in Figure 65. Stability criteria overshoot 24%, a serial resistor must be added to the output, as described in Figure 66. Stability criteria with a serial resistor at V_{CC} = 5 V.

Figure 66. **Stability criteria with a serial resistor at V_{CC} = 5 V**

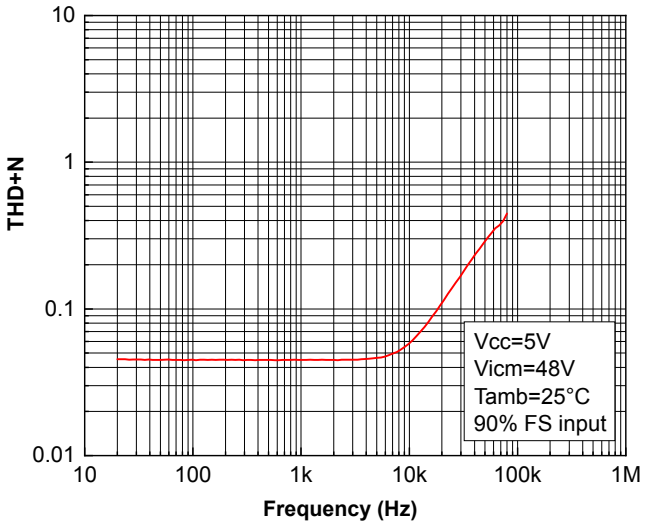


5.10 Low distortion

The TSC2020 demonstrates a low level of distortion especially in low frequency.

Figure 67. THD+N shows an optimum accuracy in the 10 kHz bandwidth. It remains good less than 1% in the bandwidth range of the TSC2020.

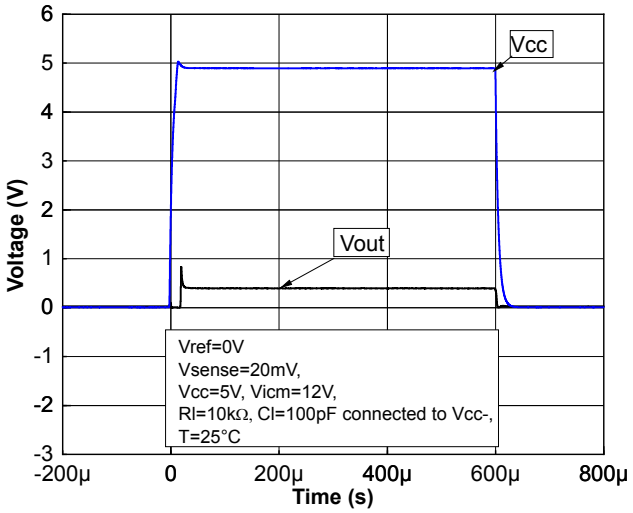
Figure 67. **THD+N**



5.11 Power supply recommendation

In order to correctly decouple the TSC202x, it is recommended to place a 100 nF bypass capacitor between Vcc and Gnd. This capacitor must be placed as close as possible to the supply pins. Figure 68. Startup time with a decoupling capacitance of 100 nF shows a startup time with a decoupling capacitance of 100 nF.

Figure 68. Startup time with a decoupling capacitance of 100 nF



It is also important to take into consideration the V_{ref} pin, which is used to fix the output common mode voltage. Effectively, this pin must be driven by a low impedance voltage source and can be decoupled thanks to a 10 nF bypass capacitor.

A larger bypass capacitor added on the V_{CC} pin and V_{ref} pin should help to enhance CMRR and PSRR performance.

5.12 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the current sensing, load, and power supply. It is good practice to use short and wide PCB traces to minimize voltage drops and parasitic inductance.

When using shunt resistance lower than 1 Ω, it is important to use a 4-wire connection technique to sense the current, as described in the schematic below. Effectively, this technique allows to separate pairs of current-carrying and voltage-sensing electrodes to make more accurate measurements by eliminating the lead and contact resistance from the measurement.

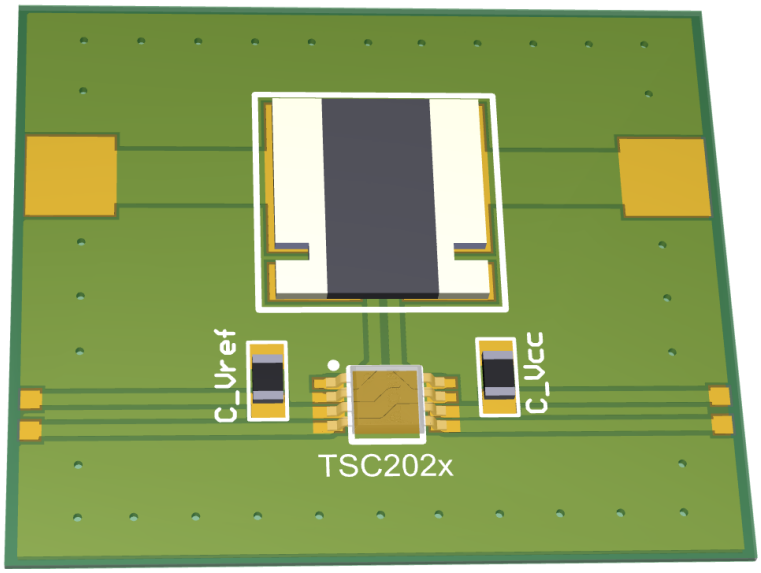
It is also important to treat the track connected to the input pin of the TSC202x as a differential pair; it must have the same length and width, ideally placed on the same PCB plane, and above all must be routed as far as possible from noisy sources. As this track carries the input bias current, in a range of hundreds of µA, it can be designed small but always by taking care of its resistivity. Any vias in these input tracks are not recommended to avoid any parasitic resistance in this path.

To minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used.

A ground plane generally helps to reduce EMI, which is why it is generally recommended to use a multilayer PCB and use the ground planes as a shield to protect the internal track. In this case, pay attention to separate the digital from the analog ground and avoid any ground loop. To minimize EMI impact, it is important to reduce the loop area or antenna.

Figure 69. Recommended layout suggests a possible routing for the TSC202x in order to minimize as much as possible parasitic effect.

Figure 69. Recommended layout

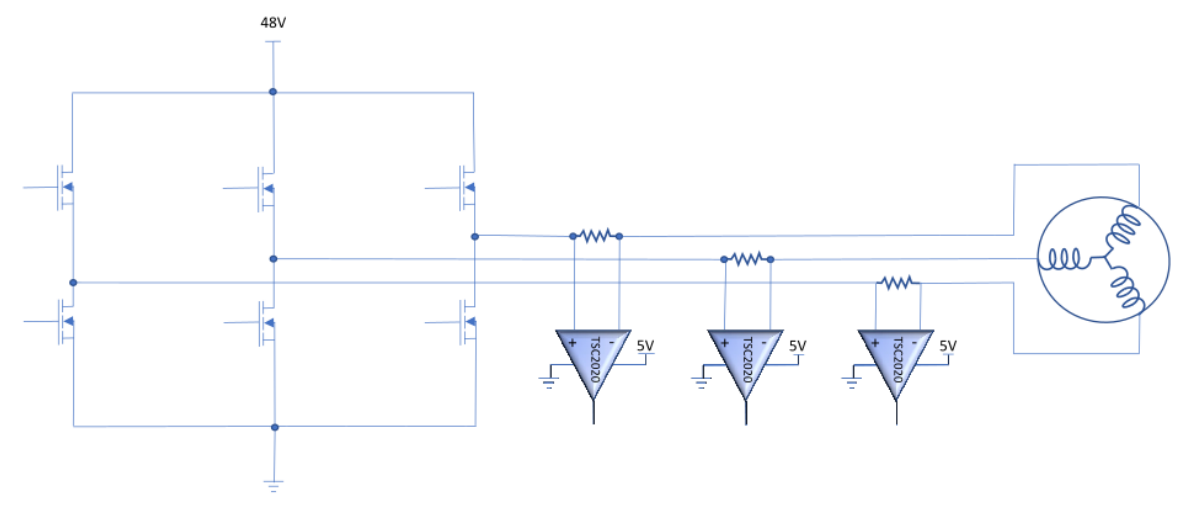


5.13 Application examples

Inline motor control application

The configuration described in Figure 70. Inline motor control application schematic, inline phase current sensing is the best method to precisely know the phase current flowing into the motor. This current measurement offers the best information that can be used in feedback motor control, to optimize the motor performance. The main advantage of this topology is that the current can be read without a strong linkage to the PWM status and without timing limitations in case of very small PWM applied to the phase (low-side current sensing can only be executed while the low-side transistor of that leg is on). It also allows the detection of phase short-circuits.

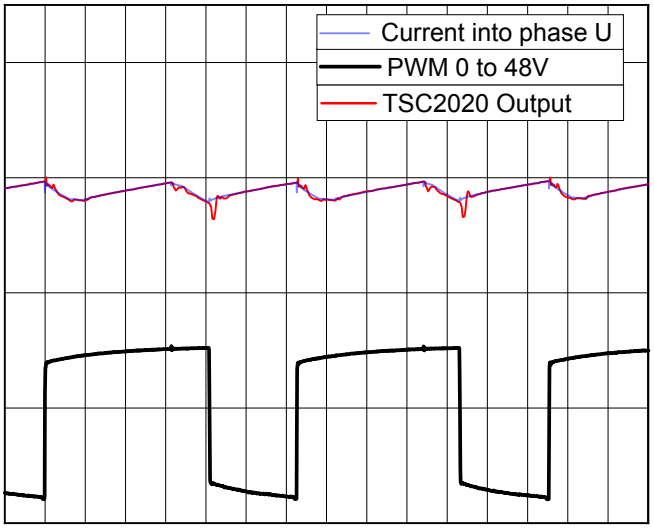
Figure 70. Inline motor control application schematic



As the shunt resistance is placed directly in line with the PWM driver, the input pins of the TSC202x can see in few nanoseconds several tens of volt, depending on the motor to drive. As demonstrated in Figure 71. TSC2020 used in inline topology, the TSC2020 can limit the unwanted disturbance on the output and offer a stable output in few µs after a common mode transient.

The TSC2020 is a bidirectional high-side current sensing especially designed for this kind of application and offers optimized performance.

Figure 71. **TSC2020 used in inline topology**



6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SO8 package information

Figure 72. **SO8 package outline**

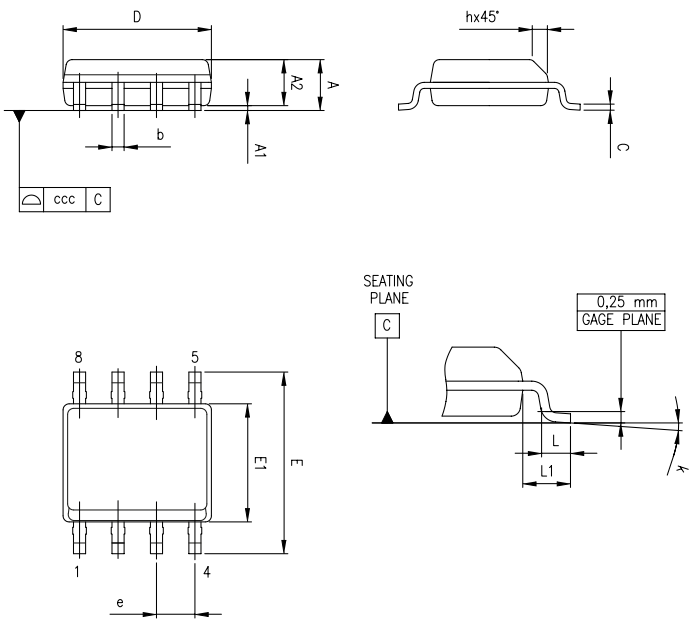
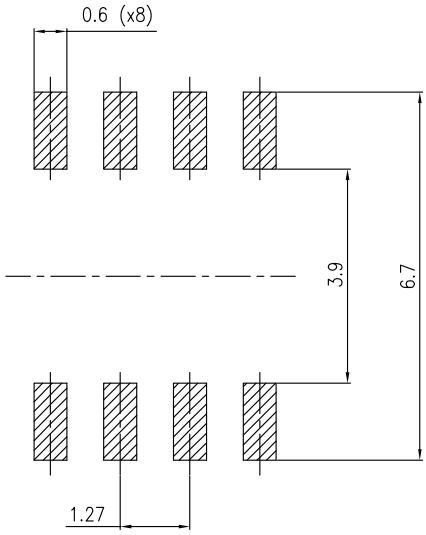


Table 6. **SO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.04		0.010
A2	1.25			0.049		
b	0.28	0.40	0.48	0.011	0.016	0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40	0.635	1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

Figure 73. **SO8 recommended footprint**



6.2 MiniSO8 package information

Figure 74. **MiniSO8 package outline**

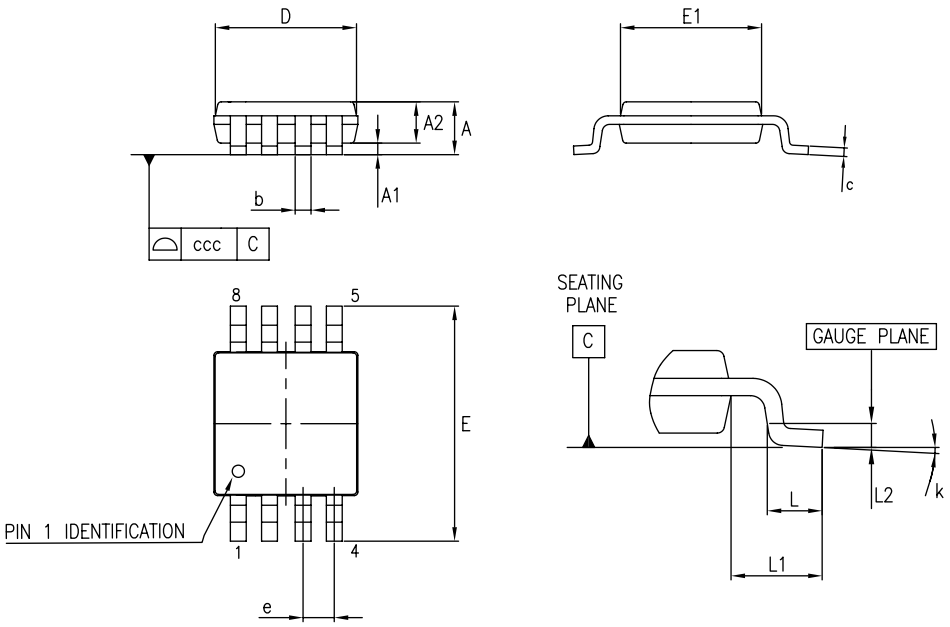
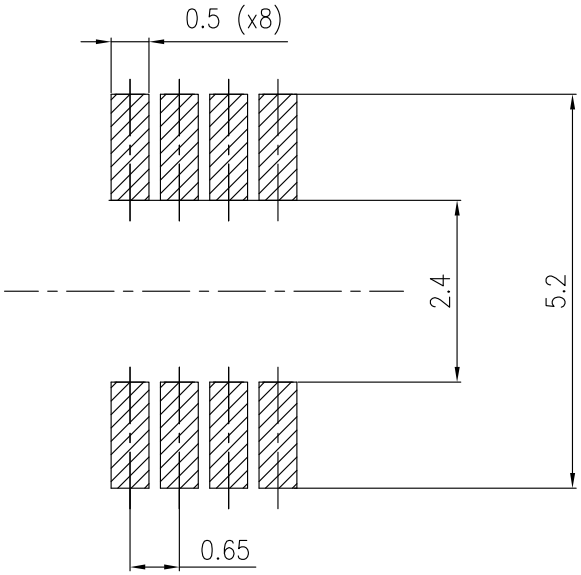


Table 7. **MiniSO8 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

Figure 75. **MiniSO8 recommended footprint**



6.3 TSSOP8 package information

Figure 76. **TSSOP8 package outline**

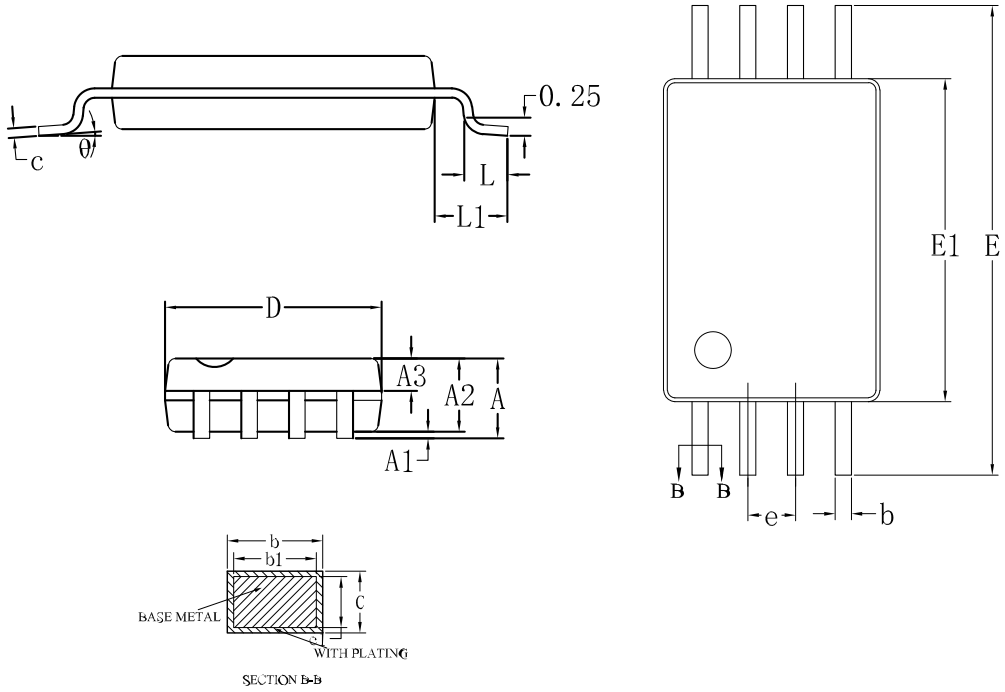
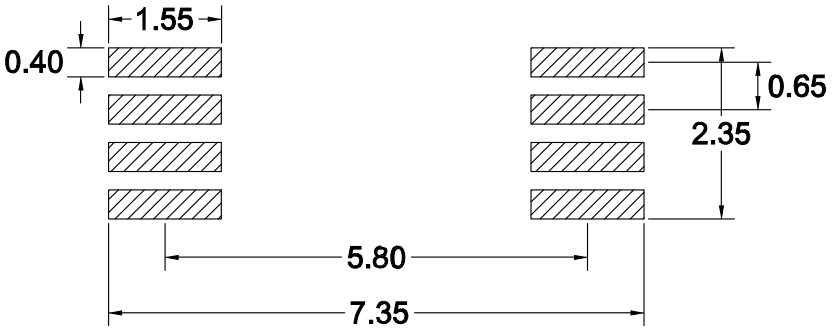


Table 8. **TSSOP8 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.20			0.047
A1	0.05	-	0.15	0.002		0.006
A2	0.90	1.00	1.05	0.035	0.039	0.041
A3	0.39	0.44	0.49	0.015	0.017	0.019
b	0.20	-	0.28	0.008	-	0.011
b1	0.19	0.22	0.25	0.007	0.008	0.010
D2	3.55	3.65	3.75	0.140	0.144	0.148
c	0.13	-	0.17	0.005	-	0.007
c1	0.12	0.13	0.14	0.005	0.005	0.006
D	2.90	3.00	3.10	0.114	0.118	0.122
E1	4.30	4.40	4.50	0.169	0.173	0.177
E	6.20	6.40	6.60	0.244	0.252	0.260
e	0.65 BSC			0.025 BSC		
L	0.45	-	0.75	0.018	-	0.030
L1	1.00 REF			0.039 REF		
θ	0°	-	8°	0°	-	8°

Figure 77. **TSSOP8 recommended footprint**



7 Ordering information

Table 9. Order codes

Order code	Gain (V/V)	Package	Packaging	Marking
TSC2020IDT	20	SO8	Tape & Reel	TSC2020
TSC2020IYDT (1)				TSC2020Y
TSC2020IST		MiniSO8		O129
TSC2020IYST (1)				O132
TSC2020IPT		TSSOP8		O129
TSC2020IYPT (1)				O132
TSC2021IDT	50	SO8		TSC2021
TSC2021IYDT (1)				TSC2021Y
TSC2021IST		MiniSO8		O130
TSC2021IYST (1)				O133
TSC2021IPT		TSSOP8		O130
TSC2021IYPT (1)				O133
TSC2022IDT	100	SO8		TSC2022
TSC2022IYDT (1)				TSC2022Y
TSC2022IST		MiniSO8		O131
TSC2022IYST (1)				O134
TSC2022IPT		TSSOP8		O131
TSC2022IYPT (1)				O134

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
22-Sep-2023	1	Initial release.
20-May-2024	2	Added new TSC2021 and TSC2022 order codes in Table 8.
02-Jul-2024	3	Updated RT condition, Acc parameter in Table 4 and Section 4: Typical characteristics.
11-Oct-2024	4	Added new package TSSOP8, Section 5: Application information and Section 6.3: TSSOP8 package information. Updated Section 1 and Table 9. Order codes.
21-Oct-2024	5	Updated ESD value for TSSOP8 in Table 2. Minor text changes.
21-Nov-2024	6	Updated Eg values in Table 4 and Table 5

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