swissbit®

Product Data Sheet

# Industrial M.2 PCIe SSD

## N-26m2 Series

PCIe 3.1, 3D pSLC

Industrial Temperature Grade

Date: November 27, 2020
Revision: 1.02










Made in Germany

# Contents


1. PRODUCT SUMMARY ..... 3
2. PRODUCT FEATURES ..... 4
3. ORDERING INFORMATION ..... 5
4. PRODUCT DESCRIPTION ..... 6
   - 4.1 Performance Specifications ..... 7
   - 4.2 Current Consumption ..... 7
   - 4.3 Environmental Specifications ..... 7
   - 4.4 Regulatory Compliance ..... 8
   - 4.5 Mechanical Specifications ..... 8
   - 4.6 Reliability and Endurance ..... 8
   - 4.7 Drive Geometry Specification ..... 9
5. ELECTRICAL INTERFACE ..... 10
6. PACKAGE MECHANICAL ..... 12
7. NVME COMMANDS ..... 14
8. IDENTIFY DEVICE INFORMATION ..... 15
9. HEALTH MONITORING FUNCTIONALITY ..... 17
10. PART NUMBER DECODER ..... 20
11. MARKING SPECIFICATION ..... 22
    - 11.1 Top View ..... 22
    - 11.2 Print on the label ..... 22
12. REVISION HISTORY ..... 23

# N-26m2 Series – Industrial M.2 PCIe SSD
# 5 GBytes up to 160 GBytes

## 1. Product Summary

- **Capacities:** 5 GBytes, 10 GBytes, 20 GBytes, 40 GBytes, 80 GBytes, 160 GBytes
- **Form Factor:** PCI Express® M.2 (2230/2242/2280, S4) (30/42/80 mm x 22 mm x 2.63 mm)
- **Compliance[1]:** PCI Express (PCIe) Specification Revision 3.1
- **Interface:** Gen3 x (x2), 4 Lanes
  - Drive operates in x1 mode in x1 M.2 PCIe slots
  - Drive operates in x2 mode in x2 M.2 PCIe slots
  - Drive operates in (x2), x4 mode in x4 M.2 PCIe slots
- **Command Sets:** Supports NVMe 1.3
- **Performance**:
  - Read Performance: Sequential Read up to 1,773 MBytes/s, Random Read 4K up to 140,000 IOPS
  - Write Performance: Sequential Write up to 827 MBytes/s, Random Write 4K up to 131,000 IOPS
- **Host Memory Buffer (HMB):** Support for increased random performance
- **Operating Temperature Range[2]:**
  - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:** -40 °C to 85 °C
- **Operating Voltage:** 3.3, 1.8 and 0.9V supply voltages
- **Low Power Consumption**
- **Power:**
  - Power States PS0, PS1, PS2, PS3 and PS4
  - Thermal Throttling supported
- **Data Retention:** 10 Years @ Life Begin; 1 Year @ Life End, @40°C
- **Endurance in TeraBytes Written (TBW) @ 80GB capacity:**
  - Client ≥ 1550
- **Shock/Vibration:** 1,500 *g* / 50 *g*
- **High-Performance Processor with Integrated, Parallel Flash Interface Engines:**
  - Triple-Level Cell (TLC) 3D NAND Flash in pSLC mode
  - LDPC Code ECC with up to 120 bit correction per 1 KByte page
- **High Reliability:**
  - Mean Time Between Failure (MTBF): > 2,000,000 hours
  - Data Reliability: < 1 non-recoverable error per $10^{16}$ bits read

[1] To check the compatibility of the customer system and the storage device is part of the customer's responsibility. Swissbit can provide guidance and support on request.

[2] Adequate airflow is required to ensure the temperature, as reported in the S.M.A.R.T. data, does not exceed 125°C (industrial temperature drive) and 110°C (commercial temperature drive) respectively.

# 2. Product Features

- Dynamic and Static Wear Leveling
- Subpage Mode Flash Translation Layer (FTL)
- Data Care Management
  - Active: Adaptive Read Refresh
  - Passive: Background Media Scan
- Lifetime Enhancements
  - Dynamic Bad Block Remapping
  - Write Amplification Reduction
- Power Fail Data Loss Protection
- Data set management support (TRIM)
- Active State Power Management (ASPM) Support
- In-Field Firmware Update[3]
- Enterprise-Grade Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
- 30 µinch Gold-Plated Connector (IPC-6012B Class 2 Compliant)
- End-to-End (E2E) Data Protection
- AES256 Encryption (on request)
- Life Cycle Management
- Controlled "Locked" BOM
- RoHS / REACH Compliant
- Swissbit Life Time Monitoring (SBLTM) Tool and SDK for SBLTM (on request)




[3] The support of In-Field FW update capabilities on host systems is recommended.

# 3. Ordering Information

**Table 1: Standard Product List**

| Capacity | Part Number | Number of Lanes |
|---|---|---|
| 5 GBytes | SFPC005GMxEC1T0-I-5E-yzP-STD | 4 |
| 10 GBytes | SFPC010GMxEC1T0-I-5E-yzP-STD | |
| 20 GBytes | SFPC020GMxEC2T0-I-5E-yzP-STD | |
| 40 GBytes | SFPC040GMxEC4T0-I-5E-yzP-STD | |
| 80 GBytes | SFPC080GMxEC4T0-I-6F-yzP-STD | |
| 160 GBytes | SFPC160GMxEC4WD-I-6F-yzP-STD | |
| 160 GBytes | SFPC160GMxEB4WD-I-6F-yzP-STD | 2 |

x = product generation; y = form type; z= firmware revision

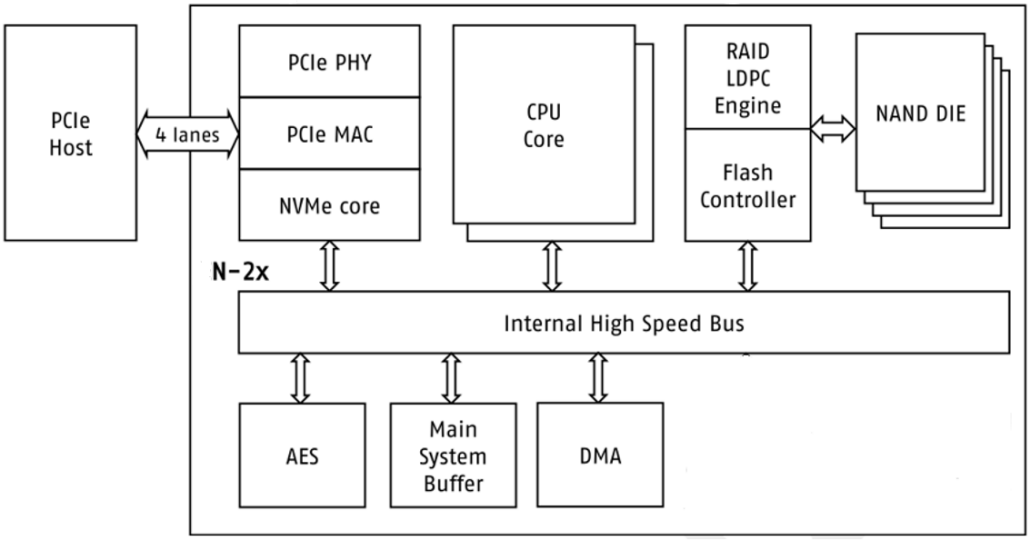
**Table 2: Available Part Numbers**

| Capacity | Part Number – Industrial Temperature | | | |
|---|---|---|---|---|
| | 2230 | 2242 | 2280 | Number of Lanes |
| 5 GBytes | SFPC005GM1EC1T0-I-5E-A1P-STD | SFPC005GM1EC1T0-I-5E-11P-STD | SFPC005GM1EC1T0-I-5E-51P-STD | 4 |
| 10 GBytes | SFPC010GM1EC1T0-I-5E-A1P-STD | SFPC010GM1EC1T0-I-5E-11P-STD | SFPC010GM1EC1T0-I-5E-51P-STD | |
| 20 GBytes | SFPC020GM1EC2T0-I-5E-A1P-STD | SFPC020GM1EC2T0-I-5E-11P-STD | SFPC020GM1EC2T0-I-5E-51P-STD | |
| 40 GBytes | SFPC040GM1EC4T0-I-5E-A1P-STD | SFPC040GM1EC4T0-I-5E-11P-STD | SFPC040GM1EC4T0-I-5E-51P-STD | |
| 80 GBytes | SFPC080GM1EC4T0-I-6F-A1P-STD | SFPC080GM1EC4T0-I-6F-11P-STD | SFPC080GM1EC4T0-I-6F-51P-STD | |
| 160 GBytes | SFPC160GM2EC4WD-I-6F-A1P-STD | SFPC160GM2EC4WD-I-6F-11P-STD | SFPC160GM2EC4WD-I-6F-51P-STD | |
| 160 GBytes | SFPC160GM1EB4WD-I-6F-A1P-STD | SFPC160GM1EB4WD-I-6F-11P-STD | SFPC160GM1EB4WD-I-6F-51P-STD | 2 |

# 4. Product Description

The Swissbit® N-26m2 Solid State Drive (SSD) leverages the M.2 standard and NVMe standard to support a PCIe electrical interface as well as AES encryption, E2E data protection and TCG Opal standards. The NVMe controller and the newest 3D NAND flash technology provides robust, non-volatile storage solution for today's embedded computing applications. A functional block diagram of the N-26m2 SSD is provided below in Figure 1.

**Figure 1: N-26m2 Functional Block Diagram**




The N-26m2 SSD incorporates a 75-position edge connector with M key to support host read/write, control, and power activity per the applicable JEDEC specification.

The on-board NVMe controller manages the interface between the host and the non-volatile NAND flash memory array. The controller is designed to support PCIe interface speeds and utilizes a dual processing core, providing an optimum balance between read/write performance, Data Care Management, and power fail protection.

Swissbit's N-26m2 SSDs deliver an impressive IOPS rate and highest endurance by combining Bit Cost Scalable (BiCS) 3D flash technology with a high-end controller architecture, firmware, and an optimized configuration. The SSDs are designed for applications requiring high data transfer rates (see Table 3: Read/Write Performance). This performance is achieved through HMB support, a 4-channel flash controller and 4-lane PCIe interface.

An on-controller Error Correction Code (ECC) engine provides the N-26m2 hardware ECC, which is capable of correcting up to 120 bits per 1 KByte page. This engine, combined with Swissbit's Data Care Management firmware, provides both passive and active data management strategies to ensure data integrity and extract the maximum possible endurance and reliability from the NAND flash array. These strategies include, but are not limited to, Global Wear Leveling, Adaptive Read Refresh, and Dynamic Block Remapping.

### Related Documentation

- NVM Express – Revision 1.3, (https://nvmexpress.org/)
- PCI Express M.2 standard – PCI Express M.2 Specification, Revision 3.0, June 26, 2019 (https://pcisig.com)

## 4.1 Performance Specifications

The N-26m2 read/write sequential and random CDM performance benchmarks are detailed in the following Table 3.

**Table 3: Read/Write Performance[4]**

| Capacity | Sequential Read (MBPS) | | Sequential Write (MBPS) | | Random Read 4K (IOPS) | | Random Write 4K (IOPS) | |
|---|---|---|---|---|---|---|---|---|
| | HMB on | HMB off | HMB on | HMB off | HMB on | HMB off | HMB on | HMB off |
| 5 GBytes | 297 | 293 | 102 | 63 | 21,000 | 16,000 | 20,000 | 8,000 |
| 10 GBytes | 297 | 293 | 103 | 63 | 21,000 | 16,000 | 20,000 | 14,000 |
| 20 GBytes | 594 | 584 | 208 | 156 | 41,000 | 30,000 | 42,000 | 36,000 |
| 40 GBytes | 1,184 | 1,145 | 385 | 205 | 80,000 | 41,400 | 69,000 | 45,000 |
| 80 GBytes | 1,773 | 1,600 | 718 | 365 | 140,000 | 67,000 | 100,000 | 76,000 |
| 160 GBytes[5] 2-Lane | 1,613 | 1,601 | 827 | 583 | 110,000 | 77,000 | 131,000 | 113,500 |
| 160 GBytes[5] 4-Lane | 1,613 | 1,601 | 827 | 583 | 110,000 | 77,000 | 131,000 | 113,500 |

## 4.2 Current Consumption

The drive-level current consumption as a function of operating mode is shown in the following Table 4.

**Table 4: Current Consumption Typical[6]**

| Capacity | Sequential Read | Sequential Write | Idle | PS3 | PS4 | Unit |
|---|---|---|---|---|---|---|
| 5 GBytes | 440 | 420 | 148<br>55[7] | 18 | 15 | mA |
| 10 GBytes | 440 | 420 | | | | |
| 20 GBytes | 520 | 470 | | | | |
| 40 GBytes | 670 | 540 | | | | |
| 80 GBytes | 810 | 680 | | | | |
| 160 GBytes[5] 2-Lane | 790 | 740 | 120<br>55[7] | 19 | 15 | |
| 160 GBytes[5] 4-Lane | 790 | 740 | 120<br>55[7] | 19 | 15 | |

## 4.3 Environmental Specifications

### 4.3.1 Recommended Operating Conditions

The recommended operating conditions for the N-26m2 SSD are provided in the following Table 5.

**Table 5: Recommended Operating Conditions[8]**

| Parameter | Value |
|---|---|
| Industrial Operating Temperature | -40 °C to 85 °C |
| Power Supply $V_{CC}$ Voltage | 3.3 V ± 5% |

### 4.3.2 Recommended Storage Conditions

The recommended storage conditions are listed in the following Table 6.

[4] The values are measured using Crystal Disk Mark. Performance depends on flash type and number, file/cluster size, and burst speed.
[5] Target values
[6] All values are typical total values recorded at 25 °C
[7] With active ASPM (active state power management)
[8] Adequate airflow is required to ensure the temperature, as reported in the S.M.A.R.T. data, does not exceed 125°C (industrial temperature drive) and 110°C (commercial temperature drive) respectively.

Table 6: Recommended Storage Conditions[9]

| Parameter | Value |
|---|---|
| Industrial Storage Temperature | -40 °C to 85 °C |

### 4.3.3 Shock, Vibration and Humidity

The maximum shock, vibration and humidity conditions are listed in the following Table 7.

Table 7: Shock, Vibration and Humidity

| Parameter | Value |
|---|---|
| Non-Operating Shock | 1,500 *g*, 0.5 ms pulse duration, half-sine wave (IEC 60068-2-27 and JESD22-B110 cond. B) |
| Non-Operating Vibration | 50 *g*, 80-2,000 Hz, 3 axes, 12 cycles (IEC 60068-2-6, MIL-STD-883 H Method 2007.3) |
| Humidity (Non-Condensing) | 85% RH 85 °C, 1000 hrs, max. supply voltage (JESD22-A101B) |

## *4.4 Regulatory Compliance*

The N-26m2 devices comply with the directives and standards listed in the following Table 8.

Table 8: Regulatory Compliance

| Abbreviation | Regulation/ Standard |
|---|---|
| EMC | (EU) 2014/30<br>(FCC) 47 CFR Part 15 |
| RoHS | (EU) 2011/65/EU with 2015/863 and 2017/2102 |
| REACh | (EU) 1907/2006 and 207/2011 |
| WEEE | (EU) 2012/19 |

## *4.5 Mechanical Specifications*

The N-26m2 SSD consists of a flash controller and NAND flash memory devices. The controller interfaces with a host system, allowing data to be written to and read from the flash memory array. Physical dimensions are detailed in the following Table 9. Figure 3 on page 12 illustrates the N-26m2 dimensions.

Table 9: Physical Dimensions

| Physical Dimensions | | Unit |
|---|---|---|
| Length | 30.00/42.00/80.00±0.15 | mm |
| Width | 22.00±0.15 | |
| Thickness (Max) | Max. 2.63 | |
| Weight (Max Capacity, 2280) | ≤5.50 | g |

## *4.6 Reliability and Endurance*

The Mean Time Between Failure (MTBF) is specified to exceed the value listed in the following Table 10. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

Table 10: Reliability

| Parameter | Value |
|---|---|
| MTBF (at 25 °C) | > 2,000,000 hours |
| Data Reliability | < 1 Non-Recoverable Error per $10^{16}$ Bits Read |
| Data Retention (up to 40°C)[10] | 10 Years at Start (JESD47), 1 Year at EOL |

[9] The retention at high temperature is reduced. The acceleration factor at 100°C compared with 40 or 55°C is very high, i.e. the initial retention from 10 years@55°C is reduced to 33 days@100°C based on NAND process node.

[10] NAND Flash data retention and endurance characteristics are defined according to JEDEC JESD47 and JESD22. The endurance limits of the storage shall be monitored by the life time information and simulated before field usage by the customer.

Endurance represented as both TeraBytes Written (TBW) and full Drive Writes Per Day (DWPD) for different application scenarios is provided in the following Table 11.

**Table 11: Endurance[11, 12]**

| Capacity | Sequential | | Client[13] | | Enterprise | |
|---|---|---|---|---|---|---|
| | TBW | DWPD[14] | TBW | DWPD[14] | TBW | DWPD[14] |
| 5 GBytes | 179 | 32.7 | 90 | 17.7 | 16.9 | 3.09 |
| 10 GBytes | 353 | 32.2 | 185 | 17.7 | 27.5 | 2.51 |
| 20 GBytes | 717 | 32.7 | 375 | 17.7 | 57.7 | 2.63 |
| 40 GBytes | 1415 | 32.3 | 750 | 17.7 | 118.9 | 2.71 |
| 80 GBytes | 2,900 | 33.1 | 1,550 | 17.7 | 234.8 | 2.68 |
| 160 GBytes[15] | tbd | tbd | tbd | tbd | 804.6 | 4.59 |

## *4.7 Drive Geometry Specification*

The N-26m2 drive geometry is set to report industry standard LBA settings per the IDEMA standard (LBA1-03). The values for each capacity are shown in the following Table 12.

**Table 12: Drive Geometry**

| Raw Capacity | User Capacity[16] | Total LBA | User Addressable Bytes |
|---|---|---|---|
| | | Decimal | (Unformatted) |
| 16 GBytes | 5 GBytes | 9,788,688 | 5,011,808,256 |
| 32 GBytes | 10 GBytes | 19,556,208 | 10,012,778,496 |
| 64 GBytes | 20 GBytes | 39,091,248 | 20,014,718,976 |
| 128 GBytes | 40 GBytes | 78,161,328 | 40,018,599,936 |
| 256 GBytes | 80 GBytes | 156,301,488 | 80,026,361,856 |
| 512 GBytes | 160 GBytes | 312,581,808 | 160,041,885,696 |

[11] Client and Enterprise workloads follow the JEDEC JESD219 standard. Enterprise workload values are measured based on 168 hours of runtime. 1 TByte = $10^{12}$ bytes

[12] According to JEDEC (JESD47I), the time to write the full TBW is a minimum of 18 months. Higher average daily data volume or frequent writing below 0°C reduces the specified TBW. The values listed are estimates and are subject to change without notice

[13] Because the JEDEC master trace file for the Client workload is designed for capacities ≥ 60 GBytes, the TBW and DWPD values for the capacities below 60 GBytes are estimates

[14] DWPD values are based on a service life of 3 years. DWPD values with consideration of the limited lifetime warranty period of the storage device according to the used flash type and device capacity. Customer workload with higher DWPD values contributes to an earlier EOL of the storage device.

[15] Target values

[16] 1 GByte = $10^9$ bytes

# 5. Electrical Interface

This 75-position m.2 connector (Figure 2) incorporates M key for Socket 2/Socket 3 PCIe-based SSDs and follows the applicable PCIe m.2 specification. The signal/pin assignments and descriptions are listed in the following Table 13.

**Figure 2: N-26m2 Electrical Interface**

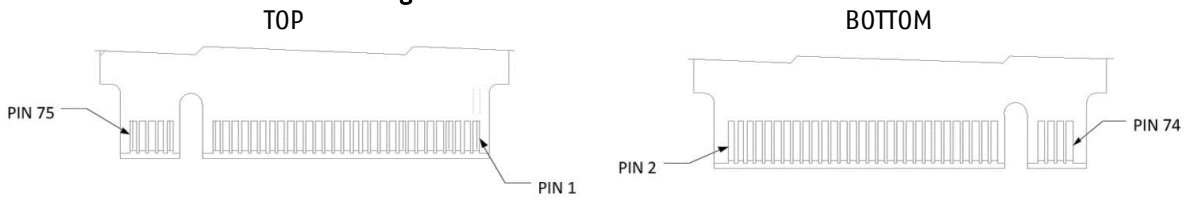



**Table 13: Pin Assignment, Name and Description**

| Description | Assignment | Pin | Pin | Assignment | Description |
|---|---|---|---|---|---|
| Config_3 | GND | 1 | 2 | +3.3V | 3.3V Source |
| Ground | GND | 3 | 4 | +3.3V | 3.3V Source |
| PCIe TX Differential Signal | PETn3* | 5 | 6 | NC | No Connect |
| PCIe TX Differential Signal | PETp3* | 7 | 8 | NC | No Connect |
| Ground | GND | 9 | 10 | DAS/DSS | DEVACT Device Activity Signal |
| PCIe RX Differential Signal | PERn3* | 11 | 12 | +3.3V | 3.3V Source |
| PCIe RX Differential Signal | PERp3* | 13 | 14 | +3.3V | 3.3V Source |
| Ground | GND | 15 | 16 | +3.3V | 3.3V Source |
| PCIe TX Differential Signal | PETn2* | 17 | 18 | +3.3V | 3.3V Source |
| PCIe TX Differential Signal | PETp2* | 19 | 20 | NC | No Connect[17] |
| Ground | GND | 21 | 22 | NC | No Connect |
| PCIe RX Differential Signal | PERn2* | 23 | 24 | NC | No Connect |
| PCIe RX Differential Signal | PERp2* | 25 | 26 | NC | No Connect |
| Ground | GND | 27 | 28 | NC | No Connect |
| PCIe TX Differential Signal | PETn1* | 29 | 30 | NC | No Connect |
| PCIe TX Differential Signal | PETp1* | 31 | 32 | NC | No Connect |
| Ground | GND | 33 | 34 | NC | No Connect |
| PCIe RX Differential Signal | PERn1* | 35 | 36 | NC | No Connect |
| PCIe RX Differential Signal | PERp1* | 37 | 38 | NC | No Connect |
| Ground | GND | 39 | 40 | NC | No Connect |
| PCIe TX Differential Signal | PETn0* | 41 | 42 | NC | No Connect |
| PCIe TX Differential Signal | PETp0* | 43 | 44 | NC | No Connect |
| Ground | GND | 45 | 46 | NC | No Connect |
| PCIe RX Differential Signal | PERn0* | 47 | 48 | NC | No Connect |
| PCIe RX Differential Signal | PERp0* | 49 | 50 | PERST# | PE-Reset (Functional Reset) |
| Ground | GND | 51 | 52 | CLKREQ# | Clock Request Signal; L1 PM |
| PCIe Reference Clock Signal | REFCLKn | 53 | 54 | PEWAKE# | PCIe PME Wake |
| PCIe Reference Clock Signal | REFCLKp | 55 | 56 | DNU | Reserved (do not use) |
| Ground | GND | 57 | 58 | DNU | Reserved (do not use) |

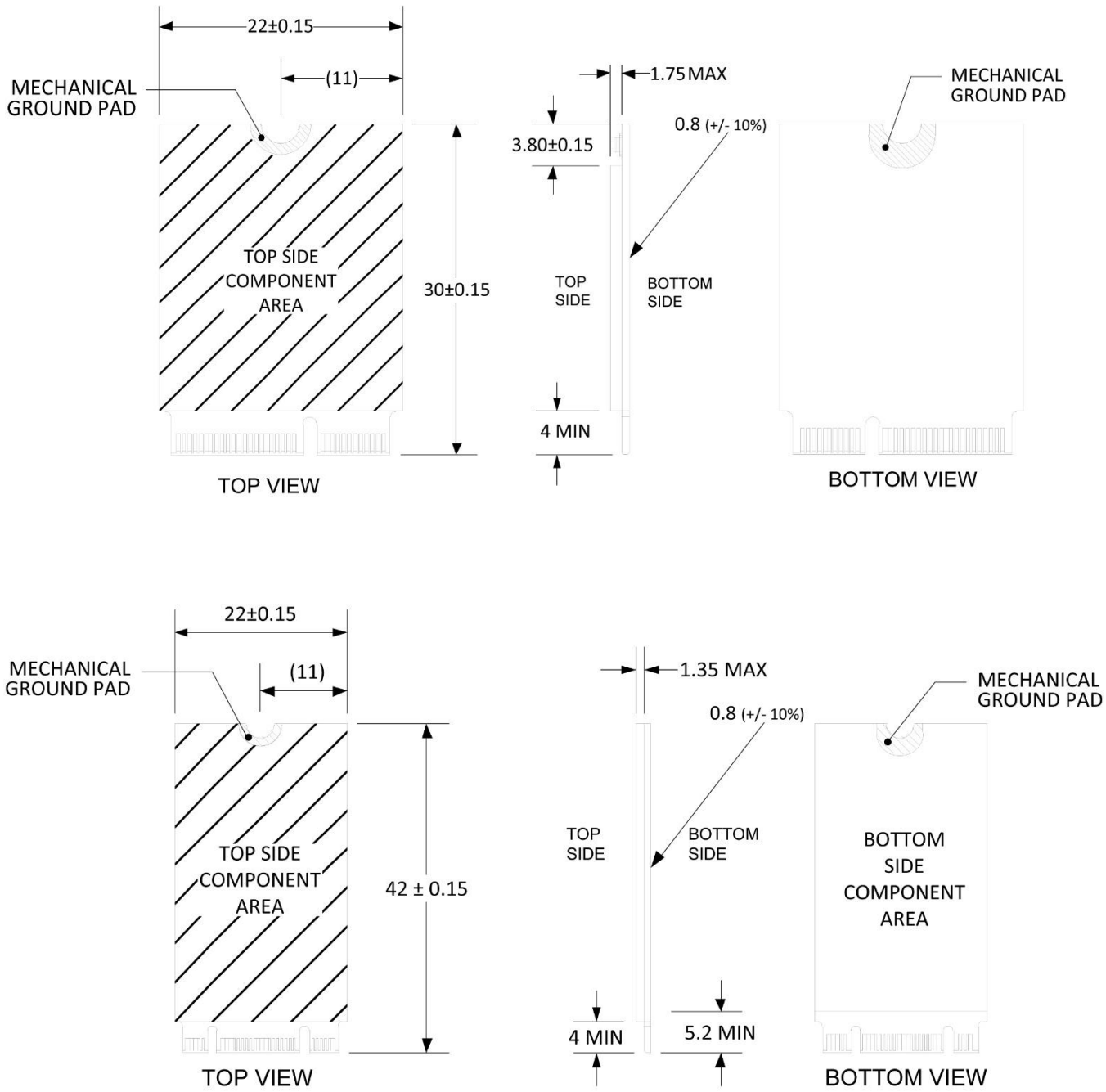
[17] The write protect option is available on this pin upon request

| | | | | | |
|---|---|---|---|---|---|
| Mechanical Notch M | - | 59-65 | 60-66 | - | Mechanical Notch M |
| RESET# | NC | 67 | 68 | NC | 32.768 kHz Clock Supply |
| Config_1 | NC | 69 | 70 | 3.3V | Supply Pin, 3.3V |
| Ground | GND | 71 | 72 | 3.3V | Supply Pin, 3.3V |
| Ground | GND | 73 | 74 | 3.3V | Supply Pin, 3.3V |
| Config_2 | GND | 75 | | | |

*TX (transmit) and RX (receive) pins are labeled from the SSD view and must be connected with the reversed RX and TX signals of the host (i.e., TX to RX and RX to TX).

# 6. Package Mechanical

**Figure 3: N-26m2 dimensions in mm**



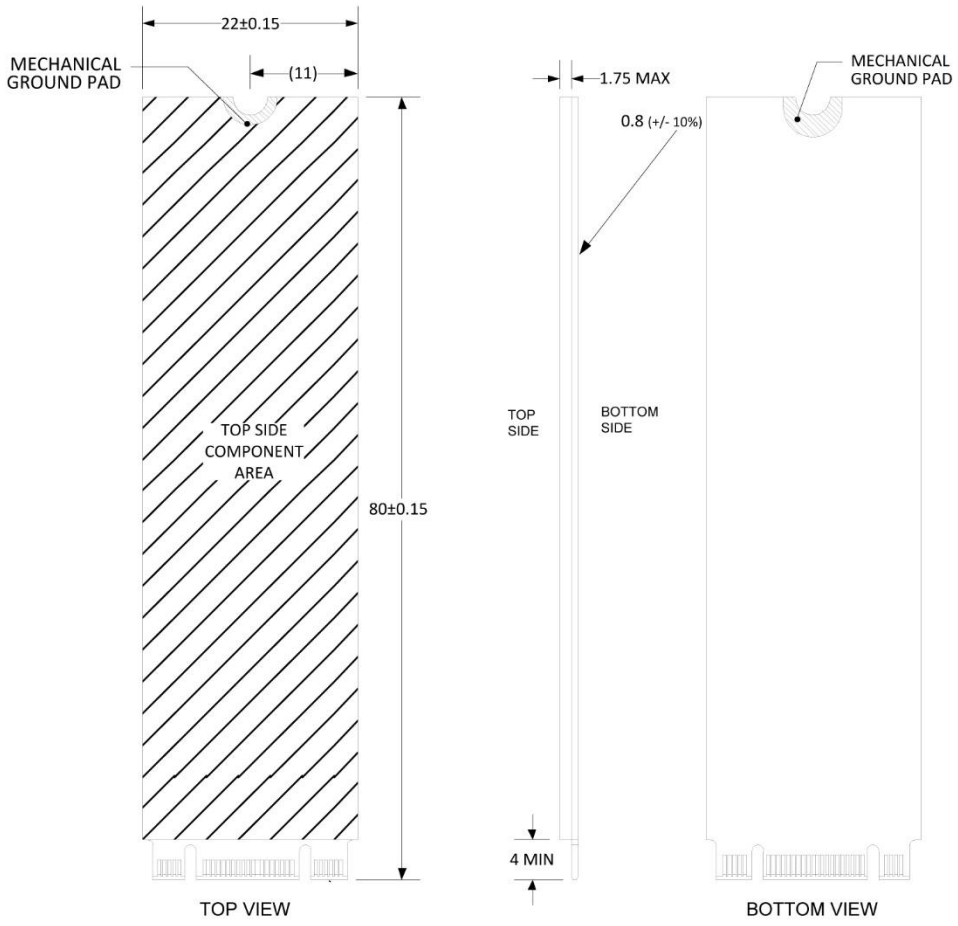
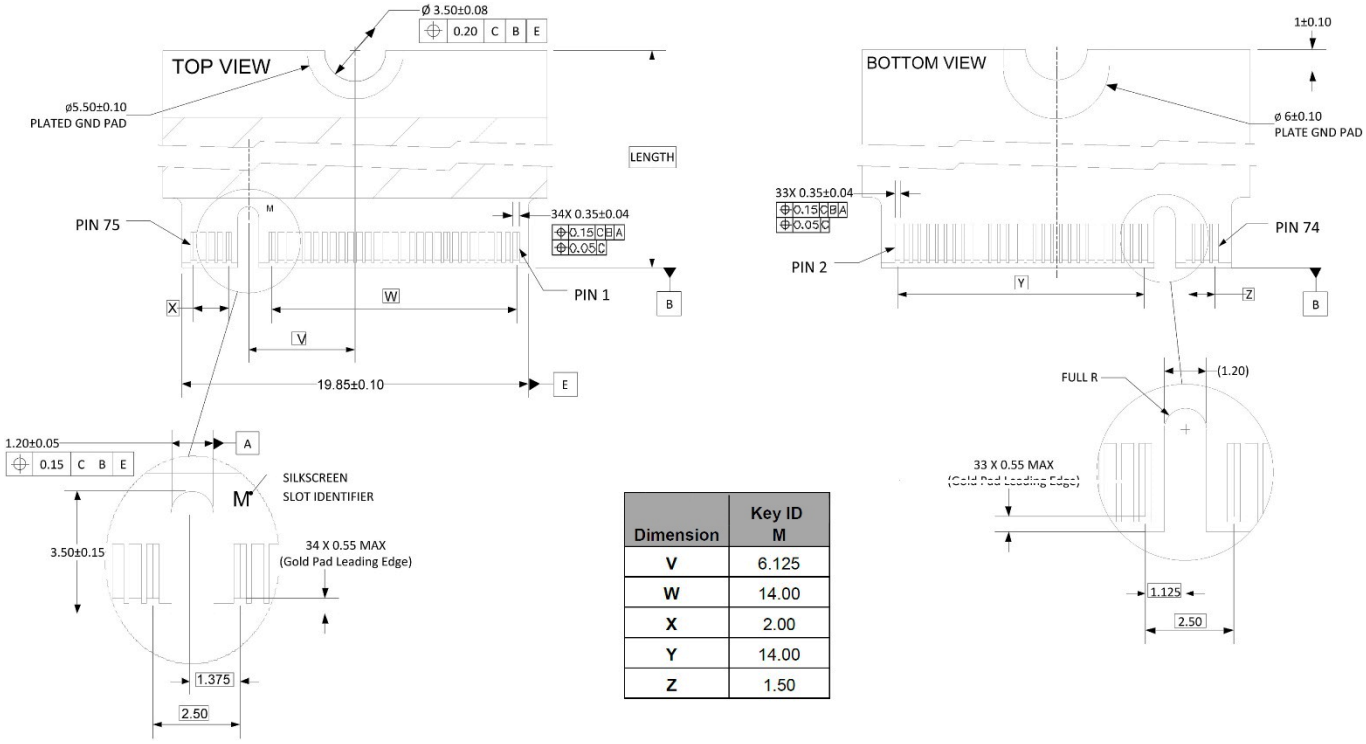



**Figure 4: M.2 Connector Dimensions in mm**




| Dimension | Key ID M |
|---|---|
| V | 6.125 |
| W | 14.00 |
| X | 2.00 |
| Y | 14.00 |
| Z | 1.50 |

# 7. NVMe Commands

This section provides information on the NVMe commands supported by the SSD. The commands are issued by loading the DWords in the command block with the supplied parameter, and then writing the command code to the register. See the following Table 14 for a list of NVMe commands the device supports. For details about setting up the command registers, see the latest NVMe Specification.

**Table 14: NVMe Command Set**

| Command | Code | Command | Code |
|---|---|---|---|
| **Admin Commands** | | | |
| Delete I/O Submission Queue | 00h | Create I/O Submission Queue | 01h |
| Get Log Page | 02h | Delete I/O Completion Queue | 04h |
| Create I/O Completion Queue | 05h | Identify | 06h |
| Abort | 08h | Set Features | 09h |
| Get Features | 0Ah | Asynchronous Event Request | 0Ch |
| Firmware Commit | 10h | Firmware Image Download | 11h |
| Device Self-test | 14h | Format NVM | 80h |
| Sanitize | 84h | | |
| **NVM Command Set** | | | |
| Flush | 00h | Write | 01h |
| Read | 02h | Write Uncorrectable | 04h |
| Compare | 05h | Write Zeroes | 08h |
| Dataset Management | 09h | | |
| **Command** | **Code** | **Command** | **Code** |
| **Admin Commands** | | | |
| Delete I/O Submission Queue | 00h | Create I/O Submission Queue | 01h |
| Get Log Page | 02h | Delete I/O Completion Queue | 04h |
| Create I/O Completion Queue | 05h | Identify | 06h |
| Abort | 08h | Set Features | 09h |
| Get Features | 0Ah | Asynchronous Event Request | 0Ch |
| Firmware Commit | 10h | Firmware Image Download | 11h |
| Device Self-test | 14h | Format NVM | 80h |
| Sanitize | 84h | | |
| **NVM Command Set** | | | |
| Flush | 00h | Write | 01h |
| Read | 02h | Write Uncorrectable | 04h |
| Compare | 05h | Write Zeroes | 08h |
| Dataset Management | 09h | | |

# 8. Identify Device Information

The following table describes the 4096 bytes of data the drive returns for the Identify command (06h).

**Table 15: Identify Namespace Data Structure (CNS 00h)**

| Byte(s) | Default Value | Data Field Type Information |
|---|---|---|
| 0-7 | XXXXh[18] | Namespace Size (NSZE) |
| 8-15 | XXXXh[18] | Namespace Capacity (NCAP) |
| 16-23 | XXXXh[18] | Namespace Utilization (NUSE) |
| 24 | 00h | Namespace Features (NSFEAT) |
| 25 | 00h | Number of LBA Formats (NLBAF) |
| 26 | 00h | Formatted LBA Size (FLBAS) |
| 27 | 00h | Metadata Capabilities (MC) |
| 28 | 00h | End-to -end Data Protection Capabilities (DPC |
| 29 | 00h | End-to -end Data Protection Type Settings (DPS) |
| 30 | 00h | Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC) |
| 31 | 00h | Reservation Capabilities (RESCAP) |
| 32 | 00h | Format Progress Indicator (FPI) |
| 33 | 00h | Deallocate Logical Block Features (DLFEAT) |
| 34-35 | 0000h | Namespace Atomic Write Unit Normal (NAWUN) |
| 36-37 | 0000h | Namespace Atomic Write Unit Power Fail (NAWUPF) |
| 38-39 | 0000h | Namespace Atomic Compare & Write Unit (NACWU) |
| 40-41 | 0000h | Namespace Atomic Boundary Size Normal (NABSN) |
| 42-43 | 0000h | Namespace Atomic Boundary Offset (NABO) |
| 44-45 | 0000h | Namespace Atomic Boundary Size Power Fail (NABSPF) |
| 46-47 | 0000h | Namespace Optimal IO Boundary (NOIOB) |
| 48-63 | All 00h | NVM Capacity (NVMCAP) |
| 64-103 | All 00h | Reserved |
| 104-119 | All 00h | Namespace Globally Unique Identifier (NGUID) |
| 120-127 | All 00h | IEEE Extended Unique Identifier (EUI64) |
| 128-131 | 00090000h | LBA Format 0 Support (LBAF0) |
| 132-191 | All 00h | LBA Format 1 to 15 Support (LBAF1 – LBAF15) |
| 192-383 | All 00h | Reserved |
| 384-4095 | All 00h | Vendor Specific (VS) |

**Table 16: Identify Controller Data Structure (CNS 01h)**

| Byte(s) | Default Value | Data Field Type Information |
|---|---|---|
| 0-1 | 1DD4h | PCI Vendor ID (VID) |
| 2-3 | 1DD4h | PCI Subsystem Vendor ID (SSVID) |
| 4-23 | XXXXh[18] | Serial Number (SN) |
| 24-63 | XXXXh[18] | Model Number (MN) |
| 64-71 | XXXXh[18] | Firmware Version (FR) |
| 72 | 06h | Recommended Arbitration Burst (RAB) |
| 73-75 | 8C6078h | IEEE OUI Identifier (IEEE) |

[18] Values depend on device configuration.

| Byte(s) | Default Value | Data Field Type Information |
|---|---|---|
| 76 | 00h | Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC) |
| 77 | 06h | Maximum Data Transfer Size (MDTS) |
| 78-79 | 0001h | Controller ID (CNTLID) |
| 80-83 | 00010300h | Version (VER) |
| 84-87 | 000249F0h | Runtime D3 Resume Latency (RTD3R) |
| 88-91 | 00013880h | Runtime D3 Entry Latency (RTD3E) |
| 92-95 | 00000200h | Optional Asynchronous Events Supported (OAES) |
| 96-99 | 00000000h | Controller Attributes (CTRATT) |
| 100-111 | All 00h | Reserved |
| 112-127 | All 00h | FRU Globally Unique Identifier (FGUID) |
| 128-255 | All 00h | Reserved |
| 256-257 | 0016h | Optional Admin Command Support (OACS) |
| 258 | 04h | Abort Command Limit (ACL) |
| 259 | 07h | Asynchronous Event Request Limit (AERL) |
| 260 | 12h | Firmware Updates (FRMW) |
| 261 | 0Eh | Log Page Attributes (LPA) |
| 262 | 3Fh | Error Log Page Entries (ELPE) |
| 263 | 04h | Number of Power States Supported (NPSS) |
| 264 | 01h | Admin Vendor-Specific Command Configuration (AVSCC) |
| 265 | 01h | Autonomous Power State Transition Attributes (APSTA) |
| 266-267 | 0170h | Warning Composite Temperature Threshold in Degrees Kelvin (WCTEMP) |
| 268-269 | 017Fh | Critical Composite Temperature Threshold in Degrees Kelvin (CCTEMP) |
| 270-271 | 0064h | Maximum Time for Firmware Activation (MTFA) |
| 272-275 | 00004000h | Host Memory Buffer Preferred Size (HMPRE) |
| 276-279 | 00004000h | Host Memory Buffer Minimum Size (HMMIN) |
| 280-295 | All 00h | Total NVM Capacity (TNVMCAP) |
| 296-311 | All 00h | Unallocated NVM Capacity (UNVMCAP) |
| 312-315 | 00000000h | Replay Protected Memory Block Support (RPMBS) |
| 316-317 | 000Ah | Extended Device Self-test Time (EDSTT) |
| 318 | 01h | Device Self-test Options (DSTO) |
| 319 | 04h | Firmware Update Granularity (FWUG) |
| 320-321 | 0000h | Keep Alive Support (KAS) |
| 322-323 | 0001h | Host Controlled Thermal Management Attributes (HCTMA) |
| 324-325 | 0157h | Minimum Thermal Management Temperature (MNTMT) |
| 326-327 | 017Fh | Maximum Thermal Management Temperature (MXTMT) |
| 328-331 | 00000002h | Sanitize Capabilities (SANICAP) |
| 332-511 | All 00h | Reserved |
| 512 | 66h | Submission Queue Entry Size (SQES) |
| 513 | 44h | Completion Queue Entry Size (CQES) |
| 514-515 | 0000h | Maximum Outstanding Commands (MAXCMD) |
| 516-519 | 000000001h | Number of Namespaces (NN) |
| 520-521 | 001Fh | Optional NVM Command Support (ONCS) |
| 522-523 | 0000h | Fused Operation Support (FUSES) |

| Byte(s) | Default Value | Data Field Type Information |
|---|---|---|
| 524 | 00h | Format NVM Attributes (FNA) |
| 525 | 01h | Volatile Write Cache (VWC) |
| 526-527 | 0000h | Atomic Write Unit Normal (AWUN) |
| 528-529 | 0000h | Atomic Write Unit Power Fail (AWUPF) |
| 530 | 00h | NVM Vendor-Specific Command Configuration (NVSCC) |
| 531 | 00h | Reserved |
| 532-533 | 0000h | Atomic Compare and Write Unit (ACWU) |
| 534-535 | 0000h | Reserved |
| 536-539 | 00000000h | Scatter Gather List Support (SGLC) |
| 540-767 | All 00h | Reserved |
| 768-1023 | All 00h | NVM Subsystem NVMe Qualified Name (SUBNQN) |
| 1024-2047 | All 00h | Reserved |
| 2048-2079 | XXXXh | Power State 0 Descriptor |
| 2080-2111 | XXXXh | Power State 1 Descriptor |
| 2112-2143 | XXXXh | Power State 2 Descriptor |
| 2144-2175 | XXXXh | Power State 3 Descriptor |
| 2176-2207 | XXXXh | Power State 4 Descriptor |
| 2208-3071 | All 00h | Power State 5 - 31 Descriptor (Not Applicable) |
| 3072-4095 | All 00h | Vendor Specific (VS) |

# 9. Health Monitoring Functionality

The N-26m2 SSDs support Self-Monitoring, Analysis, and Reporting Technology (SMART) attributes. The SSD supports log information as defined in the NVMe specification. Supported information is shown in the log pages defined in Table 17:

**Table 17: Supported Log Pages**

| Log Page | Log Identifier |
|---|---|
| Error Information | 01h |
| SMART/Health Information | 02h |
| Firmware Slot Information | 03h |
| Commands Supported and Effects | 05h |
| Device Self-Test Log | 06h |
| Telemetry Host-Initiated | 07h |
| Telemetry Controller-Initiated | 08h |

See the following table for the 512-byte data structure of the SMART/Health Information log page:

**Table 18: SMART/Health Information (Log Identifier 02h)**

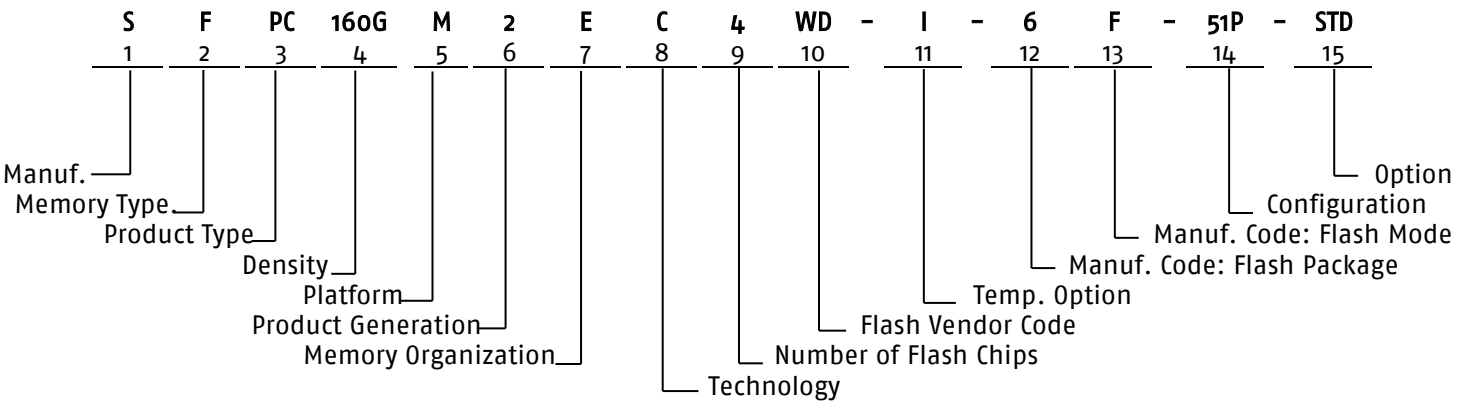
| Byte(s) | Description |
|---|---|
| 0 | Critical warning: for the state of the controller |
| 1-2 | Composite Temperature: in degrees Kelvin |
| 3 | Available Spare: as a percentage of remaining spare capacity |
| 4 | Available Spare Threshold |
| 5 | Percentage Used: Estimate of the percentage of the NVM subsystem life left based on usage |
| 6-31 | Reserved |
| 32-47 | Data Units Read: Number of 512-byte sectors read by the host (in 1000 increments) |
| 48-63 | Data Units Written: Number of 512-byte sectors written by the host (in 1000 increments) |
| 64-79 | Host Read Commands: Number of Read commands completed by the controller |
| 80-95 | Host Write Commands: Number of Write commands completed by the controller |
| 96-111 | Controller Busy Time: Amount of time, in minutes, the controller was busy with I/O commands |
| 112-127 | Power Cycles: Number of power cycles that has occurred over the life of the drive |
| 128-143 | Power On Hours: Number of hours the device has been powered over the life of the drive (does not include the time the device is in low power state conditions) |
| 144-159 | Unsafe Shutdowns: Number of shutdowns that occurred without a shutdown notification |
| 160-175 | Media and Data Integrity Errors: Number of unrecoverable errors, including UECC, CRC checksum failures, and LBA mismatches, that occurred over the life of the drive |
| 176-191 | Number of Error Information Log Entries: Number of entries recorded in the Error Information log over the life of the drive |
| 192-195 | Warning Composite Temperature Time: Amount of time, in minutes, the controller was operational and the Composite Temperature was equal to or greater than the Warning Composite Temperature Threshold (WCTEMP) but less than the Critical Composite Temperature Threshold (CCTEMP) |
| 196-199 | Critical Composite Temperature Time: Amount of time, in minutes, the controller was operational and the Composite Temperature was equal to or greater than the Critical Composite Temperature Threshold (CCTEMP) |
| 200-201 | Temperature Sensor 1: Current temperature, in degrees Kelvin, reported by temperature sensor 1 |
| 202-203 | Temperature Sensor 2: Current temperature, in degrees Kelvin, reported by temperature sensor 2 |
| 204-215 | Not used |
| 216-219 | Thermal Management Temperature 1 Transition Count: number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance |
| 220-223 | Thermal Management Temperature 2 Transition Count: number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance |
| 224-227 | Total Time For Thermal Management Temperature 1: number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance |
| 228-231 | Total Time For Thermal Management Temperature 2: number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance |
| 232-511 | Reserved |

The following data structure is applied to both Telemetry Host-Initiated log and Telemetry Controller-Initiated log:

**Table 19: Telemetry Log (Log Identifier 07h & 08h)**

| Byte(s) | Description |
|---|---|
| **Telemetry Header** | |
| 0 | Log Identifier: This field shall be 07h or 08h |
| 1-4 | Reserved |
| 5-7 | IEEE OUI Identifier (IEEE): |
| 4 | Telemetry Host-Initiated Data Area 1 Last Block: This field shall be 0001h |
| 10-381 | Reserved |
| 382 | Telemetry Controller-Initiated Data Available |
| 383 | Telemetry Controller-Initiated Data Generation Number |
| 384-511 | Reserved |
| **Telemetry Data Block 1** | |
| 528-529 | Minimum Temperature, in degrees Kelvin |
| 530-531 | Current Temperature, in degrees Kelvin |
| 530-531 | Maximum Temperature, in degrees Kelvin |
| 560-561 | Number of valid spare blocks |
| 562-563 | Number of initial spare blocks |
| 564-565 | Run Time Bad Block Count |
| 596-599 | Maximum Erase Count |
| 604-607 | Average Erase Count |
| 640 | Remaining Life Percentage Based On P/E |
| 772-776 | NVMe/PCIe Reset Count |
| 804-807 | PCIe Gen1 Link Count |
| 808-811 | PCIe Gen2 Link Count |
| 812-815 | PCIe Gen3 Link Count |
| 816-823 | PCIe ECRC Event Count |
| 824-831 | PCIe LCRC Event Count |
| 873 | PCIe Power On Link Speed |
| 876 | PCIe Current Link Speed |
| 877 | PCIe Current Link Width |
| 878 | PCIe ASPM Enabled |
| 879 | PCIe L1 Sub State Enabled |
| 880-887 | PS3 Resume Count |
| 888-895 | PS4 Resume Count |
| 932-935 | PCIe x1 Link Count |
| 936-939 | PCIe x2 Link Count |
| 940-943 | PCIe x3 Link Count |
| 944-951 | PCIe L1 Event Count |

# 10. Part Number Decoder




## 10.1 Manufacturer

| | |
|---|---|
| Swissbit Code | S |

## 10.2 Memory Type

| | |
|---|---|
| Flash | F |

## 10.3 Product Type

| | |
|---|---|
| PCIe Interface | PC |

## 10.4 Density

| | |
|---|---|
| 5 GBytes | 005G |
| 10 GBytes | 010G |
| 20 GBytes | 020G |
| 40 GBytes | 040G |
| 80 GBytes | 080G |
| 160 GBytes | 160G |

## 10.5 Platform

| | |
|---|---|
| M.2 SSD | M |

## 10.6 Product Generation

## 10.7 Memory Organization

| | |
|---|---|
| Flash Products Embedded BGA | E |

## 10.8 Technology

| | |
|---|---|
| N-26m2 Series | C |

## 10.9 Number of channels

| | |
|---|---|
| 1 Flash channel | 1 |
| 2 Flash channel | 2 |
| 4 Flash channel | 4 |

## 10.10 Flash Code

| | |
|---|---|
| Toshiba / Kioxia | T0 |
| Western Digital | WD |

## 10.11 Temperature Option

| | |
|---|---|
| Industrial Temperature Range: -40 °C to 85 °C | I |

## 10.12 Die Classification

| | |
|---|---|
| 3D TLC MONO (single die package) | 5 |
| 3D TLC DDP (dual die package) | 6 |

## 10.13 Pin Mode

| | |
|---|---|
| Single nCE and Single R/nB | E |
| Dual nCE and Dual R/nB | F |

## 10.14 Drive configuration XYZ

### X = Dimension and Assembly

| Dimension | Assembly | X |
|---|---|---|
| 2230 | Single-Sided | A |
| 2242 | Single-Sided | 1 |
| 2280 | Single-Sided | 5 |

### Y = Firmware Revision

| FW Revision | Y |
|---|---|
| Standard | 1 |

### Z = Feature

| Feature | Z |
|---|---|
| SLC Mode | P |

## 10.15 Option

| | |
|---|---|
| Standard | STD |

# 11. Marking Specification

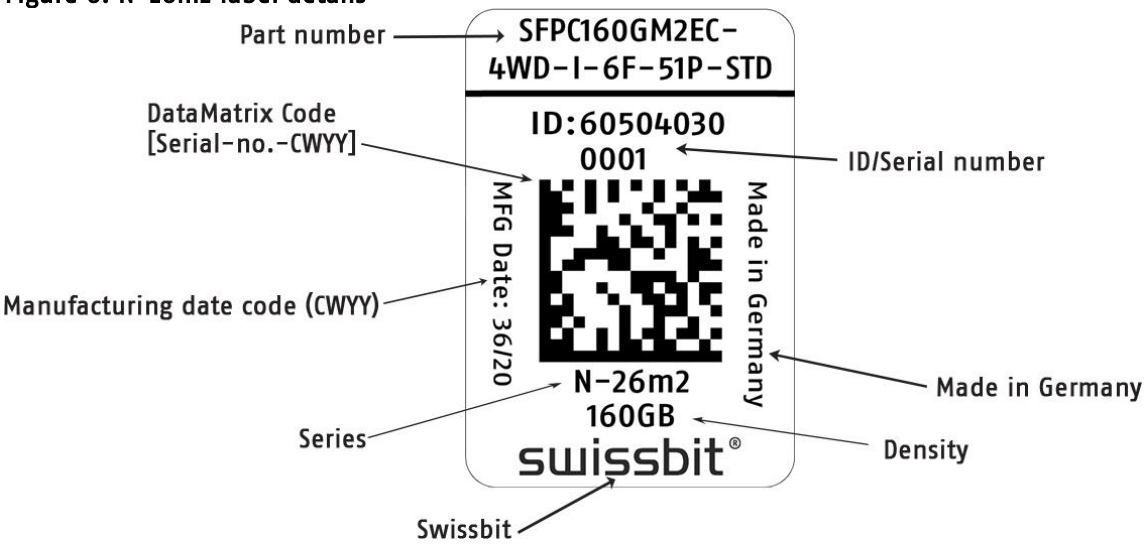
## *11.1 Top View*

Figure 5: N-26m2 top view




## *11.2 Print on the label*

Figure 6: N-26m2 label details



# 12. Revision History

Table 20: Document Revision History

| Date | Revision | Description | Revision Details |
|---|---|---|---|
| 17-July-2020 | 1.00 | First release | Doc. req. no. 3996 |
| 03-September-2020 | 1.01 | Updated product illustrations | Doc. req. no. 4002 |
| 27-November-2020 | 1.02 | Added 160GB 2-Lane product, updated performance and current values | Doc. req. no. 4237 |

**Disclaimer:**
No part of this document may be copied or reproduced in any form or by any means, or transferred to any third party, without the prior written consent of an authorized representative of Swissbit AG ("SWISSBIT"). The information in this document is subject to change without notice. SWISSBIT assumes no responsibility for any errors or omissions that may appear in this document and disclaims responsibility for any consequences resulting from the use of the information set forth herein. SWISSBIT makes no commitments to update or to keep current information contained in this document. The products listed in this document are not suitable for use in applications such as, but not limited to, aircraft control systems, aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. Moreover, SWISSBIT does not recommend or approve the use of any of its products in life support devices or systems or in any application where failure could result in injury or death. If a customer wishes to use SWISSBIT products in applications not intended by SWISSBIT, said customer must contact an authorized SWISSBIT representative to determine SWISSBIT willingness to support a given application. The information set forth in this document does not convey any license under the copyrights, patent rights, trademarks or other intellectual property rights claimed and owned by SWISSBIT. The information set forth in this document is considered to be "Proprietary" and "Confidential" property owned by SWISSBIT.

ALL PRODUCTS SOLD BY SWISSBIT ARE COVERED BY THE PROVISIONS APPEARING IN SWISSBIT'S TERMS AND CONDITIONS OF SALE ONLY, INCLUDING THE LIMITATIONS OF LIABILITY, WARRANTY AND INFRINGEMENT PROVISIONS. SWISSBIT MAKES NO WARRANTIES OF ANY KIND, EXPRESS, STATUTORY, IMPLIED OR OTHERWISE, REGARDING INFORMATION SET FORTH HEREIN OR REGARDING THE FREEDOM OF THE DESCRIBED PRODUCTS FROM INTELLECTUAL PROPERTY INFRINGEMENT AND EXPRESSLY DISCLAIMS ANY SUCH WARRANTIES INCLUDING WITHOUT LIMITATION ANY EXPRESS, STATUTORY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

© 2020 SWISSBIT AG All rights reserved.