LP3995 Micropower 150-mA CMOS Voltage Regulator With Active Shutdown

1 Features

- Input Range: 2.5 V to 6 V
- Accurate Output Voltage: ±75 mV / 2%
- Typical Dropout with 150 mA Load: 60 mV
- Virtually Zero Quiescent Current When Disabled
- Low Output Voltage Noise
- Stable With a 1-µF Output Capacitor
- Output Current: 150 mA
- Fast Turnon: 30 µs (Typical)
- Fast Turnoff: 175 µs (Typical)
- Stable With Ceramic Capacitor
- Logic Controlled Enable
- Fast Turnon
- Active Disable for Fast Turnoff
- Thermal-Overload and Short-Circuit Protection
- −40 to +125°C Junction Temperature Range for Operation

2 Applications

- GSM Portable Phones
- CDMA Cellular Handsets
- Wideband CDMA Cellular Handsets
- Bluetooth Devices
- Portable Information Appliances

3 Description

The LP3995 linear regulator is designed to meet the requirements of portable battery-powered applications, providing an accurate output voltage with low noise and low quiescent current. Ideally suited for powering RF and analog devices, this device can also be used to meet more general circuit needs in which a fast turnoff is essential.

For battery-powered applications the low dropout and low ground current provided by the device allows the lifetime of the battery to be maximized. The Enable(/Disable) control function allows the system to further extend the battery lifetime by reducing the power consumption to virtually zero. This function also incorporates an active discharge circuit on the output for faster device shutdown. Where the fast turnoff is not required the LP3999 linear regulator is recommended. The LP3995 also features internal protection against short-circuit currents and overtemperature conditions.

The LP3995 is designed to be stable with small 1-µF ceramic capacitors. The small outline of the LP3995 DSBGA package with the required ceramic capacitors can realize a system application within minimal board area. Performance is specified for a −40°C to +125°C temperature range.

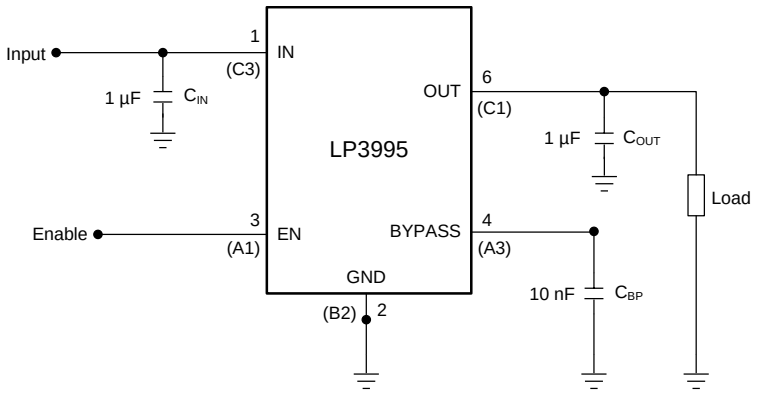
The LP3995 is available in fixed output voltages from 1.5 V to 3.3 V, in DSBGA or WSON packages. For other package options or output-voltage options, contact your local TI sales office.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
LP3995	DSBGA (5)	1.502 mm × 1.045 mm (MAX)
	WSON (6)	3.29 mm × 2.92 mm (NOM)

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 6
6.7 Typical Characteristics ... 7
7 Parameter Measurement Information ... 10
7.1 Input Test Signals ... 10
8 Detailed Description ... 11
8.1 Overview ... 11
8.2 Functional Block Diagram ... 11
8.3 Feature Description ... 11
8.4 Device Functional Modes ... 12
9 Application and Implementation ... 13
9.1 Application Information ... 13
9.2 Typical Application ... 13
10 Power Supply Recommendations ... 17
11 Layout ... 17
11.1 Layout Guidelines ... 17
11.2 Layout Examples ... 17
11.3 DSBGA Mounting ... 18
11.4 DSBGA Light Sensitivity ... 18
12 Device and Documentation Support ... 19
12.1 Documentation Support ... 19
12.2 Community Resources ... 19
12.3 Trademarks ... 19
12.4 Electrostatic Discharge Caution ... 19
12.5 Glossary ... 19
13 Mechanical, Packaging, and Orderable Information ... 19

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2013) to Revision F — **Page**

- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Changed *Thermal Values*, ... 1
- Deleted Lead Temp from *Abs Max* table (in POA); delete *Heatsinking* sections re: specific packages (outdated info) ... 4

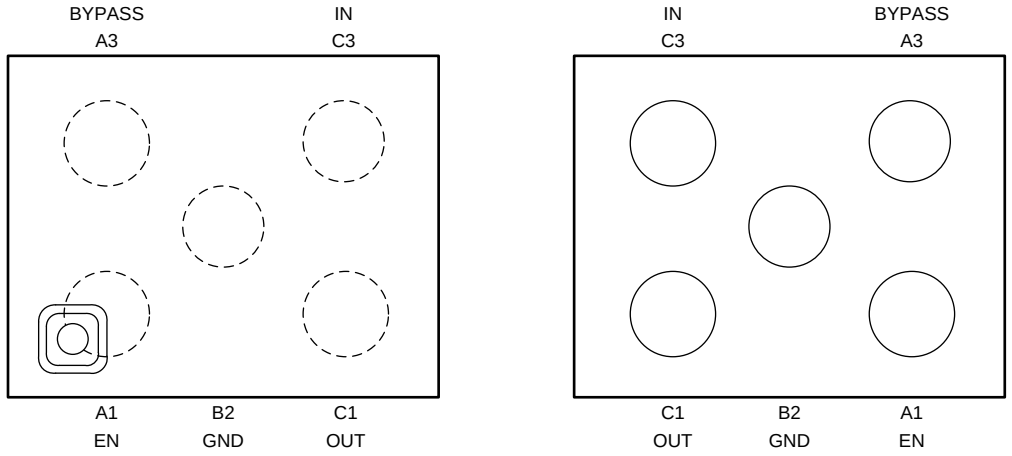
Changes from Revision D (March 2013) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format ... 18

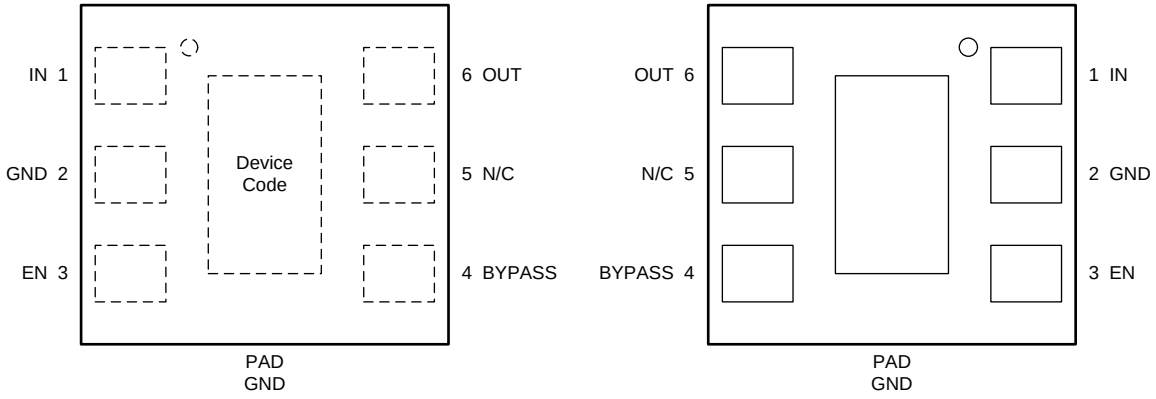
Copyright © 2003–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

YZR Package
5-Pin DSBGA
Top View



NGD Package
6-Pin WSON
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	WSON	DSBGA		
BYPASS	4	A3	—	Bypass capacitor connection. Connect a 0.01-µF capacitor for noise reduction.
EN	3	A1	Input	Enable input; Disables the regulator when ≤ 0.4 V. Enables the regulator when ≥ 0.9 V.
GND	2	B2	Ground	Common ground
GND	Thermal Pad	—	Ground	The exposed thermal pad on the bottom of the WSON package should be connected to a copper thermal pad on the PCB under the package. The use of thermal vias to remove heat from the package into the PCB is recommended. Connect the exposed thermal pad to ground potential or leave floating. Do not connect the thermal pad to any potential other than the same ground potential seen at device pin 2. For additional information on using TI's non pull-back WSON package, see TI Application Note AN- 1187 *Leadless Leadframe Package (LLP)* (SNOA401).
IN	1	C3	Input	Voltage supply input
N/C	5	—	—	No internal connection. This pin can be connected to GND, or left open.
OUT	6	C1	Output	Voltage output. Connect this output to the load circuit.

Copyright © 2003–2015, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2][3]

	MIN	MAX	UNIT
Input voltage, V_{IN}	–0.3	6.5	V
Output voltage	–0.3	(V_{IN} + 0.3 V) to 6.5	V
Enable input voltage	–0.3	6.5	V
Junction temperature		150	°C
Continuous power dissipation[4]	Internally limited		
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(4) In applications where high power dissipation and/or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(MAX)}$) is dependant on the maximum operating junction temperature ($T_{J(MAX-OP)}$), the maximum power dissipation ($P_{D(MAX)}$), and the junction-to-ambient thermal resistance in the application ($R_{\theta JA}$). This relationship is given by: $T_{A(MAX)} = T_{J(MAX-OP)} - (P_{D(MAX)} \times R_{\theta JA})$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage, V_{IN}	2.5		6	V
Enable input voltage	0		6	V
Junction temperature	−40		125	°C
Ambient temperature[1]	−40		85	°C

(1) In applications where high power dissipation and/or poor thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(MAX)}$) is dependant on the maximum operating junction temperature ($T_{J(MAX-OP)}$), the maximum power dissipation ($P_{D(MAX)}$), and the junction-to-ambient thermal resistance in the application ($R_{\theta JA}$). This relationship is given by: $T_{A(MAX)} = T_{J(MAX-OP)} - (P_{D(MAX)} \times R_{\theta JA})$.

Copyright © 2003–2015, Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC[1]		LP3995		UNIT
		YZR (DSBGA)	NGD (WSON)	
		5 PINS	6 PINS	
$R_{\theta JA}$[2]	Junction-to-ambient thermal resistance, High-K	181.2	68.5[3]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.8	71.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	107.9	35.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	107.9	35.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	8.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: *JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
(3) The PCB for the NGD (WSON) package $R_{\theta JA}$ includes two (2) thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.

6.5 Electrical Characteristics

Unless otherwise noted, V_{EN} = 1.5 V, V_{IN} = V_{OUT} + 1 V, C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 1 µF, C_{BYPASS} = 0.01 µF. Typical (TYP) values and limits apply for T_J = 25°C; minimum (MIN) and maximum (MAX) apply over the full temperature range for operation, −40 to +125°C, unless otherwise specified in the Test Conditions. [1][2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		2.5		6	V
DEVICE OUTPUT: 1.5 ≤ V_{OUT} < 1.8V						
ΔV_{OUT}	Output voltage tolerance	I_{OUT} = 1 mA, T_J = 25°C	–50		50	mV
		I_{OUT} = 1 mA	–75		75	
	Line regulation error	V_{IN} = ($V_{OUT(NOM)}$+1 V) to 6V, I_{OUT} = 1 mA	–3.5		3.5	µV/mA
	Load regulation error, DSBGA	I_{OUT} = 1 mA to 150 mA		10	75	µV/mA
	Load regulation error, WSON	I_{OUT} = 1 mA to 150 mA		70	125	µV/mA
PSRR	Power supply rejection ratio[3]	f = 1 kHz, I_{OUT} = 1 mA		55		dB
		f = 10 kHz, I_{OUT} = 1 mA		53		
DEVICE OUTPUT: 1.8 V ≤ V_{OUT} < 2.5 V						
ΔV_{OUT}	Output voltage tolerance	I_{OUT} = 1 mA, T_J = 25°C	–50		50	mV
		I_{OUT} = 1 mA	–75		75	
	Line regulation error, DSBGA	V_{IN} = ($V_{OUT(NOM)}$+1 V) to 6 V, I_{OUT} = 1 mA	–2.5		2.5	mV/V
	Line regulation error, WSON	V_{IN} = ($V_{OUT(NOM)}$+1 V) to 6 V I_{OUT} = 1 mA	–3.5		3.5	mV/V
	Load regulation error, DSBGA	I_{OUT} = 1 mA to 150 mA		10	75	µV/mA
	Load regulation error, WSON	I_{OUT} = 1 mA to 150 mA		80	125	µV/mA
PSRR	Power supply rejection ratio[3]	f = 1 kHz, I_{OUT} = 1 mA		55		dB
		f = 10 kHz, I_{OUT} = 1 mA		50		

(1) All limits are ensured. All electrical characteristics having room-temperature limits are tested during production at T_J = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) $V_{OUT(NOM)}$ is the stated output voltage option for the device.
(3) This electrical specification is ensured by design.

Copyright © 2003–2015, Texas Instruments Incorporated

Electrical Characteristics (continued)

Unless otherwise noted, V_{EN} = 1.5 V, V_{IN} = V_{OUT} + 1 V, C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 1 µF, C_{BYPASS} = 0.01 µF. Typical (TYP) values and limits apply for T_J = 25°C; minimum (MIN) and maximum (MAX) apply over the full temperature range for operation, −40 to +125°C, unless otherwise specified in the Test Conditions. (1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE OUTPUT: 2.5 V ≤ V_{OUT} ≤ 3.3 V						
ΔV_{OUT}	Output voltage tolerance	I_{OUT} = 1 mA, T_J = 25°C	–2		2	% of $V_{OUT(NOM)}$
		I_{OUT} = 1 mA	–3		3	
	Line regulation error	V_{IN} = ($V_{OUT(NOM)}$+1 V) to 6 V I_{OUT} = 1 mA	–0.1		0.1	%/V
	Load regulation error, DSBGA	I_{OUT} = 1 mA to 150 mA		0.0004	0.002	%/mA
	Load regulation error, WSON	I_{OUT} = 1 mA to 150 mA		0.002	0.005	%/mA
	Dropout voltage	I_{OUT} = 1 mA		0.4	2	mV
		I_{OUT} = 150 mA		60	100	
PSRR	Power supply rejection ratio (3)	f = 1 kHz, I_{OUT} = 1 mA		60		dB
		f = 10 kHz, I_{OUT} = 1 mA		50		
FULL V_{OUT} RANGE						
I_{LOAD}	Load current	See (3)(4)	0			µA
I_Q	Quiescent current	V_{EN} = 1.5 V, I_{OUT} = 0 mA		85	150	µA
		V_{EN} = 1.5 V, I_{OUT} = 150 mA		140	200	
		V_{EN} = 0.4 V		0.003	1.5	
I_{SC}	Short-circuit current limit			450		mA
E_N	Output noise voltage (3)	BW = 10 Hz to 100 kHz, V_{IN} = 4.2 V, I_{OUT} = 1 mA		25		μV_{RMS}
$T_{SHUTDOWN}$	Thermal shutdown	Temperature		160		°C
		Hysteresis		20		
ENABLE CONTROL CHARACTERISTICS						
I_{EN}	Maximum input current at EN input	V_{EN} = 0 V and V_{IN} = 6 V		0.001		µA
V_{IL}	Low input threshold				0.4	V
V_{IH}	High input threshold		0.9			V

(4) The device maintains a stable, regulated output voltage without load.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{ON}	Turnon time to 95% level (1)(2)		30		µs
t_{OFF}	Turnoff time to 5% level (1)(3)		175		µs

(1) This electrical specification is ensured by design.
(2) Time from V_{EN} = 0.9 V to V_{OUT} = 95% ($V_{OUT(NOM)}$).
(3) Time from V_{EN} = 0.4 V to V_{OUT} = 5% ($V_{OUT(NOM)}$).

Copyright © 2003–2015, Texas Instruments Incorporated

6.7 Typical Characteristics

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $V_{IN} = V_{OUT} + 1$ V, $T_A = 25$°C, EN pin is tied to V_{IN}.

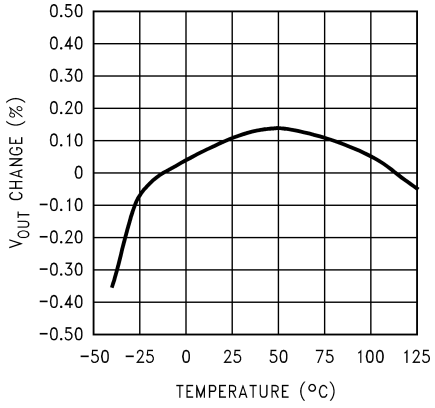
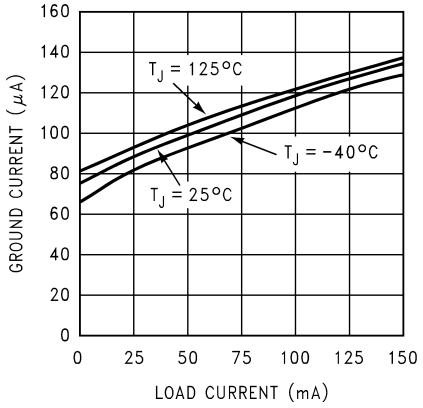
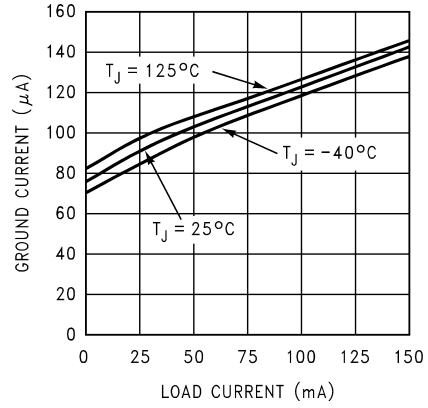


Figure 1. Output Voltage Change vs Temperature



V_{OUT} = 1.8 V

Figure 2. Ground Current vs Load Current



V_{OUT} = 2.8 V

Figure 3. Ground Current vs Load Current

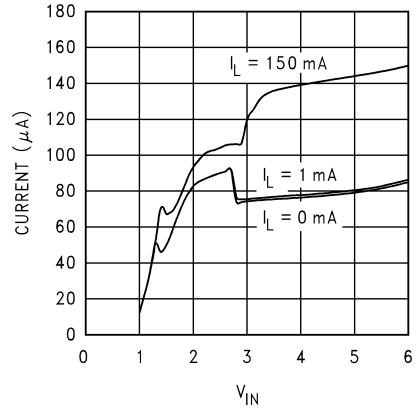


Figure 4. Ground Current vs V_{IN} at 25°C

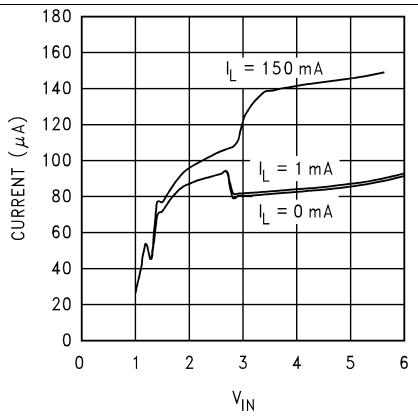


Figure 5. Ground Current vs V_{IN} at 125°C

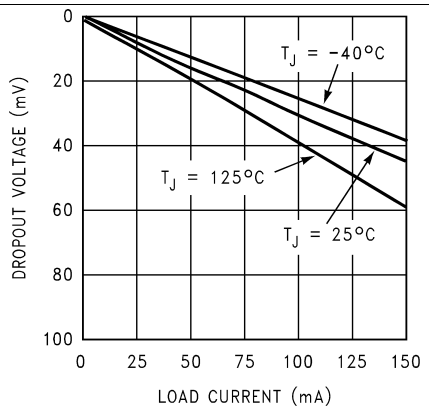


Figure 6. Dropout vs Load Current

Copyright © 2003–2015, Texas Instruments Incorporated

Typical Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $V_{IN} = V_{OUT} + 1$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.

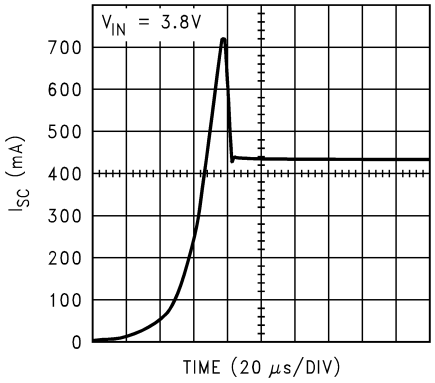
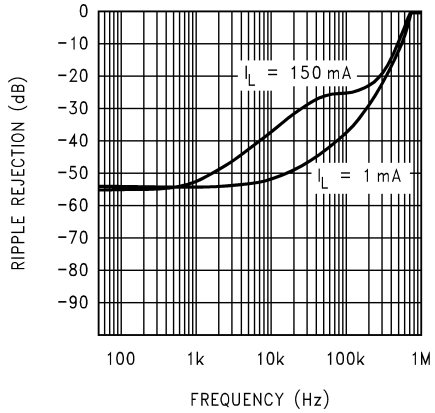
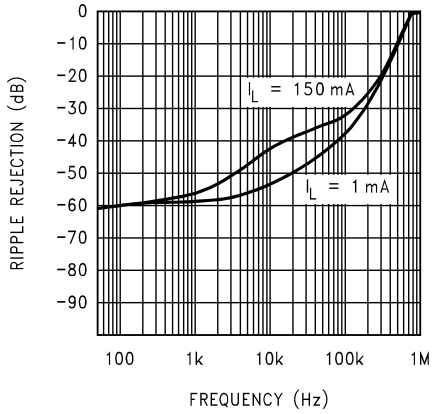


Figure 7. Short-Circuit Current



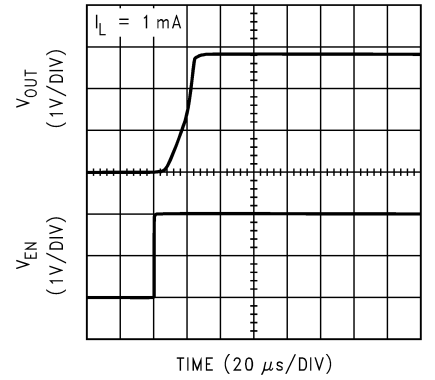
V_{OUT} = 1.8 V

Figure 8. Ripple Rejection



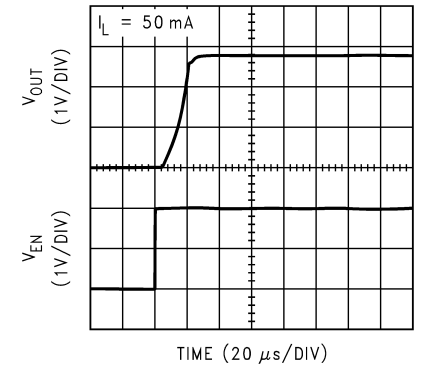
V_{OUT} = 2.8 V

Figure 9. Ripple Rejection



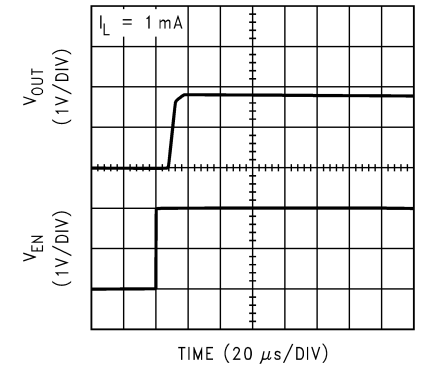
V_{OUT} = 2.8 V

Figure 10. Enable Start-Up Time



V_{OUT} = 2.8 V

Figure 11. Enable Start-Up Time



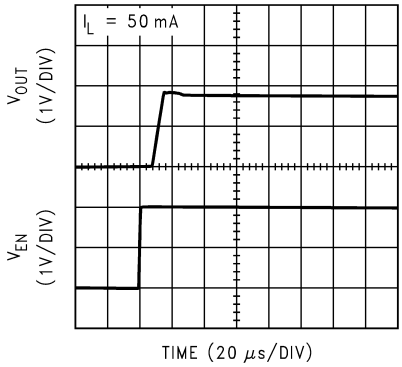
V_{OUT} = 1.8 V

Figure 12. Enable Start-Up Time

Copyright © 2003–2015, Texas Instruments Incorporated

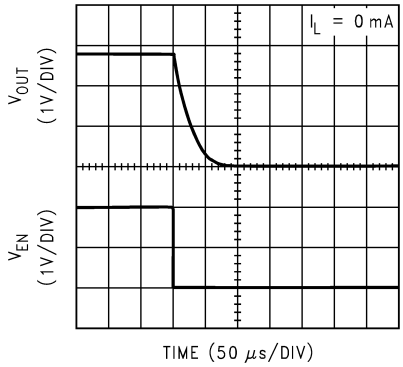
Typical Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT} = 1$ µF ceramic, $V_{IN} = V_{OUT} + 1$ V, $T_A = 25°C$, EN pin is tied to V_{IN}.



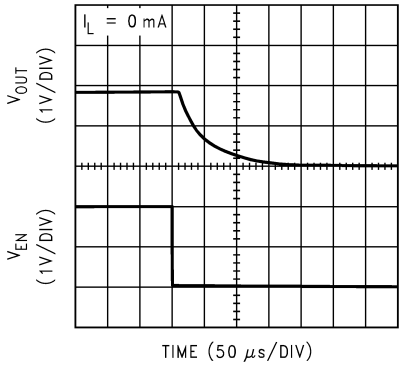
V_{OUT} = 1.8 V

Figure 13. Enable Start-Up Time



V_{OUT} = 2.8 V

Figure 14. Turnoff Time



V_{OUT} = 1.8 V

Figure 15. Turnoff Time

7 Parameter Measurement Information

7.1 Input Test Signals

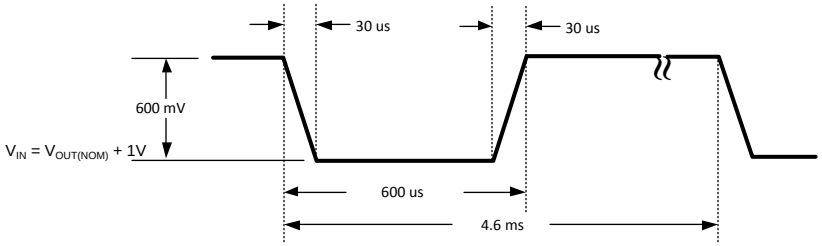


Figure 16. Line Transient Response Input Test Signal

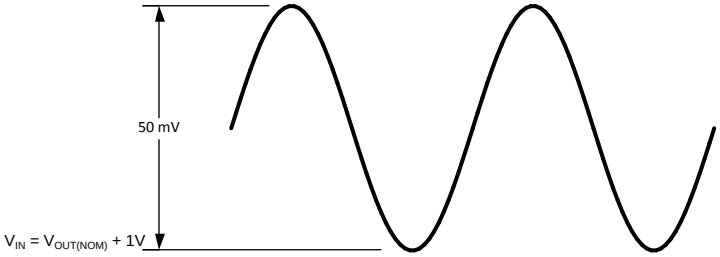


Figure 17. PSRR Input Test Signal

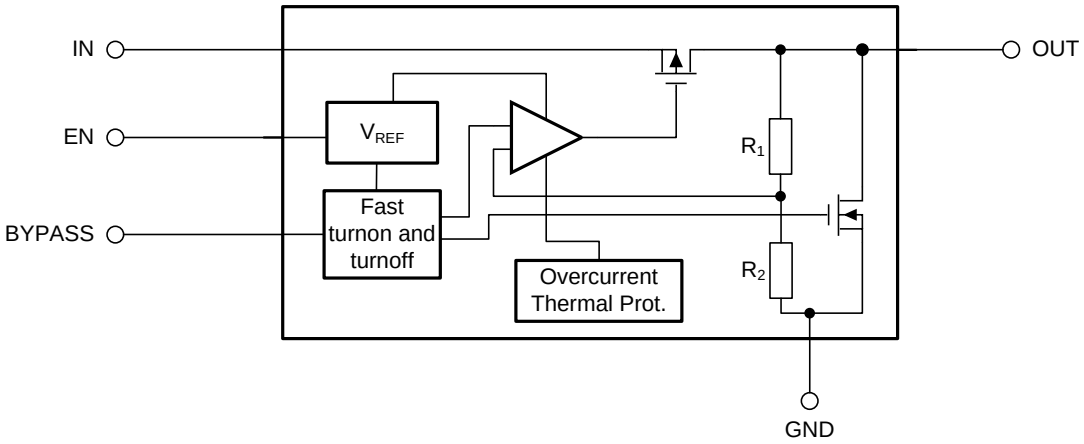
Copyright © 2003–2015, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The LP3995 device is a CMOS voltage regulator with a low input operating voltage tolerance. Key protection circuits, including thermal-overload and short-circuit protection, are integrated in the device. Using the EN pin, the device may be controlled to provide a shutdown state, in which negligible supply current is drawn. The LP3995 is designed to be stable with space-saving ceramic capacitors.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable (EN)

The EN pin is used to control the ON or OFF status of the LP3995. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

8.3.2 Fast Turnoff

When the EN pin voltage is lower than the V_{IL} threshold, the output is disabled, and the pull-down circuitry is activated to discharge the output capacitance.

8.3.3 Low Output Noise

The BYPASS pin is an external connection into the LP3995 band-gap circuitry allows the addition of an external capacitor to reduce output noise . A fast-charge circuit is controlled by the enable circuitry to reduce start-up delays. The capacitor on the BYPASS pin also prevents overshoot on the output during startup.

8.3.4 Output Capacitor

The LP3995 requires at least a 1-µF low ESR ceramic capacitor at the OUT pin.

8.3.5 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry automatically enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating. The thermal shutdown circuitry of the LP3995 has been designed to protect against temporary thermal overload conditions. The thermal shutdown circuitry is not intended to replace proper heat-sinking. Continuously running the LP3995 device into thermal shutdown may degrade device reliability.

Copyright © 2003–2015, Texas Instruments Incorporated

8.4 Device Functional Modes

8.4.1 Enable Operation

The LP3995 may be switched ON or OFF by a logic input at the EN pin, V_{EN}. A high voltage at this pin turns the device on. When the EN pin is low, the regulator output is off and the device typically consumes 3 nA. If the application does not require the shutdown feature, the EN pin should be tied to V_{IN} to keep the regulator output permanently on. To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turn-on/off voltage thresholds listed in *Electrical Characteristics* under V_{IL} and V_{IH}.

Copyright © 2003–2015, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP3995 can provide 150-mA output current with 2.5-V to 6-V input. It is stable with a 1-µF ceramic output capacitor. An optional external bypass capacitor reduces the output noise without slowing down the load transient response. Typical output noise is 25 μV_{RMS} at frequencies from 10 Hz to 100 kHz. Typical power supply rejection is 60 dB at 1 kHz.

9.2 Typical Application

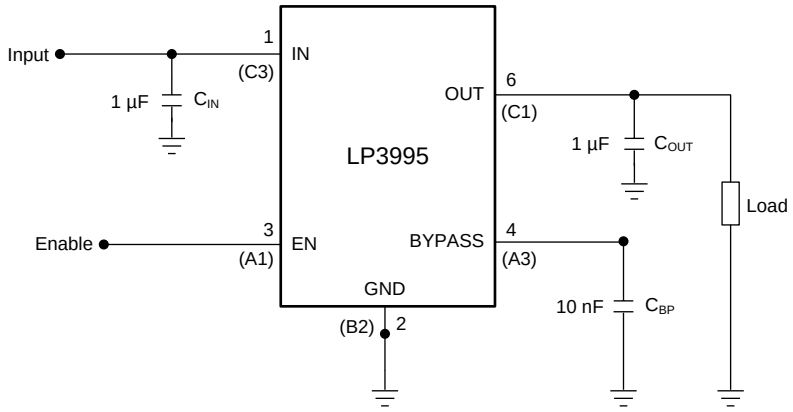


Figure 18. LP3995 Typical Application

9.2.1 Design Requirements

For typical CMOS voltage regulator applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.5 V
Minimum output voltage	1.8 V
Output current	150 mA

9.2.2 Detailed Design Procedure

9.2.2.1 External Capacitors

In common with most regulators, the LP3995 requires external capacitors to ensure stable operation. The LP3995 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

9.2.2.2 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected between the LP3995 IN pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Copyright © 2003–2015, Texas Instruments Incorporated

NOTE

Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the equivalent series resistance (ESR) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance remains ≅ 1 µF over the entire operating temperature range.

9.2.2.3 Output Capacitor

The LP3995 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types Z5U, Y5V or X7R) in the 1-µF to 10-µF range, and with ESR between 5 mΩ to 500 mΩ, is suitable in the LP3995 application circuit.

For this device the output capacitor should be connected between the OUT pin and ground.

It may also be possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

Table 2. Recommended Output Capacitor

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	Units
C_{OUT}	Output Capacitor	Capacitance(1)	0.7	1		µF
		ESR	5		500	mΩ

(1) The capacitor tolerance should be ±30% or better over the temperature range. The recommended capacitor type is X7R however, dependant on the application X5R, Y5V, and Z5U can also be used.

9.2.2.4 No-Load Stability

The LP3995 remains stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

9.2.2.5 Capacitor Characteristics

The LP3995 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 1 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP3995.

The temperature performance of ceramic capacitors varies by type. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to +85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range. Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum increases about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

Copyright © 2003–2015, Texas Instruments Incorporated

9.2.2.6 Noise Bypass Capacitor

A bypass capacitor should be connected between the BYPASS pin and ground to significantly reduce the noise at the regulator output. This device pin connects directly to a high impedance node within the bandgap reference circuitry. Any significant loading on this node causes a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy.

The use of a 0.01-µF bypass capacitor is strongly recommended to prevent overshoot on the output during start-up.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High quality ceramic capacitors with NPO or COG dielectric typically have very low leakage. Polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

Unlike many other LDOs, the addition of a noise reduction capacitor does not effect the transient response of the device.

9.2.2.7 Fast Turnoff and Turnon

The controlled switch-off feature of the device provides a fast turn off by discharging the output capacitor via an internal FET device. This discharge is current limited by the R_{DSon} of this switch. Fast turnon is ensured by control circuitry within the reference block allowing a very fast ramp of the output voltage to reach the target voltage.

9.2.2.8 Power Dissipation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the device, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

Equation 1 restates the equation given in note 5 of *Absolute Maximum Ratings*:

$$T_{A(MAX)} = T_{J(MAX-OP)} - (P_{D(MAX)} \times R_{\theta JA}) \quad (1)$$

The allowable power dissipation for the device in a given package can be calculated:

$$P_D = T_{J(MAX)} - T_A / R_{\theta JA} \quad (2)$$

With an $R_{\theta JA}$ = 255°C/W, the device in the DSBGA package returns a value of 392 mW with a maximum junction temperature of 125°C.

With an $R_{\theta JA}$ = 88°C/W, the device in the WSON package returns a value of 1.136 mW with a maximum junction temperature of 125°C.

The actual power dissipation across the device can be represented by Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. Equation 2 and Equation 3 should be used to determine the optimum operating conditions for the device in the application.

This thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper-spreading area and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper area acting as a heatsink.

9.2.2.9 Estimating Junction Temperature

The EIA/JEDEC standard recommends the use of psi (Ψ) thermal characteristics to estimate the junction temperatures of surface mount devices on a typical PCB board application. These characteristics are not true thermal resistance values, but rather package specific thermal characteristics that offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal characteristics (Ψ_{JT} and Ψ_{JB}) are given in *Thermal Information* and are used in accordance with Equation 4 or Equation 5.

Copyright © 2003–2015, Texas Instruments Incorporated

$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$

where

- $P_{D(MAX)}$ is explained in Equation 2
- T_{TOP} is the temperature measured at the center-top of the device package. (4)

$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$

where

- $P_{D(MAX)}$ is explained in Equation 2.
- T_{BOARD} is the PCB surface temperature measured 1-mm from the device package and centered on the package edge. (5)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see TI Application Report *Semiconductor and IC Package Thermal Metrics* (SPRA953); for more information about measuring T_{TOP} and T_{BOARD}, see the TI Application Report *Using New Thermal Metrics* (SBVA025); and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017). Aforementioned application notes are available at www.ti.com.

9.2.3 Application Curves

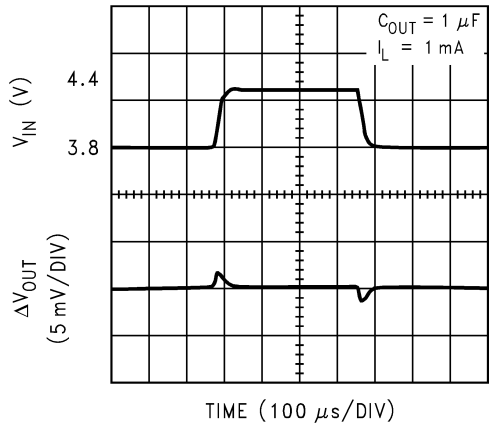


Figure 19. Line Transient Response

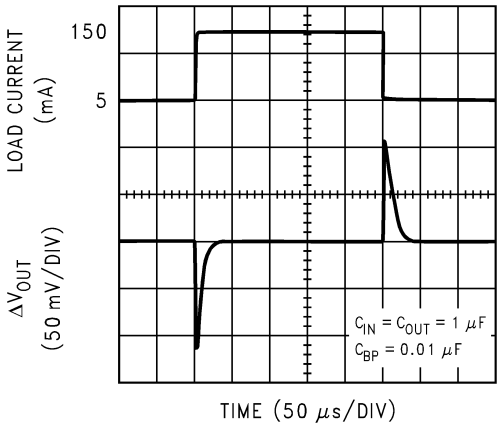


Figure 20. Load Transient Response

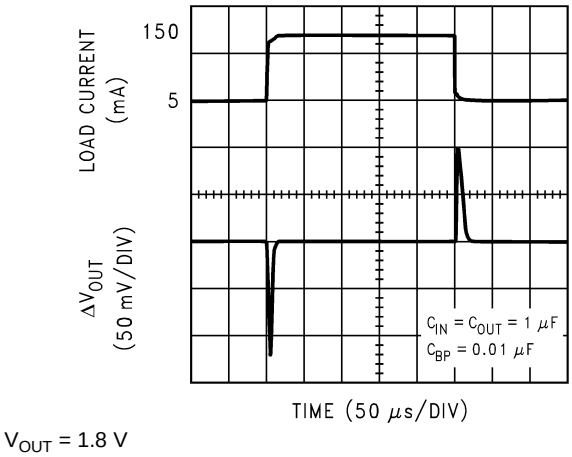


Figure 21. Load Transient Response

Copyright © 2003–2015, Texas Instruments Incorporated

10 Power Supply Recommendations

The LP3995 is designed to operate from an input voltage supply range from 2.5 V to 6 V.

11 Layout

11.1 Layout Guidelines

The dynamic performance of the LP3995 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP3995. Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP3995, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LP3995 ground pin using as wide, and as short, of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These add parasitic inductances and resistance that result in inferior performance especially during transient conditions.

11.2 Layout Examples

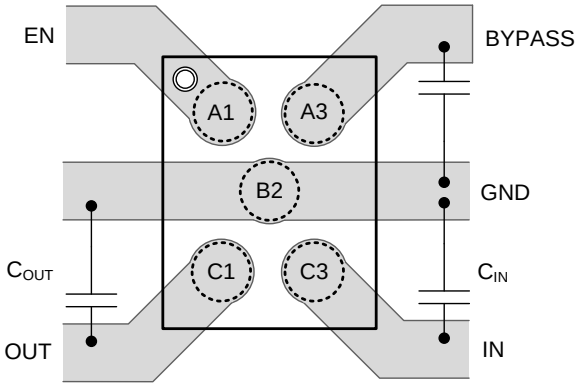


Figure 22. LP3995 DSBGA Layout

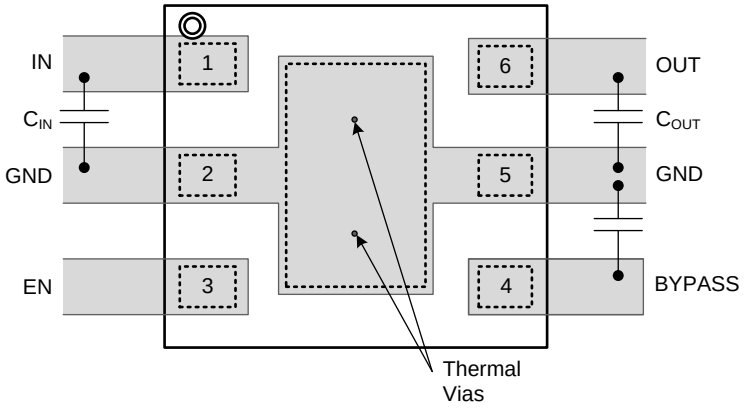


Figure 23. LP3995 WSON Layout

11.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques that are detailed in TI's AN-1112 Application Report (SNVA009). Referring to the section *Surface Mount Assembly Considerations*, it should be noted that the pad style which must be used with the 5-pin package is NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

11.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct sunlight may cause mis-operation of the device. Light sources such as halogen lamps can affect electrical performance if they are situated in proximity to the device.

The wavelengths that have the most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has little effect on performance. Tests carried out on a DSBGA test board showed a negligible effect on the regulated output voltage when brought within 1 cm of a fluorescent lamp. A deviation of less than 0.1% from nominal output voltage was observed.

Copyright © 2003–2015, Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For additional information, see the following:

- TI Application Note *DSBGA Wafer Level Chip Scale Package* (SNVA009).
- TI Application Note *Leadless Leadframe Package (LLP)* (SNOA401).
- TI Application Report *Semiconductor and IC Package Thermal Metrics* (SPRA953).
- TI Application Report *Using New Thermal Metrics* (SBVA025).
- TI Application Report *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* (SZZA017).

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2003–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3995ILD-1.5/NOPB	Active	Production	WSON (NGD) | 6	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L020B
LP3995ILD-1.5/NOPB.A	Active	Production	WSON (NGD) | 6	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L020B
LP3995ILD-1.8/NOPB	Active	Production	WSON (NGD) | 6	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L022B
LP3995ILD-1.8/NOPB.A	Active	Production	WSON (NGD) | 6	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L022B
LP3995ILD-2.8/NOPB	Active	Production	WSON (NGD) | 6	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L026B
LP3995ILD-2.8/NOPB.A	Active	Production	WSON (NGD) | 6	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L026B
LP3995ILD-3.0/NOPB	Active	Production	WSON (NGD) | 6	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L030B
LP3995ILD-3.0/NOPB.A	Active	Production	WSON (NGD) | 6	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L030B
LP3995ILDX-2.8/NO.A	Active	Production	WSON (NGD) | 6	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L026B
LP3995ILDX-2.8/NOPB	Active	Production	WSON (NGD) | 6	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	L026B
LP3995ITL-1.5/NOPB	Active	Production	DSBGA (YZR) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITL-1.5/NOPB.A	Active	Production	DSBGA (YZR) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITL-1.8/NOPB	Active	Production	DSBGA (YZR) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITL-1.8/NOPB.A	Active	Production	DSBGA (YZR) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITL-2.5/NOPB	Active	Production	DSBGA (YZR) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITL-2.5/NOPB.A	Active	Production	DSBGA (YZR) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITL-2.8/NOPB	Active	Production	DSBGA (YZR) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITL-2.8/NOPB.A	Active	Production	DSBGA (YZR) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITL-3.0/NOPB	Active	Production	DSBGA (YZR) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITL-3.0/NOPB.A	Active	Production	DSBGA (YZR) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITLX-1.5/NO.A	Active	Production	DSBGA (YZR) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITLX-1.5/NOPB	Active	Production	DSBGA (YZR) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITLX-1.8/NO.A	Active	Production	DSBGA (YZR) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITLX-1.8/NOPB	Active	Production	DSBGA (YZR) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITLX-1.9/NO.A	Active	Production	DSBGA (YZR) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITLX-1.9/NOPB	Active	Production	DSBGA (YZR) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITLX-2.8/NO.A	Active	Production	DSBGA (YZR) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITLX-2.8/NOPB	Active	Production	DSBGA (YZR) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9
LP3995ITLX-3.0/NO.A	Active	Production	DSBGA (YZR) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP3995ITLX-3.0/NOPB	Active	Production	DSBGA (YZR) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	9

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

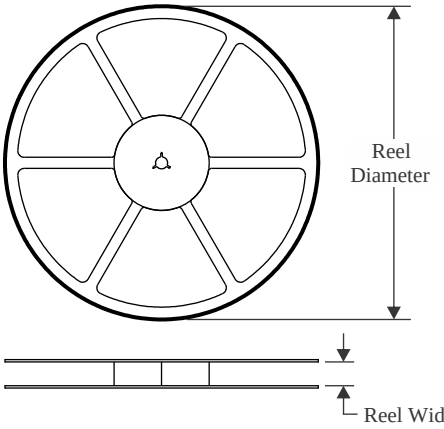
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

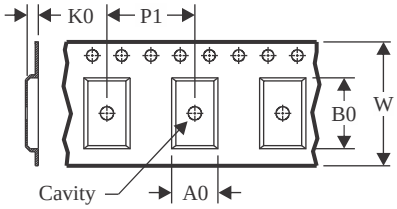
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

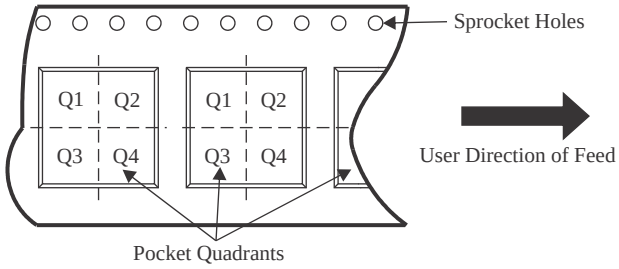


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

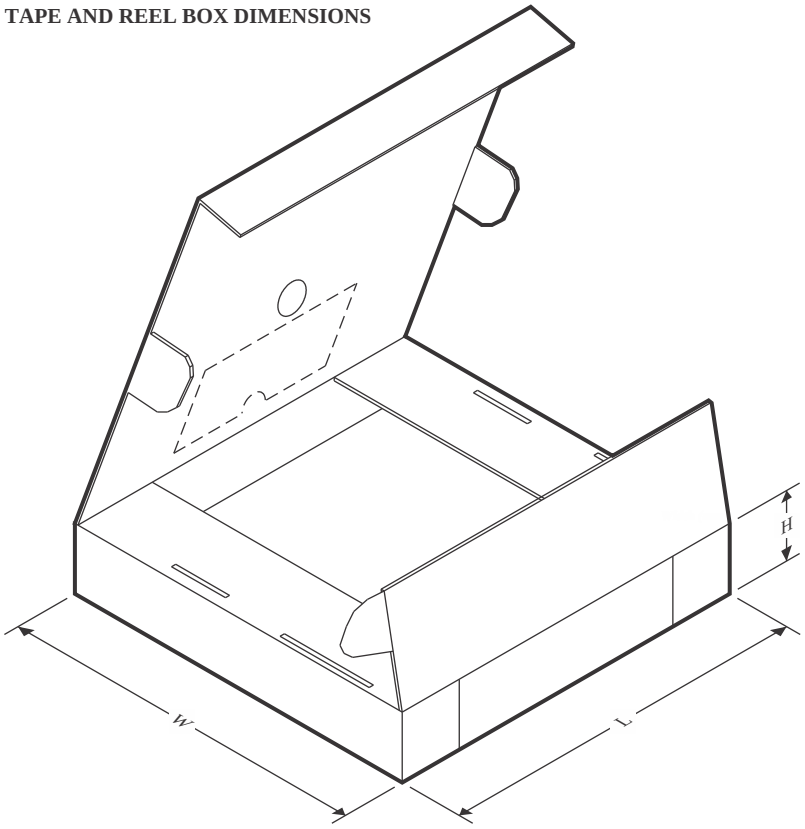
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3995ILD-1.5/NOPB	WSON	NGD	6	1000	177.8	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP3995ILD-1.8/NOPB	WSON	NGD	6	1000	177.8	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP3995ILD-2.8/NOPB	WSON	NGD	6	1000	177.8	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP3995ILD-3.0/NOPB	WSON	NGD	6	1000	177.8	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP3995ILDX-2.8/NOPB	WSON	NGD	6	4500	330.0	12.4	3.6	3.2	1.0	8.0	12.0	Q1
LP3995ITL-1.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3995ITL-1.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3995ITL-2.5/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3995ITL-2.8/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3995ITL-3.0/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3995ITLX-1.5/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3995ITLX-1.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3995ITLX-1.9/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3995ITLX-2.8/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1
LP3995ITLX-3.0/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.09	1.55	0.76	4.0	8.0	Q1

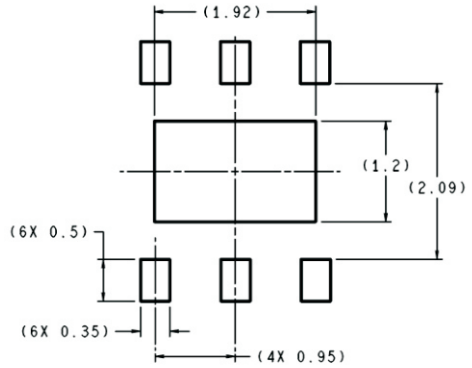
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

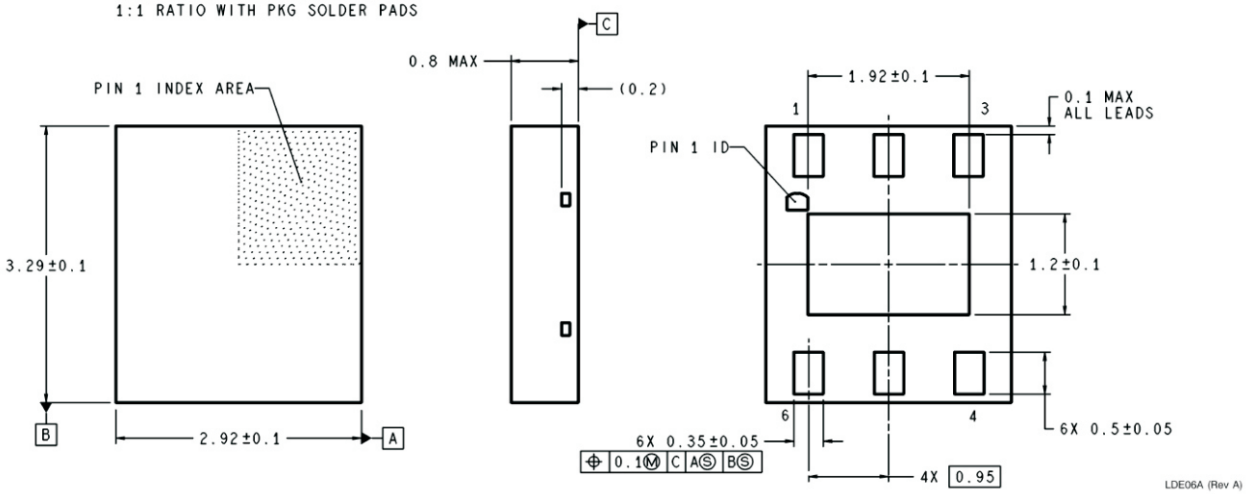
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3995ILD-1.5/NOPB	WSON	NGD	6	1000	208.0	191.0	35.0
LP3995ILD-1.8/NOPB	WSON	NGD	6	1000	208.0	191.0	35.0
LP3995ILD-2.8/NOPB	WSON	NGD	6	1000	208.0	191.0	35.0
LP3995ILD-3.0/NOPB	WSON	NGD	6	1000	208.0	191.0	35.0
LP3995ILDX-2.8/NOPB	WSON	NGD	6	4500	356.0	356.0	36.0
LP3995ITL-1.5/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LP3995ITL-1.8/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LP3995ITL-2.5/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LP3995ITL-2.8/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LP3995ITL-3.0/NOPB	DSBGA	YZR	5	250	208.0	191.0	35.0
LP3995ITLX-1.5/NOPB	DSBGA	YZR	5	3000	208.0	191.0	35.0
LP3995ITLX-1.8/NOPB	DSBGA	YZR	5	3000	208.0	191.0	35.0
LP3995ITLX-1.9/NOPB	DSBGA	YZR	5	3000	208.0	191.0	35.0
LP3995ITLX-2.8/NOPB	DSBGA	YZR	5	3000	208.0	191.0	35.0
LP3995ITLX-3.0/NOPB	DSBGA	YZR	5	3000	208.0	191.0	35.0

NGD0006A

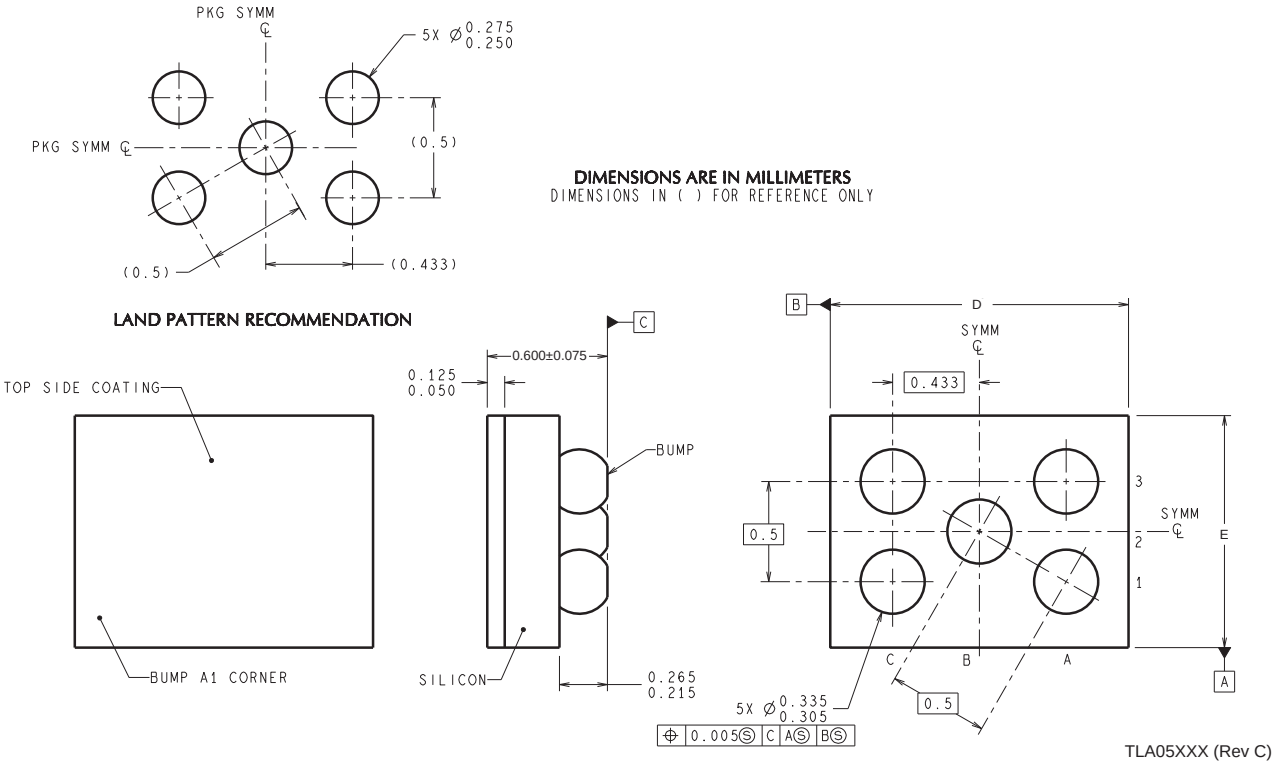


DIMENSIONS ARE IN MILLIMETERS

RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS



YZR0005



D: Max = 1.502 mm, Min =1.441 mm

E: Max = 1.045 mm, Min =0.984 mm

4215043/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated