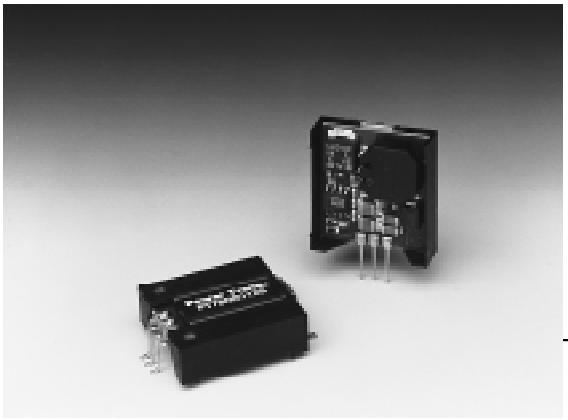
PT78NR100 Series

Power Trends Products from Texas Instruments

1 Amp Plus to Minus Voltage Integrated Switching Regulator

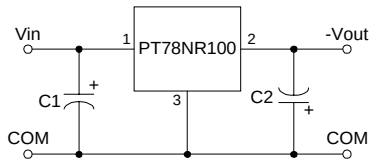
SLTS058B
(Revised 8/31/2000)



- Negative output from positive input
- Wide Input Range
- Self-Contained Inductor
- Short Circuit Protection
- Over-Temperature Protection
- Fast Transient Response

The PT78NR100 Series creates a negative output voltage from a positive input voltage greater than 7V. These easy-to-use, 3-terminal, Integrated Switching Regulators (ISRs) have maximum output power of 5 watts and a negative output voltage that is laser trimmed. They also have excellent line and load regulation.

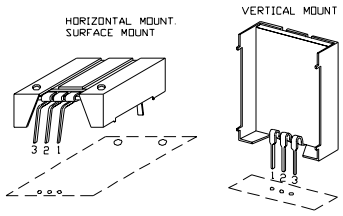
Standard Application



C1 = Required 100µF electrolytic (1)
C2 = Required 100µF electrolytic (1)

Pin-Out Information

Pin	Function
1	$+V_{in}$
2	$-V_{out}$
3	GND



Pkg Style 500

Ordering Information

PT78NR1 XX Y

Output Voltage	Package Suffix
03 = -3.0 Volts	**V** = Vertical Mount
05 = -5.0 Volts	**S** = Surface Mount
52 = -5.2 Volts	**H** = Horizontal Mount
06 = -6.0 Volts	
07 = -7.0 Volts	
08 = -8.0 Volts	
09 = -9.0 Volts	
10 = -10.0 Volts	
12 = -12.0 Volts	
14 = -13.9 Volts	
15 = -15.0 Volts	

Specifications

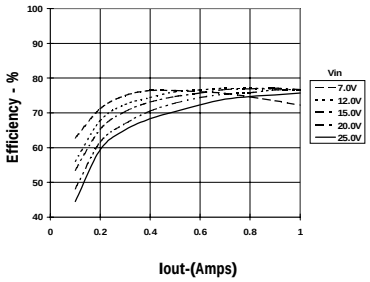
Characteristics (T_a= 25°C unless noted)	Symbols	Conditions	PT78NR100 SERIES Min	Typ	Max	Units
Output Current	I_o	Over V_{in} range V_o=-5V	0.05 (2)	—	1.00	A
		V_o=-6V	0.05 (2)	—	0.8	
		V_o=-7, -8, -9V	0.05 (2)	—	0.55	
		V_o=-10V	0.05 (2)	—	0.5	
		V_o=-12V	0.05 (2)	—	0.40	
		V_o=-13.9, -15V	0.05 (2)	—	0.30	
Short Circuit Current	I_{sc}	V_{in}=10V	—	4×I_{max}	—	Apk
Inrush Current	I_{ir}	V_{in}=10V	—	4	—	A
	t_{ir}	On start-up	—	0.5	—	mSec
Input Voltage Range	V_{in}	0.1 ≤ I_o ≤ I_{max} V_o=-5V	7	—	25	V
		V_o=-6, -7, -8, -9V	7	—	21	V
		V_o=-10, -12V	7	—	18	V
		V_o=-13.9, -15V	7	—	15	V
Output Voltage Tolerance	ΔV_o	Over V_{in} range, T_a=-20°C to +70°C	—	±1.0	±3.0	%V_o
Line Regulation	Reg_{line}	Over V_{in} range	—	±0.5	±1.0	%V_o
Load Regulation	Reg_{load}	0.1 ≤ I_o ≤ I_{max}	—	±0.5	±1.0	%V_o
V_o Ripple/Noise	V_n	V_{in}=10V, I_o=I_{max}	—	±2	—	%V_o
Transient Response (with 100µF output cap)	t_{tr}	50% load change	—	100	250	µSec
		V_o over/undershoot	—	5.0	—	%V_o
Efficiency	η	V_{in}=10V, I_o=0.5×I_{max}, V_o = -5V	—	75	—	%
Switching Frequency	f_o	Over V_{in} and I_o ranges	600	650	700	kHz
Absolute Maximum Operating Temperature Range	T_a	Free Air Convection, (40-60LFM) Over V_{in} Range	-40	—	+85 (3)	°C
Thermal Resistance	θ_{ja}	Free Air Convection, (40-60LFM)	—	45	—	°C/W
Storage Temperature	T_s	—	-40	—	+125	°C
Mechanical Shock	—	Per Mil-STD-883D, Method 2002.3	—	500	—	G's
Mechanical Vibration	—	Per Mil-STD-883D, Method 2007.2, 20-2000 Hz, soldered in a PC board	—	5	—	G's
Weight	—	—	—	6.5		Grams

Notes: (1) *The PT78NR100 Series requires a 100µF electrolytic or tantalum capacitor at both the input and output for proper operation in all applications. The input capacitor, C_1 must have a ripple current rating ≥600 mArms, and an ESR ≤0.2Ω.*
(2) The ISR will operate down to no load with reduced specifications.
(3) See Thermal Derating chart.

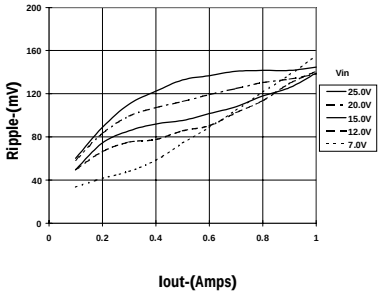
Typical Characteristics

PT78NR105 -5.0 VDC (See Note A)

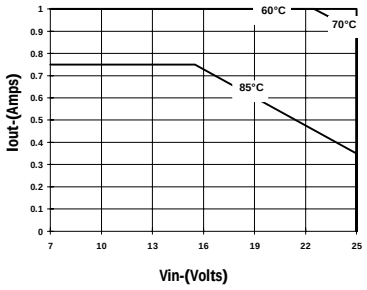
Efficiency vs Output Current



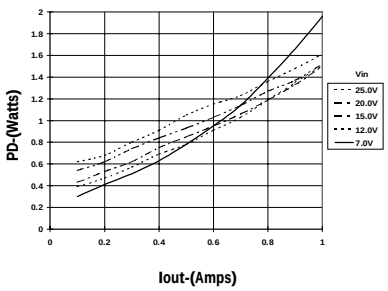
Ripple vs Output Current



Thermal Derating (T_a) (See Note B)

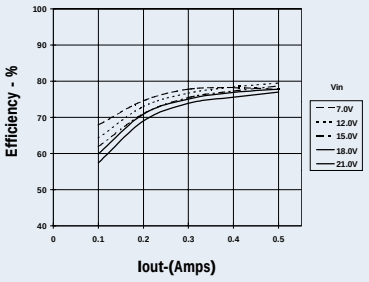


Power Dissipation vs Output Current

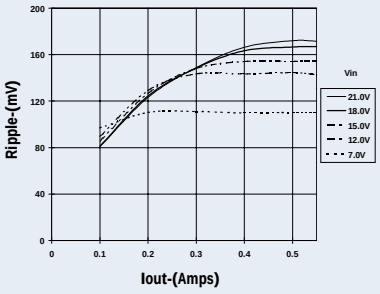


PT78NR109 -9.0 VDC (See Note A)

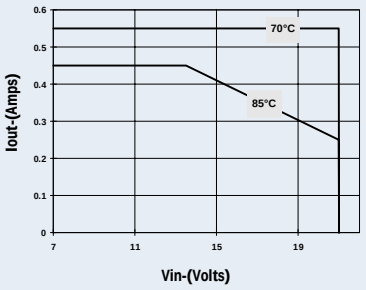
Efficiency vs Output Current



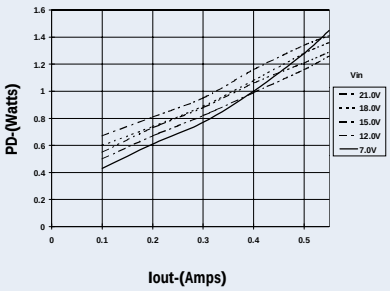
Ripple vs Output Current



Thermal Derating (T_a) (See Note B)

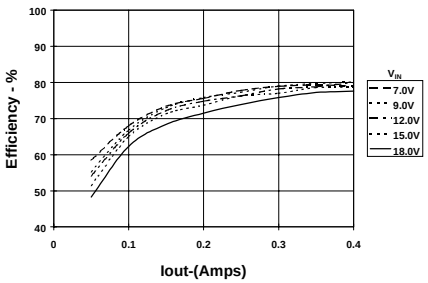


Power Dissipation vs Output Current

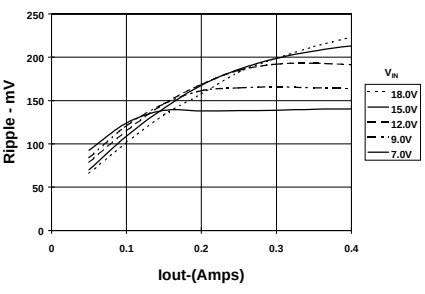


PT78NR112 -12.0 VDC (See Note A)

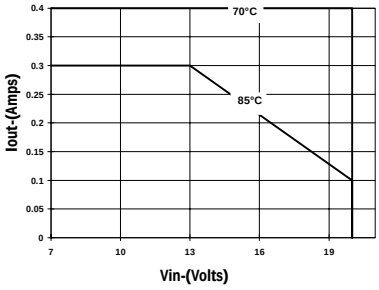
Efficiency vs Output Current



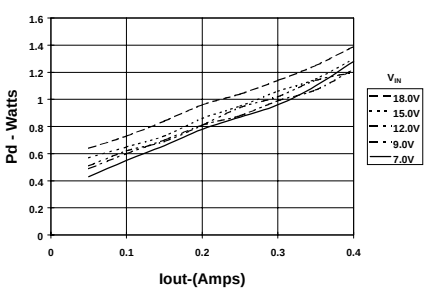
Ripple vs Output Current



Thermal Derating (T_a) (See Note B)



Power Dissipation vs Output Current



Note A: *All data listed in the above graphs, except for derating data, has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *Thermal derating graphs are developed in free air convection cooling of 40-60 LFM. (See Thermal Application Notes.)*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PT78NR103H	OBSOLETE	SIP MODULE	EFA	3		TBD	Call TI	Call TI	-40 to 85		
PT78NR103V	OBSOLETE	SIP MODULE	EFD	3		TBD	Call TI	Call TI	-40 to 85		
PT78NR106V	OBSOLETE	SIP MODULE	EFD	3		TBD	Call TI	Call TI			
PT78NR108ST	OBSOLETE	SIP MODULE	EFC	3		TBD	Call TI	Call TI			
PT78NR108V	OBSOLETE	SIP MODULE	EFD	3		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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