10-A, 4.5-V to 14-V INPUT, NON-ISOLATED POWER MODULE

FOR 3-GHz DSP SYSTEMS

FEATURES

- Up to 10-A Output Current
- 4.5-V to 14-V Input Voltage
- Wide-Output Voltage Adjust (0.69 V to 2.0 V)
- ±1.5% Total Output Voltage Variation
- Efficiencies up to 93%
- Output Overcurrent Protection (Nonlatching, Auto-Reset)
- Operating Temperature: –40°C to 85°C
- Safety Agency Approvals:
  - UL/IEC/CSA-C22.2 60950-1
- Prebias Startup
- On/Off Inhibit
- Differential Output Voltage Remote Sense
- Adjustable Undervoltage Lockout
- Auto-Track™ Sequencing
- SmartSync Technology
- POLA™ Compatible
- TurboTrans™ Technology
- Designed to meet Ultra-Fast Transient Requirements for 3-GHz DSP Systems
- 15 mV Output Voltage Deviation (C_O = 2000 μF, ΔI = 3 A)

APPLICATIONS

- Wireless Infrastructure Base Stations



DESCRIPTION

The PTH08T240F is a high-performance 10-A rated, non-isolated power module designed to meet ultra-fast transient requirements for 3-GHz DSP systems like Texas Instrument's TMS320TCI6488. This module is an addition to the 2nd generation of the popular PTH series power modules which include a reduced footprint and additional features.

Operating from an input voltage range of 4.5 V to 14 V, the PTH08T240F requires a single resistor to set the output voltage to any value over the range, 0.69 V to 2.0 V. The output voltage range makes the PTH08T240F particularly suitable for the 3-GHz DSP's core voltage requirements.

The module incorporates a comprehensive list of features. Output over-current and over-temperature shutdown protects against most load faults. A differential remote sense ensures tight load regulation. An adjustable under-voltage lockout allows the turn-on voltage threshold to be customized. Auto-Track™sequencing is a popular feature that greatly simplifies the simultaneous power-up and power-down of multiple modules in a power system.

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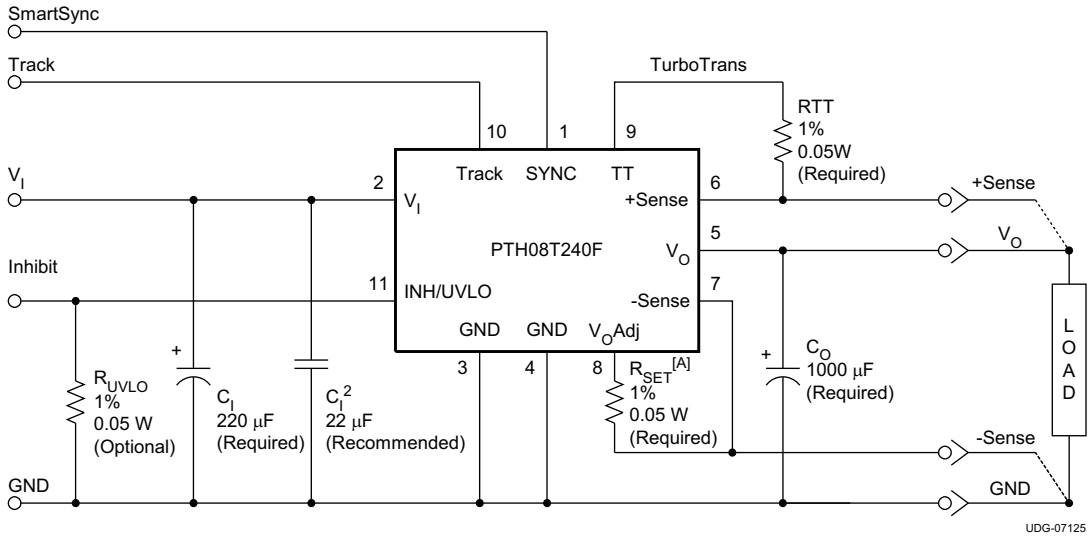
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The PTH08T240F includes new patented technologies, **TurboTrans™** and **SmartSync**. The TurboTrans feature optimizes the transient response of the regulator while simultaneously reducing the quantity of external output capacitors required to meet a target voltage deviation specification. TurboTrans allows PTH08T240F to meet the tight transient voltage tolerances required by 3-GHz DSPs with minimal output capacitance. SmartSync allows for switching frequency synchronization of multiple modules, thus simplifying EMI noise suppression tasks and reducing input capacitor RMS current requirements. The module uses double-sided surface mount construction to provide a low profile and compact footprint. Package options include both through-hole and surface mount configurations that are lead (Pb) - free and RoHS compatible.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



A. R_{SET} required to set the output voltage to a value higher than 0.69 V. See *Electrical Characteristics* table.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

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ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

					UNIT
V_{Track}	Track pin voltage			–0.3 to V_I + 0.3	V
T_A	Operating temperature range	Over V_I range		–40 to 85	°C
T_{wave}	Wave soldering temperature	Surface temperature of module body or pins **(5 seconds maximum)**	suffix AD	260	
T_{reflow}	Solder reflow temperature	Surface temperature of module body or pins	suffix AS	235 (1)	
			suffix AZ	260 (1)	
T_{stg}	Storage temperature	Storage temperature of module removed from shipping package		–55 to 125	
T_{pkg}	Packaging temperature	Shipping Tray or Tape and Reel storage or bake temperature		45	
	Mechanical shock	Per Mil-STD-883D, Method 2002.3 1 msec, 1/2 sine, mounted	suffix AD	500	G
			suffix AS & AZ	250	
	Mechanical vibration	Mil-STD-883D, Method 2007.2 20-2000 Hz		15	
	Weight			5	grams
	Flammability	Meets UL94V-O			

(1) During reflow of surface mount package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

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ELECTRICAL CHARACTERISTICS

PTH08T240F

T_A = 25°C, V_I = 5 V, V_O = 1.0 V, C_I = 220 µF, C_O = 1000 µF, and I_O = I_O max (unless otherwise stated)

PARAMETER		TEST CONDITIONS			PTH08T240F			UNIT
					MIN	TYP	MAX	
I_O	Output current	Over V_O range	25°C, natural convection		0		10	A
V_I	Input voltage range	Over I_O range		0.69V ≤ V_O < 1.3V	4.5		14 (1)	V
				1.3V ≤ V_O ≤ 2.0	4.5		14	
V_{OADJ}	Output voltage adjust range	Over I_O range			0.69		2.0	V
V_O	Set-point voltage tolerance					±0.5	±1 (2)	%V_O
	Temperature variation	–40°C < T_A < 85°C				±0.3		%V_O
	Line regulaltion	Over V_I range				±3		mV
	Load regulation	Over I_O range				±2		mV
	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C					±1.5 (2)	%V_O
η	Efficiency	I_O = 10 A	R_{SET} = 4.78 kΩ, V_O = 1.8 V			90%		
			R_{SET} = 7.09 kΩ, V_O = 1.5 V			88%		
			R_{SET} = 12.1 kΩ, V_O = 1.2 V			87%		
			R_{SET} = 20.8 kΩ, V_O = 1.0 V			85%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth				10 (1)		mV_{PP}
I_{LIM}	Overcurrent threshold	Reset, followed by auto-recovery				20		A
t_{tr}	Transient response	2.5 A/µs load step 0.5 A to 3.5 A step V_O = 0.9 V	C_O = 1000 µF, Type C R_{TT}=open	Recovery time		500		µs
ΔV_{tr}				V_O over/undershoot		25		mV
t_{trTT}			C_O = 2000 µF, Type C R_{TT}=24.3 = kΩ	Recovery time		800		µs
ΔV_{trTT}				V_O over/undershoot		14		mV
I_{IL}	Track input current (pin 10)	Pin to GND					–130 (3)	µA
dV_{track}/dt	Track slew rate capability	C_O ≤ C_O (max)					1	V/ms
$UVLO_{ADJ}$	Adjustable Under-voltage lockout (pin 11)	V_I increasing, R_{UVLO} = OPEN				4.3	4.45	V
		V_I decreasing, R_{UVLO} = OPEN			3.7	4.2		
		Hysteresis, R_{UVLO} ≤ 52.3 kΩ				0.5		
	Inhibit control (pin 11)	Input high voltage (V_{IH})					Open (4)	V
		Input low voltage (V_{IL})			-0.2		0.8	
		Input low current (I_{IL}), Pin 11 to GND				-235		µA
I_{in}	Input standby current	Inhibit (pin 11) to GND, Track (pin 10) open				5		mA
f_s	Switching frequency	Over V_I and I_O ranges, SmartSync (pin 1) to GND			260	300	340	kHz
f_{SYNC}	Synchronization frequency				240		400	kHz
V_{SYNCH}	SYNC High-Level Input Voltage				2		5.5	V
V_{SYNCL}	SYNC Low-Level Input Voltage						0.8	V
t_{SYNC}	SYNC Minimum Pulse Width				200			nSec
C_I	External input capacitance			Nonceramic	220 (5)			µF
				Ceramic		22 (5)		
C_O	External output capacitance	Capacitance Value		Nonceramic	1000 (6)		10000	µF
		Capacitance × ESR product (C_O × ESR)			1000		10000	µF×mΩ
MTBF	Reliability	Telcordia SR-332, 50% stress, T_A= 40°C, ground benign			6.1			10^6 Hr

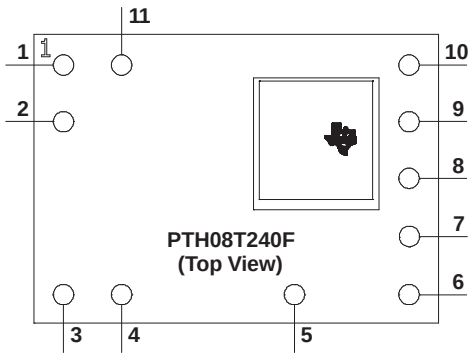
(1) For output voltages less than 1.3 V, the ripple may increase (up to 2×) when operating at input voltages greater than (V_O × 11). See the SmartSync section and the TurboTrans section of the datasheet for additional information.
(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
(3) A low-leakage (<100 nA), open-drain device, such as MOSFET or voltage supervisor IC, is recommended to control pin 10. The open-circuit voltage is less than 8 V_{dc}.
(4) This control pin has an internal pull-up. Do not place an external pull-up on this pin. If it is left open-circuit, the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET is recommended for control. For additional information, see the related application information section.
(5) A 220 µF electrolytic input capacitor is required for proper operation. The electrolytic capacitor must be rated for a minimum of 500 mA rms of ripple current. An additional 22-µF ceramic input capacitor is recommended to reduce rms ripple current.
(6) 1000 µF of external low-ESR output capacitance is required for basic operation. See the Capacitor Recommendation section and TurboTrans Application Information section for more guidance.

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TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	2	The positive input voltage power node to the module, which is referenced to common GND.
V_O	5	The regulated positive power output with respect to GND.
GND	3, 4	This is the common ground connection for the V_I and V_O power connections. It is also the 0 V_{dc} reference for the control inputs.
Inhibit(1) and UVLO	11	The Inhibit pin is an open-collector/drain, negative logic input that is referenced to GND. Applying a low level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied. This pin is also used for input undervoltage lockout (UVLO) programming. Connecting a resistor from this pin to GND (pin 3) allows the ON threshold of the UVLO to be adjusted higher than the default value. For more information, see the Application Information section.
V_o Adjust	8	A 0.05 W 1% resistor must be directly connected between this pin and pin 7 (–Sense) to set the output voltage to a value higher than 0.69 V. The temperature stability of the resistor should be 100 ppm/°C (or better). The setpoint range for the output voltage is from 0.69 V to 2.0 V. If left open circuit, the output voltage will default to its lowest value. For further information, on output voltage adjustment see the related application note. The specification table gives the preferred resistor values for a number of standard output voltages.
+ Sense	6	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy, +Sense must be connected to V_O, very close to the load.
– Sense	7	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy –Sense must be connected to GND (pin 4) very close to the module (within 10 cm).
Track	10	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the module's output voltage follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V_I. NOTE: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, see the related application note.
TurboTrans™	9	This input pin adjusts the transient response of the regulator. To activate the *TurboTrans*™ feature, a 1%, 50 mW resistor must be connected between this pin and pin 6 (+Sense) very close to the module. For a given value of output capacitance, a reduction in peak output voltage deviation is achieved by utililizing this feature. The resistance requirement can be selected from the TurboTrans™ resistor table in the Application Information section. External capacitance must never be connected to this pin unless the TurboTrans resistor value is a short, 0 Ω.
SmartSync	1	This input pin sychronizes the switching frequency of the module to an external clock frequency. The SmartSync feature can be used to sychronize the switching fequency of multiple PTH08T240F modules, aiding EMI noise suppression efforts. If unused, this pin should be connected to GND (pin 3). For more information, please review the Application Information section.

(1) Denotes negative logic: Open = Normal operation, Ground = Function active



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TYPICAL CHARACTERISTICS(1)(2)

CHARACTERISTIC DATA (V_I = 5 V)

EFFICIENCY VS LOAD CURRENT

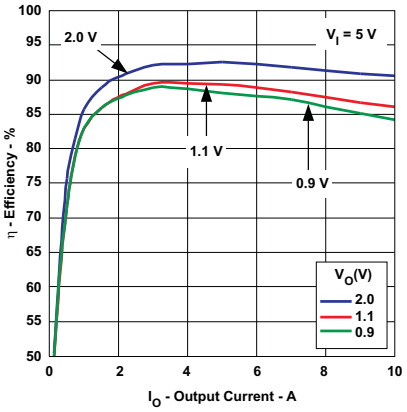


Figure 1.

OUTPUT RIPPLE VS LOAD CURRENT

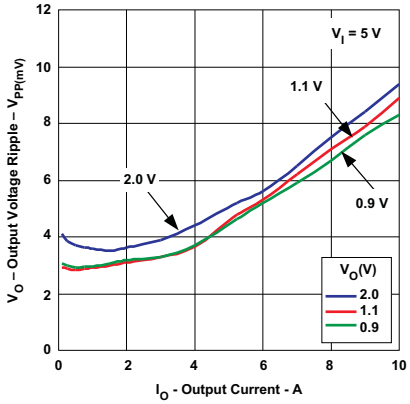


Figure 2.

POWER DISSIPATION VS LOAD CURRENT

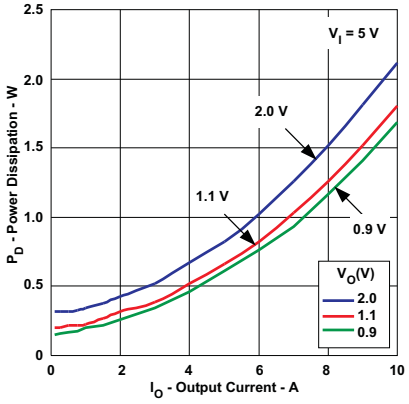


Figure 3.

SAFE OPERATING AREA

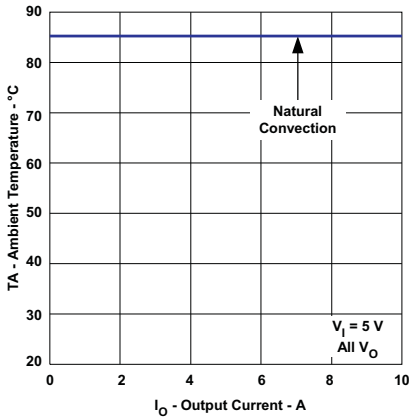


Figure 4.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias must be utilized. Please refer to the mechanical specification for more information. Applies to Figure 4.

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TYPICAL CHARACTERISTICS(1)(2)

CHARACTERISTIC DATA (V_I = 8 V)

EFFICIENCY VS LOAD CURRENT

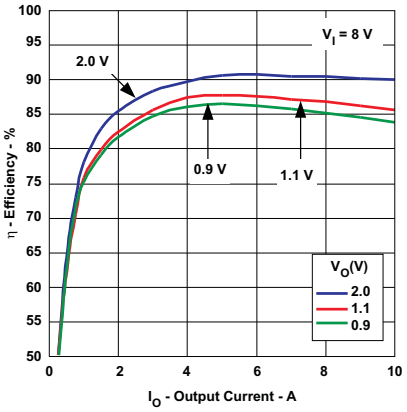


Figure 5.

OUTPUT RIPPLE VS LOAD CURRENT

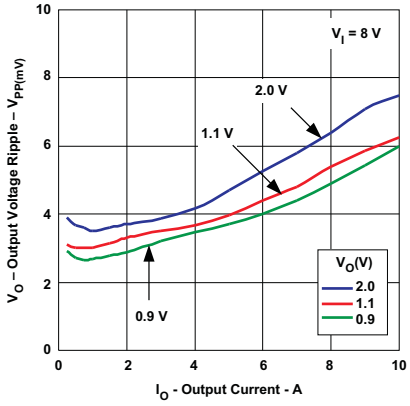


Figure 6.

POWER DISSIPATION VS LOAD CURRENT

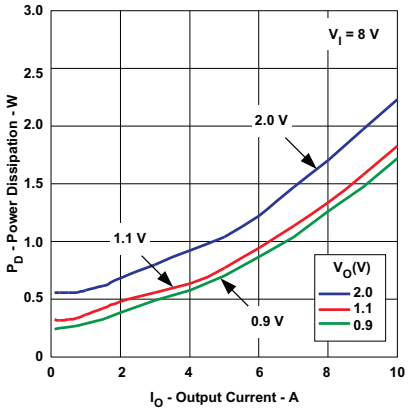


Figure 7.

SAFE OPERATING AREA

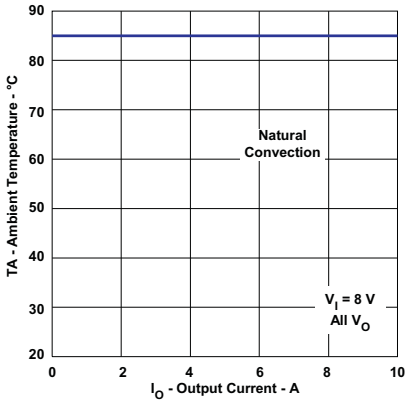


Figure 8.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 5, Figure 6, and Figure 7.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias must be utilized. Please refer to the mechanical specification for more information. Applies to Figure 8.

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TYPICAL CHARACTERISTICS(1)(2)(3)

CHARACTERISTIC DATA (V_I = 12 V)

EFFICIENCY VS OUTPUT CURRENT

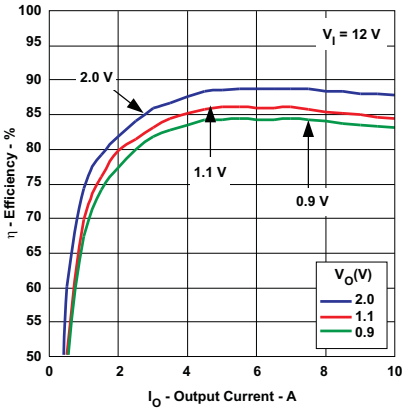


Figure 9.

OUTPUT RIPPLE VS OUTPUT CURRENT

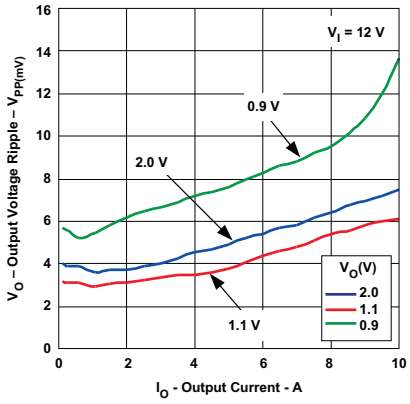


Figure 10. See Note 2 below

POWER DISSIPATION VS OUTPUT CURRENT

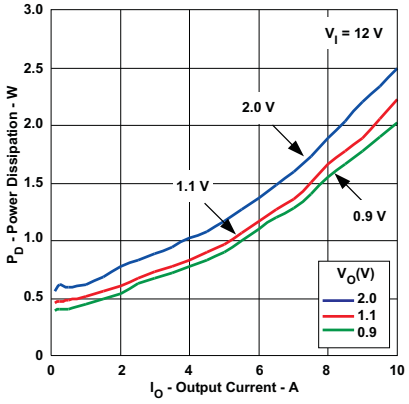


Figure 11.

SAFE OPERATING AREA

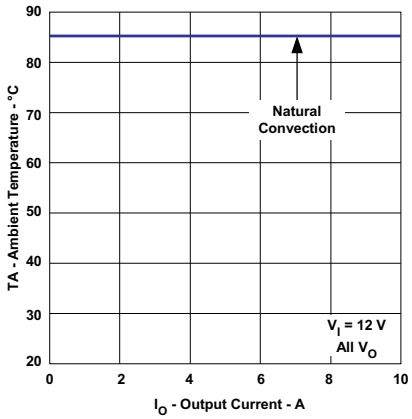


Figure 12.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to , Figure 9, Figure 11 and Figure 10.

(2) Output ripple may increase up to 2x when operating at input voltages greater than (V_O x 11). See the Smart Sync section of the datasheet for input voltage and frequency limitations.

(3) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias must be utilized. Please refer to the mechanical specification for more information. Applies to Figure 12.

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APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE

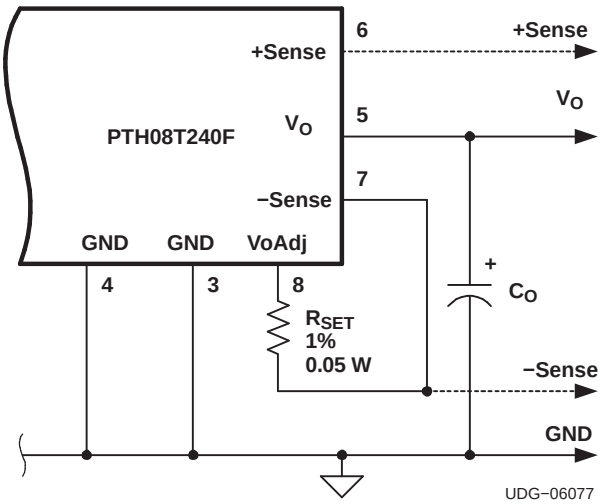
The V_OAdjust control (pin 8) sets the output voltage of the PTH08T240F. The adjustment range is 0.69 V to 2.0 V. The adjustment method requires the addition of a single external resistor, R_{SET}, that must be connected directly between the V_OAdjust and – Sense pins. Table 1 gives the standard value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 2. Figure 13 shows the placement of the required resistor.

$$R_{SET} = 10\ k\Omega \times \frac{0.69}{V_O - 0.69} - 1.43\ k\Omega \quad (1)$$

Table 1. Standard Values of R_{SET} for Standard Output Voltages

V_O (Standard) (V)	R_{SET} (Standard Value) (kΩ)	V_O (Actual) (V)
1.8	4.75	1.807
1.5	6.98	1.510
1.2	12.1	1.200
1.1	15.4	1.100
1	20.5	1.004
0.9	31.6	0.899



(1) **R_{SET}:** Use a 0.05-W resistor with a tolerance of 1% and temperature stability of 100 ppm/°C (or better). Connect the resistor directly between pins 8 and 7, as close to the regulator as possible, using dedicated PCB traces.

(2) Never connect capacitors to V_OAdjust (pin 8). Any capacitance added to the V_OAdjust pin affects the stability of the regulator.

Figure 13. V_O Adjust Resistor Placement

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Table 2. Output Voltage Set-Point Resistor Values (Standard Values)

V_O Required (V)	R_{SET} (kΩ)
0.70 (1)	681
0.75 (1)	113
0.80 (1)	61.9
0.85 (1)	41.2
0.90 (1)	31.6
0.95 (1)	24.9
1.00 (1)	20.5
1.05 (1)	17.8
1.10 (1)	15.4
1.15 (1)	13.3
1.20 (1)	12.1
1.25 (1)	10.7
1.30	9.88
1.35	9.09
1.40	8.25
1.45	7.68
1.50	6.98
1.55	6.49
1.60	6.04
1.65	5.76
1.70	5.36
1.75	5.11
1.80	4.75
1.85	4.53
1.90	4.22
1.95	4.02
2.00	3.83

(1) For output voltages less than 1.3 V, the ripple may increase (up to 2×) when operating at input voltages greater than (V_O × 11). See the SmartSync section and the TurboTrans section of the datasheet for more information.

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CAPACITOR RECOMMENDATIONS FOR THE PTH08T240F POWER MODULE

Capacitor Technologies

Electrolytic Capacitors

When using electrolytic capacitors, high quality, computer-grade electrolytic capacitors are recommended. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above -20°C. For operation below -20°C, tantalum, ceramic, or OS-CON type capacitors are required.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have very low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

Tantalum, Polymer-Tantalum Capacitors

Tantalum type capacitors may only used on the output bus, and are recommended for applications where the ambient operating temperature is less than 0°C. The AVX TPS series and Kemet capacitor series are suggested over many other tantalum types due to their lower ESR, higher rated surge, power dissipation, and ripple current capability. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

Input Capacitor (Required)

The PTH08T240F requires a minimum input capacitance of 220 µF electrolytic type. The ripple current rating of the electrolytic capacitor must be at least 500 mArms. An additional 22-µF X5R/X7R ceramic is recommended to reduce the RMS ripple current.

Input Capacitor Information

The size and value of the input capacitor is determined by the converter's transient performance capability. This minimum value assumes that the converter is supplied with a responsive, low inductance input source. This source should have ample capacitive decoupling, and be distributed to the converter via PCB power and ground planes.

Ceramic capacitors should be located as close as possible to the module's input pins, within 0.5 inch (1,3 cm). Adding ceramic capacitance is necessary to reduce the high-frequency ripple voltage at the module's input. This will reduce the magnitude of the ripple current through the electroytic capacitor, as well as the amount of ripple current reflected back to the input source. Additional ceramic capacitors can be added to further reduce the RMS ripple current requirement for the electrolytic capacitor.

Increasing the minimum input capacitance to 680 µF is recommended for high-performance applications, or wherever the input source performance is degraded.

The main considerations when selecting input capacitors are the RMS ripple current rating, temperature stability, and less than 100 mΩ of equivalent series resistance (ESR).

Regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of 2 × (maximum dc voltage + ac ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with a sufficient voltage rating to meet this requirement.

When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered.

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Output Capacitor (Required)

The PTH08T240F requires a minimum output capacitance of 1000 µF of aluminum, polymer-aluminum, tantulum, or polymer-tantalum type.

The required capacitance above the minimum is determined by actual transient deviation requirements. See the TurboTrans Technology application section within this document for specific capacitance selection.

Output Capacitor Information

When selecting output capacitors, the main considerations are capacitor type, temperature stability, and ESR. Consider the capacitance X ESR product (see the following section).

Ceramic output capacitors added for high-frequency bypassing should be located as close as possible to the load to be effective. Ceramic capacitor values below 10 µF should not be included when calculating the total output capacitance value.

When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered.

TurboTrans Output Capacitance

TurboTrans allows the designer to optimize the output capacitance according to the system transient design requirement. High quality, ultra-low ESR capacitors are required to maximize TurboTrans effectiveness. The capacitor's capacitance (µF) × ESR (mΩ) product determines its capacitor type; Type B, or C. Capacitor types are defined as follows:

Type B = (1000 < capacitance × ESR ≤ 5000) (e.g. polymer-tantalum)

Type C = (5000 < capacitance × ESR ≤ 10,000) (e.g. OS-CON)

When using more than one type of output capacitor, select the capacitor type that makes up the majority of your total output capacitance. When calculating the C×ESR product, use the maximum ESR value from the capacitor manufacturer's datasheet.

Working Examples:

A capacitor with a capacitance of 330 µF and an ESR of 5 mΩ, has a C × ESR product of 1650 µF x mΩ (330 µF × 5 mΩ). This is a Type B capacitor. A capacitor with a capacitance of 1000 µF and an ESR of 8 mΩ, has a C × ESR product of 8000 µF x mΩ (1000 µF × 8 mΩ). This is a Type C capacitor.

See the TurboTrans Technology application section within this document for specific capacitance selection.

Table 3 includes a preferred list of capacitors by type and vendor. See the Output Bus / TurboTrans column.

Designing for Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 2.5 A/µs. The typical voltage deviation for this load transient is given in the Electrical Characteristics table using the minimum required value of output capacitance. As the di/dt of a transient is increased, the response of a converter’s regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability.

If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional low ESR ceramic capacitor decoupling. Generally, with load steps greater than 100 A/µs, adding multiple 10 µF ceramic capacitors plus 10 × 1 µF, and numerous high frequency ceramics (≤ 0.1 µF) is all that is required to soften the transient higher frequency edges. The PCB location of these capacitors in relation to the load is critical. DSP, FPGA and ASIC vendors identify types, location and amount of capacitance required for optimum performance. Low impedance buses, unbroken PCB copper planes, and components located as close as possible to the high frequency devices are essential for optimizing transient performance.

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Table 3. Input/Output Capacitors(1)

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity		
	Working Voltage (V)	Value (µF)	Max ESR at 100 kHz (mΩ)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Output Bus: TurboTrans Cap Type(2)	Vendor Part No.
Panasonic								
FC (Radial)	25	270	90	755	10 × 12,5	≥1(3)	N/R(4)	EEUFC1E271
FC (Radial)	25	560	65	1205	12,5 × 15	≥1(3)	N/R(4)	EEUFC1E561S
FC(SMD)	25	470	65	1200	12,5 × 16,5	≥1(3)	N/R(4)	EEVFC1E471LQ
FK(SMD)	25	470	80	850	10 ×10,2	≥1(3)	N/R(4)	EEVFK1E471P
United Chemi-Con								
PTB(SMD) Poly-Tantalum	6.3	330	25	2600	7,3x4,3x2.8	N/R(5)	C ≥ 3(2)	4PTB337MD6TER
LXZ, Aluminum (Radial)	25	330	90	760	10 × 12,5	≥1(3)	N/R(4)	LXZ25VB331M10X12LL
PS, Poly-Alum(Radial)	16	330	14	5060	10 × 12,5	≥1(3)	B ≥ 3(2)	16PS330MJ12
PXA, Poly-Alum(SMD)	16	330	14	5050	10 × 12,2	≥1(3)	B ≥ 3(2)	PXA16VC331MJ12TP
PS, Poly-Alum(Radial)	10	270	14	4420	8 × 11,5	≥1(3)	B ≥ 4(2)	10PS270MH11
PXA, Poly-Alum(Radial)	10	330	14	4420	8 × 12	≥1(3)	B ≥ 3(2)	PXA10VC331MH12
Nichicon, Aluminum								
HD (Radial)	25	220	72	760	8 × 11,5	≥1(3)	N/R(4)	UHD1E221MPR
PM (Radial)	25	330	95	750	10 × 15	≥1(3)	N/R(4)	UPM1E331MPH6
PM (Radial)	35	560	48	1360	16 × 15	≥1(3)	N/R(4)	UPM1V561MHH6
Panasonic, Poly-Aluminum	2.0	390	5	4000	7,3×4,3×4,2	N/R(5)	B ≥ 3(2)	EEFSE0J391R (V_O≤ 1.6V)(6)
Sanyo								
TPE, Poscap (SMD)	10	330	25	3000	7,3 × 4,3	≥1(3)	C ≥ 3(2)	10TPE330MF (V_I ≤ 8V)
TPE Poscap(SMD)	2.5	470	7	4400	7,3 × 4,3	N/R(5)	B ≥ 2(2)	2R5TPE470M7
TPD Poscap (SMD)	2.5	1000	5	6100	7,3 × 4,3	N/R(5)	B ≥ 1(2)	2R5TPD1000M5
SEP, OS-CON (Radial)	16	330	16	4700	10 ×13	≥1(3)	B ≥ 3(2)	16SEP330M
SP OS-CON (Radial)	16	270	18	4400	10 × 11,5	≥1(3)	B ≥ 4(2)	16SP270M
SEPC, OS-CON (Radial)	16	270	11	5000	8 × 13	≥1(3)	B ≥ 4(2)	16SEPC270M
SVP, OS-CON (SMD)	16	330	16	4700	10 × 12,6	≥1(3)	B ≥ 3(2)(7)	16SVP330M

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products.
RoHS, Lead-free and Material Details
See the capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.
(2) Required capacitors with TurboTrans. See the TurboTrans Application information for Capacitor Selection
Capacitor Types:
a. Type B = (1,000 < capacitance × ESR ≤ 5,000)
b. Type C = (5,000 < capacitance × ESR ≤ 10,000)
(3) In addition to the required input electrolytic capacitance, ≥ 22 µF of ceramic capacitance is recommended to reduce the high-frequency reflected ripple current.
(4) Aluminum Electrolytic capacitor not recommended for the TurboTrans due to higher capacitance × ESR products. Aluminum and higher ESR capacitors can be used in conjunction with lower ESR capacitance.
(5) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.
(6) The voltage rating of this capacitor only allows it to be used for output voltage that is equal to or less than 80% of the working voltage.
(7) Total bulk nonceramic capacitors on the output bus with ESR of ≥ 15mΩ to ≤ 30mΩ requires an additional ≥ 200 µF of ceramic capacitance.

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Table 3. Input/Output Capacitors (continued)

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity		
	Working Voltage (V)	Value (µF)	Max ESR at 100 kHz (mΩ)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Output Bus: TurboTrans Cap Type(2)	Vendor Part No.
Kemet, Poly-Tantalum								
T520 (SMD)	10	330	25	2600	7,3×4,3×4,1	≥1(8)	C ≥ 3(9)	T520X337M010ASE025 (V_I ≤ 8V)
T530 (SMD)	6.3	330	15	3800	7,3×4,3×4,1	N/R(10)	B ≥ 3(9)	T530X337M006ASE015
T530 (SMD)	4	680	5	7300	7,3×4,3×4,1	N/R(10)	B ≥ 2(9)	T530X687M004ASE005
T530 (SMD)	2.5	1000	5	7300	7,3 × 4,3	N/R(10)	B ≥ 1(9)	T530X108M2R5ASE005
Vishay-Sprague								
597D, Tantalum (SMD)	16	220	40	2300	7,2×5,7×4,1	≥1(8)	C ≥ 5(11)(9)	597D227X16E2T
94SP, OS-CON (Radial)	16	270	18	4400	10 × 10,5	≥1(8)	B ≥ 4(9)	94SP277X0016FBP
94SVP OS-CON(SMD)	16	330	17	4500	10 × 12,7	≥1(8)	B ≥ 3(9)	94SVP337X016F12
Kemet, Ceramic X5R (SMD)	16	10	2	–	3225	≥2(8)	N/R	C1210C106M4PAC
Murata, Ceramic X5R	25	22	2	–	3225	≥1(8)	N/R	GRM32ER61E226K
(SMD)	16	10				≥2(8)	N/R	GRM32DR61C106K
TDK, Ceramic X5R	16	10	2	–	3225	≥2(8)	N/R	C3225X5R1C106MT0
(SMD)	16	22				≥1(8)	N/R	C3225X5R1C226MT

(8) In addition to the required input electrolytic capacitance, ≥ 22 µF of ceramic capacitance is recommended to reduce the high-frequency reflected ripple current.
(9) Required capacitors with TurboTrans. See the TurboTrans Application information for Capacitor Selection
Capacitor Types:
a. Type B = (1,000 < capacitance × ESR ≤ 5,000)
b. Type C = (5,000 < capacitance × ESR ≤ 10,000)
(10) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.
(11) Total bulk nonceramic capacitors on the output bus with ESR of ≥ 15mΩ to ≤ 30mΩ requires an additional ≥ 200 µF of ceramic capacitance.

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TurboTrans™ Technology

TurboTrans technology is a feature introduced in the T2 generation of the PTH/PTV family of power modules. TurboTrans optimizes the transient response of the regulator with added external capacitance using a single external resistor. Benefits of this technology include reduced output capacitance, minimized output voltage deviation following a load transient, and enhanced stability when using ultra-low ESR output capacitors. The amount of output capacitance required to meet a target output voltage deviation is reduced with TurboTrans activated. Likewise, for a given amount of output capacitance, the amplitude of the voltage deviation following a load transient is reduced. Applications requiring tight transient voltage tolerances and minimized capacitor footprint area benefits greatly from this technology.

TurboTrans™ Selection

Utilizing TurboTrans requires connecting a resistor, R_{TT}, between the +Sense pin (pin 6) and the TurboTrans pin (pin 9). The value of the resistor directly corresponds to the amount of output capacitance required. All T2 products require a minimum value of output capacitance. For the PTH08T240F, the minimum required capacitance is 1000 µF. Capacitors with a capacitance × ESR product above 1000 µF×mΩ and below 10,000 µF×mΩ are required. (Multiply the capacitance (in µF) by the ESR (in mΩ) to determine the capacitance × ESR product.) See the *Capacitor Selection* section of the datasheet for a variety of capacitors that meet this criteria.

Figure 14 thru Figure 21 show the amount of output capacitance required to meet a desired transient voltage deviation for Type B (e.g. polymer-tantalum) and Type C (e.g. OS-CON) capacitors. To calculate the proper value of R_{TT}, first determine your required transient voltage deviation limits and magnitude of your transient load step. Next, determine what type of output capacitors are used. (If more than one type of output capacitor is used, select the capacitor type that makes up the majority of your total output capacitance.) Knowing this information, use the chart (Figure 14 thru Figure 21) that corresponds to the capacitor type selected. To use the chart, begin by dividing the maximum voltage deviation limit (in mV) by the magnitude of your load step (in Amps). This gives a mV/A value. Find this value on the Y-axis of the appropriate chart. Read across the graph to the *'TurboTrans'* plot. From this point, read down to the X-axis which lists the minimum required capacitance, C_O, to meet that transient voltage deviation. The required R_{TT} resistor value can then be calculated using the equation or selected from the TurboTrans table. The TurboTrans tables include both the required output capacitance and the corresponding R_{TT} values to meet several values of transient voltage deviation for 25% (2.5 A), 50% (5 A), and 75% (7.5 A) output load steps.

The chart can also be used to determine the achievable transient voltage deviation for a given amount of output capacitance. By selecting the amount of output capacitance along the X-axis, reading up to the desired *'TurboTrans"* curve, and then over to the Y-axis, gives the transient voltage deviation limit for that value of output capacitance. The required R_{TT} resistor value can be calculated using the equation or selected from the TurboTrans table.

As an example, let's look at a 5-V application requiring a 15-mV deviation during a 3-A load transient. A majority of 680-µF, 10-mΩ ouput capacitors will be used. (680 (in µF) × 10 (in mΩ) = 6,800; therefore this is Type C capacitance). Use the 5-V, Type C capacitor chart, Figure 19. Dividing 15 mV by 3 A gives 5 mV/A transient voltage deviation per amp of transient load step. Select 5 mV/A on the Y-axis and read across to the *'TurboTrans"* plot. Following this point down to the X-axis gives a minimum required output capacitance of approximately 1800 µF. The required R_{TT} resistor value for 1800 µF can then be calculated or selected from Table 4. The required R_{TT} resistor is approximately 32.0 kΩ.

Applications operating from an input bus greater than 8 V may encounter reduced transient performance when the output voltage is less than $V_I/11$. Additional output capacitance may be required in order to achieve the expected transient performance. See Figure 17 and Figure 21 when operating at an increased V_I to V_O ratio.

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PTH08T240F Type B Capacitors

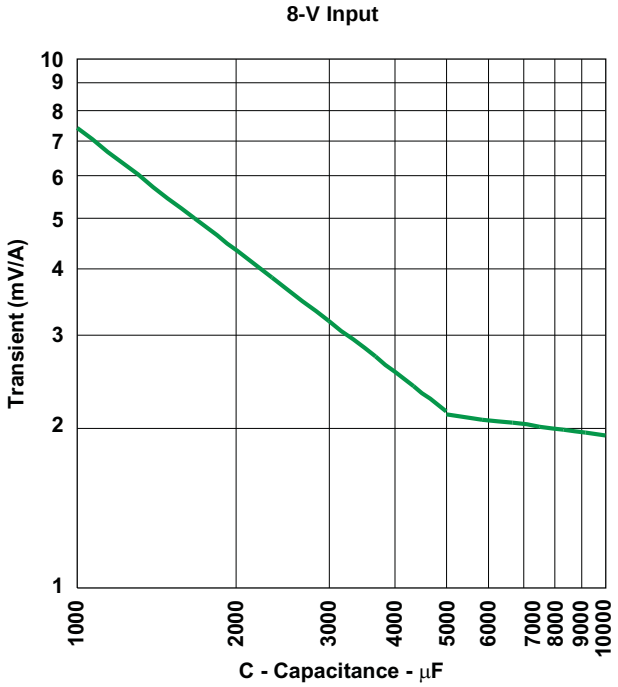


Figure 14. Capacitor Type B, 1000 < C(µF)×ESR(mΩ) ≤ 5000 (e.g. Polymer-Tantalum)

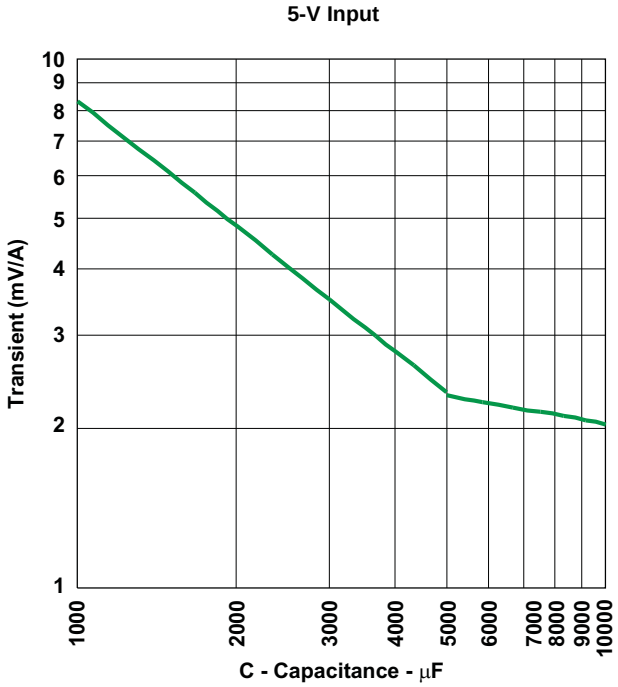


Figure 15. Capacitor Type B, 1000 < C(µF)×ESR(mΩ) ≤ 5000 (e.g. Polymer-Tantalum)

Table 4. Type B TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			8-V Input		5-V Input	
25% load step (2.5 A)	50% load step (5 A)	75% load step (7.5 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
20	40	60	1000	open	1060	576
18	36	54	1040	866	1200	147
16	32	48	1200	147	1400	71.5
14	28	42	1440	64.9	1660	40.2
12	24	36	1760	34.0	2020	23.2
10	20	30	2230	18.2	2550	12.7
8	16	24	3000	8.06	3400	5.36
6	12	18	4350	1.54	4900	0.205

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming, see Equation 2.

$$R_{TT} = \frac{40 \times \left[1 - \left(C_O / 5000\right)\right]}{\left[\left(C_O / 1000\right) - 1\right]} \left(k\Omega\right) \quad (2)$$

Where C_O is the total output capacitance in µF. C_O values greater than or equal to 5000 µF require R_{TT} to be a short, 0 Ω. (R_{TT} results in a negative value when C_O > 5000 µF).

To ensure stability, the value of R_{TT} must be calculated using the minimum required output capacitance determined from the capacitor transient response charts above.

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PTH08T240F Type B Capacitors (12-V)

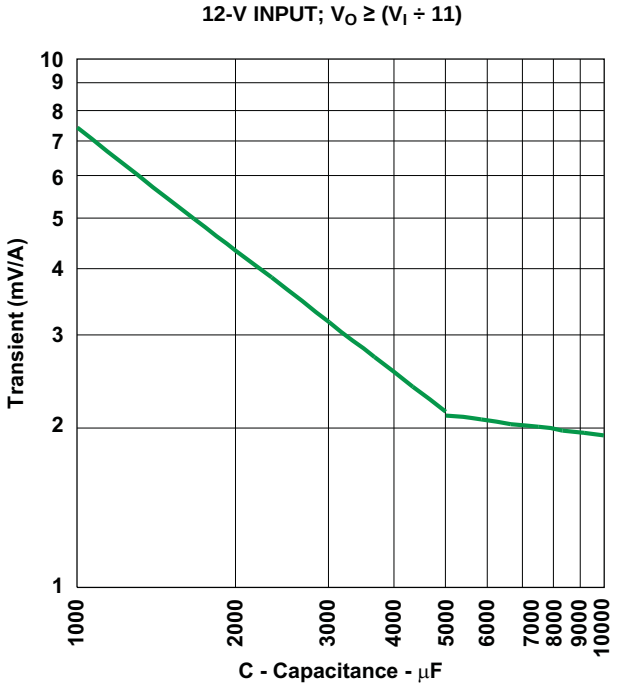


Figure 16. ($V_O \geq V_I \div 11$) Capacitor Type B

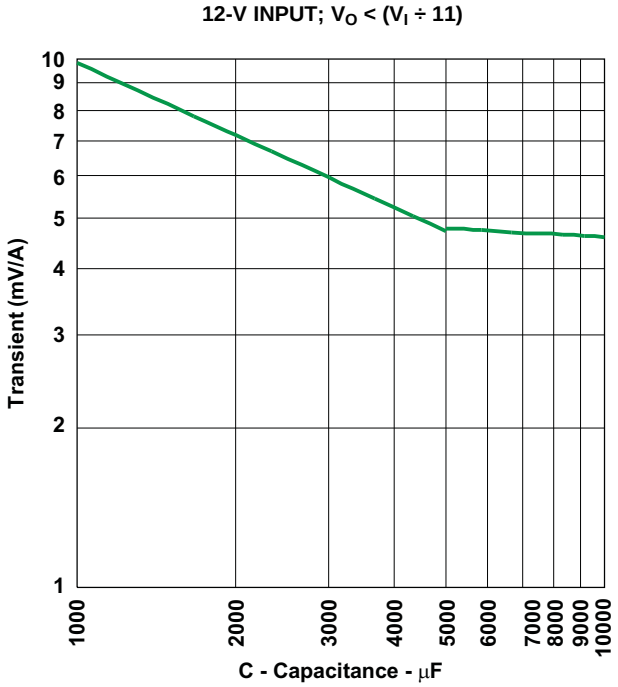


Figure 17. $V_O < (V_I \div 11)$ Capacitor Type B

Table 5. Type B TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			$V_O \geq V_I/11$		$V_O < V_I/11$	
25% load step (2.5 A)	50% load step (5 A)	75% load step (7.5 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
25	50	75	1000	open	1000	open
20	40	60	1000	open	1600	46.4
18	36	54	1050	634	2000	23.7
15	30	45	1300	97.6	3000	8.06
12	24	36	1760	34.0	4900	0.255
10	20	30	2250	17.4	exceeds max	-
8	16	24	3000	8.06	exceeds max	-
5	10	15	7900	short	exceeds max	-

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming, see Equation 3.

$$R_{TT} = \frac{40 \times \left[1 - (C_O/5000)\right]}{\left[(C_O/1000) - 1\right]} \ (k\Omega) \quad (3)$$

Where C_O is the total output capacitance in µF. C_O values greater than or equal to 5000 µF require R_{TT} to be a short, 0 Ω. (R_{TT} results in a negative value when C_O > 5000 µF).

To ensure stability, the value of R_{TT} must be calculated using the minimum required output capacitance determined from the capacitor transient response charts above.

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PTH08T240F Type C Capacitors

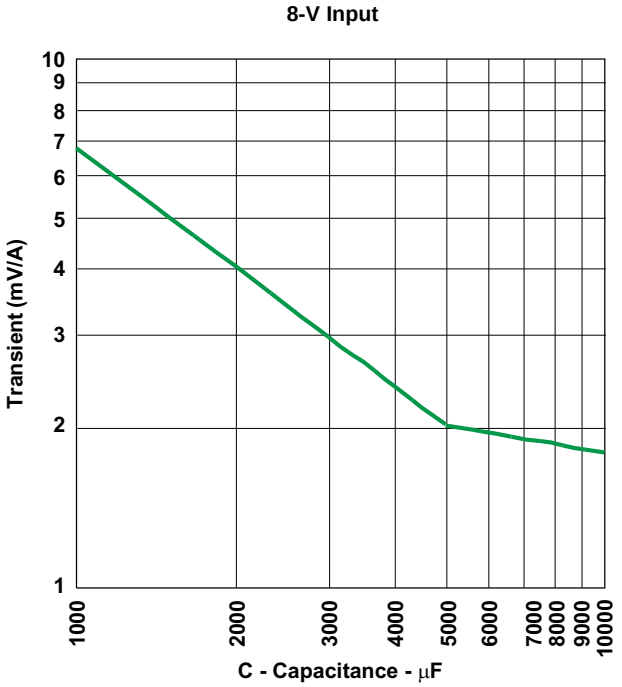


Figure 18. Capacitor Type C, 5000 < C(µF)×ESR(mΩ) ≤ 10,000 (e.g. OS-CON)

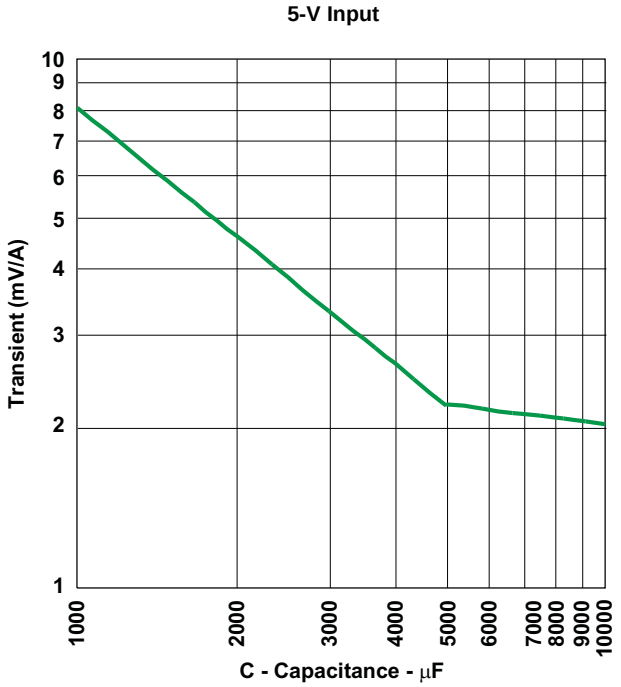


Figure 19. Capacitor Type C, 5000 < C(µF)×ESR(mΩ) ≤ 10,000 (e.g. OS-CON)

Table 6. Type C TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			8-V Input		5-V Input	
25% load step (2.5 A)	50% load step (5 A)	75% load step (7.5 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
20	40	60	1000	open	1040	787
18	36	54	1000	open	1180	169
16	32	48	1100	340	1350	82.5
14	28	42	1300	97.6	1600	45.3
12	24	36	1600	45.3	1930	26.7
10	20	30	2050	22.6	2420	14.7
8	16	24	2750	10.5	3200	6.49
6	12	18	4050	2.49	4560	1.0

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming, see Equation 4 .

$$R_{TT} = \frac{40 \times \left[1 - \left(C_O / 5000\right)\right]}{\left[\left(C_O / 1000\right) - 1\right]} \left(k\Omega\right) \quad (4)$$

Where C_O is the total output capacitance in µF. C_O values greater than or equal to 5000 µF require R_{TT} to be a short, 0 Ω. (R_{TT} results in a negative value when C_O > 5000 µF).

To ensure stability, the value of R_{TT} must be calculated using the minimum required output capacitance determined from the capacitor transient response charts above.

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PTH08T240F Type C Capacitors (12-V)

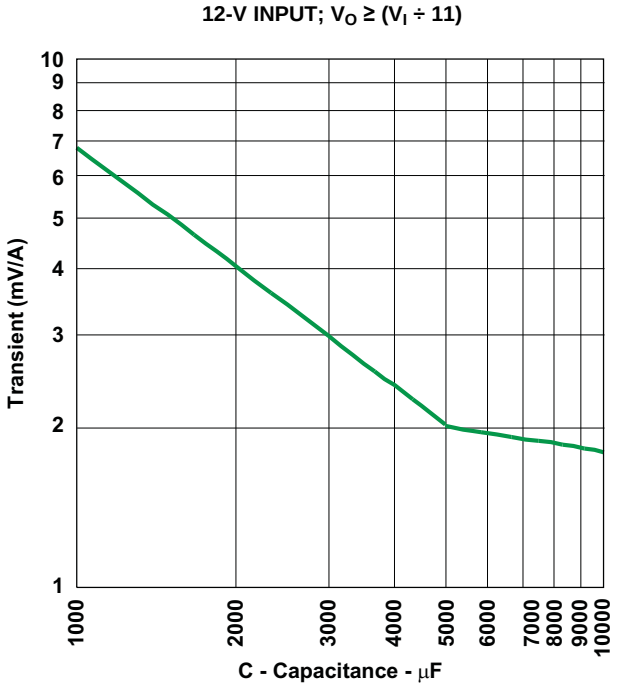


Figure 20. $V_O \geq (V_I \div 11)$ Capacitor Type C

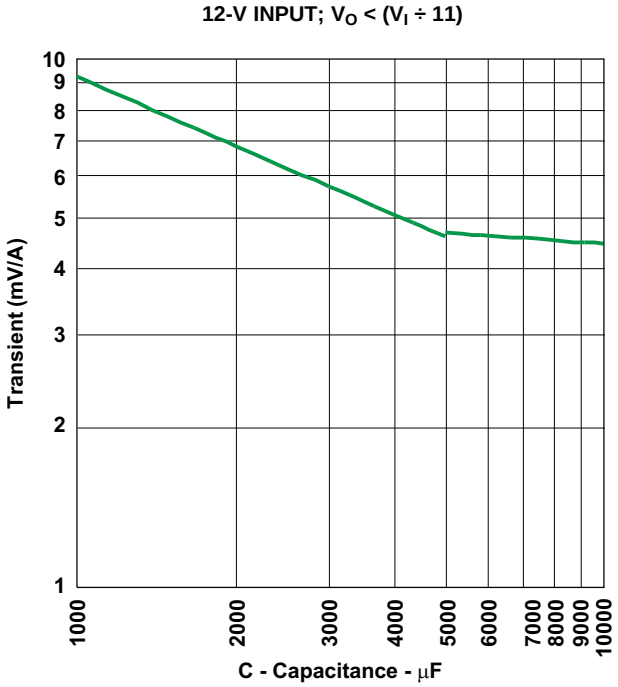


Figure 21. $V_O < (V_I \div 11)$ Capacitor Type C

Table 7. Type C TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			$V_O \geq V_I/11$		$V_O < V_I/11$	
25% load step (2.5 A)	50% load step (5 A)	75% load step (7.5 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
25	50	75	1000	open	1000	open
20	40	60	1000	open	1450	63.4
18	36	54	1000	open	1850	29.4
15	30	45	1200	150	2800	9.76
12	24	36	1600	45.3	4600	0.887
10	20	30	2050	22.6	exceeds max	-
8	16	24	2750	10.2	exceeds max	-
5	10	15	5400	short	exceeds max	-

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming, see Equation 5.

$$R_{TT} = \frac{40 \times \left[1 - (C_O/5000)\right]}{\left[(C_O/1000) - 1\right]} \ (k\Omega) \quad (5)$$

Where C_O is the total output capacitance in µF. C_O values greater than or equal to 5000 µF require R_{TT} to be a short, 0 Ω. (R_{TT} results in a negative value when C_O > 5000 µF).

To ensure stability, the value of R_{TT} must be calculated using the minimum required output capacitance determined from the capacitor transient response charts above.

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Application Diagram and Waveforms

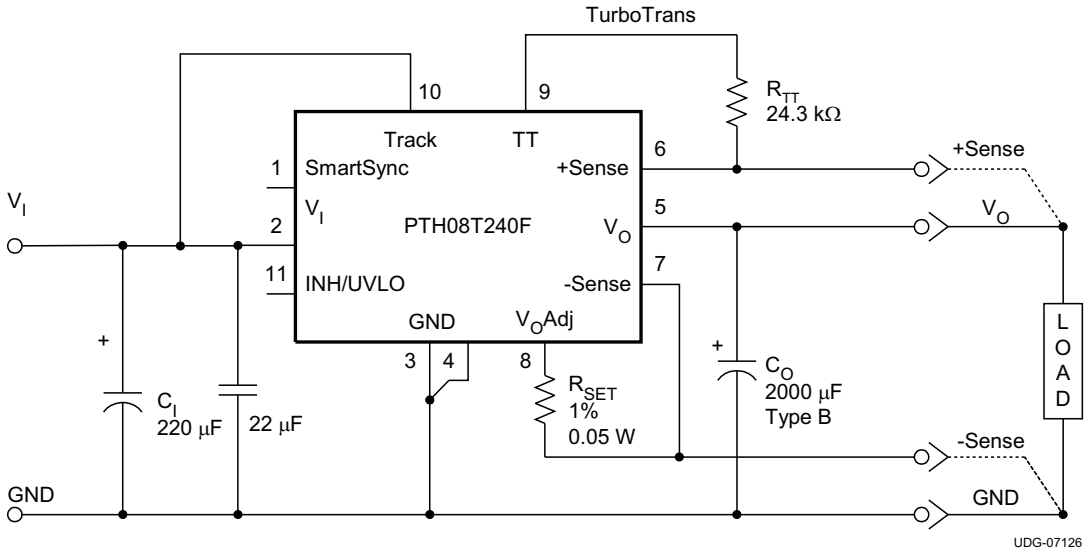


Figure 22. Typical TMS320TCI6488 Application

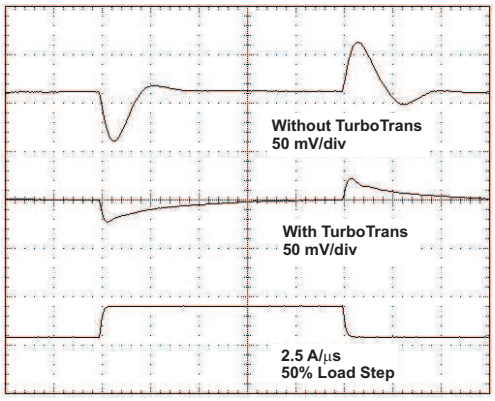


Figure 23. Typical TurboTrans Waveforms (5-V Input)

UNDERVOLTAGE LOCKOUT (UVLO)

The PTH08T240F power modules incorporate an input undervoltage lockout (UVLO). The UVLO feature prevents the operation of the module until there is sufficient input voltage to produce a valid output voltage. This enables the module to provide a clean, monotonic powerup for the load circuit, and also limits the magnitude of current drawn from the regulator's input source during the power-up sequence.

The UVLO characteristic is defined by the ON threshold (V_{THD}) voltage. Below the *ON* threshold, the Inhibit control is overridden, and the module does not produce an output. The hysteresis voltage, which is the difference between the *ON* and *OFF* threshold voltages, is set at 500 mV. The hysteresis prevents start-up oscillations, which can occur if the input voltage droops slightly when the module begins drawing current from the input source.

The UVLO feature of the PTH08T240F module allows for limited adjustment of the *ON* threshold voltage. The adjustment is made via the *Inhbit/UVLO Prog* control pin (pin 11) using a single resistor (see Figure 24). When pin 11 is left open circuit, the *ON* threshold voltage is internally set to its default value, which is 4.3 V. The *ON* threshold might need to be raised if the module is powered from a tightly regulated 12-V bus. Adjusting the threshold prevents the module from operating if the input bus fails to completely rise to its specified regulation voltage.

Equation 6 determines the value of R_{UVLO} required to adjust V_{THD} to a new value. The default value is 4.3 V, and it may only be adjusted to a higher value.

$$R_{UVLO} = \frac{9690 - \left(137 \times V_I\right)}{\left(137 \times V_I\right) - 585} \ (k\Omega) \tag{6}$$

Table 8 shows a chart of standard resistor values for R_{UVLO} for different options of the on-threshold (V_{THD}) voltage.

Table 8. Standard R_{UVLO} values for Various V_{THD} values

V_{THD} (V)	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5
R_{UVLO} (kΩ)	88.7	52.3	37.4	28.7	23.2	19.6	16.9	14.7

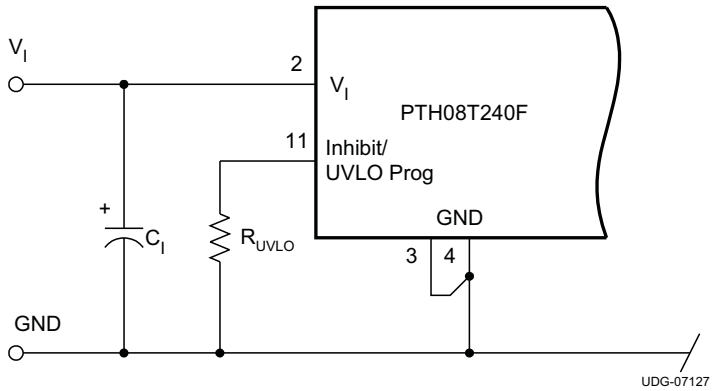


Figure 24. Undervoltage Lockout Adjustment Resistor Placement

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Soft-Start Power Up

The Auto-Track feature allows the power-up of multiple PTH/PTV modules to be directly controlled from the Track pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the Track pin should be directly connected to the input voltage, V_I (see Figure 25).

When the Track pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically between 5 ms and 15 ms) before allowing the output voltage to rise.

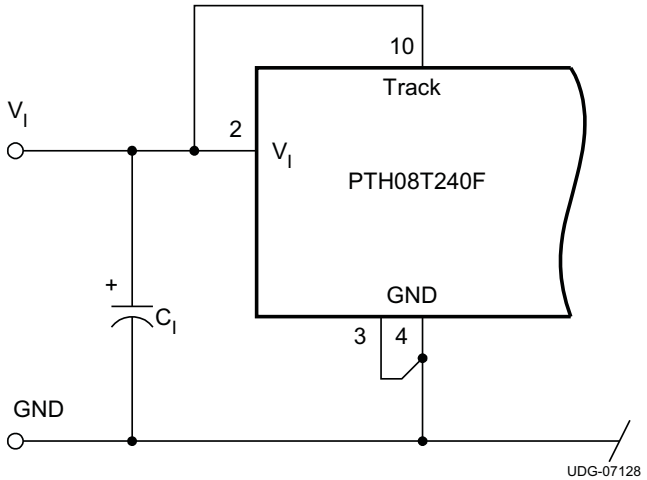


Figure 25. Defeating the Auto-Track Function

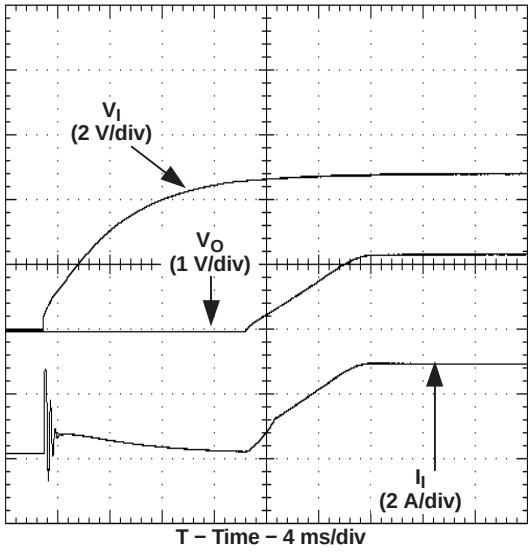


Figure 26. Power-Up Waveform

The output then progressively rises to the module's setpoint voltage. Figure 26 shows the soft-start power-up characteristic of the PTH08T240F operating from a 5-V input bus and configured for a 1.1-V output. The waveforms were measured with a 10-A constant current load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 30 ms.

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On/Off Inhibit

For applications requiring output voltage on/off control, the PTH08T240F incorporates an Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND.

Figure 27 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit input has its own internal pull-up. An external pull-up resistor should never be used with the inhibit pin. The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

Turning Q1 on applies a low voltage to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 15 ms. Figure 28 shows the typical rise in both the output voltage and input current, following the turn-off of Q1. The turn off of Q1 corresponds to the rise in the waveform, V_{INH}. The waveforms were measured with a 10-A constant current load.

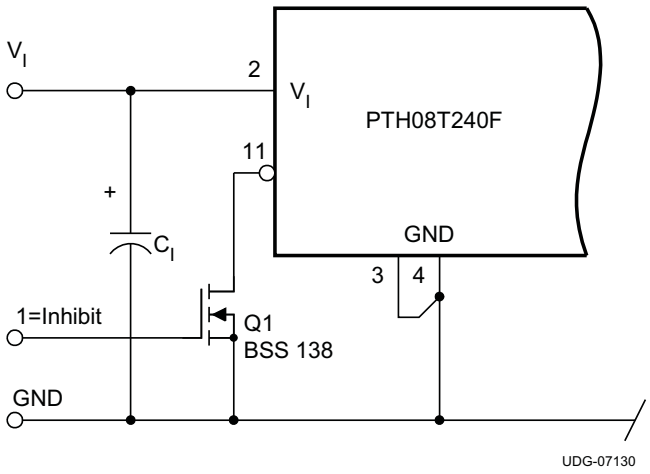


Figure 27. On/Off Inhibit Control Circuit

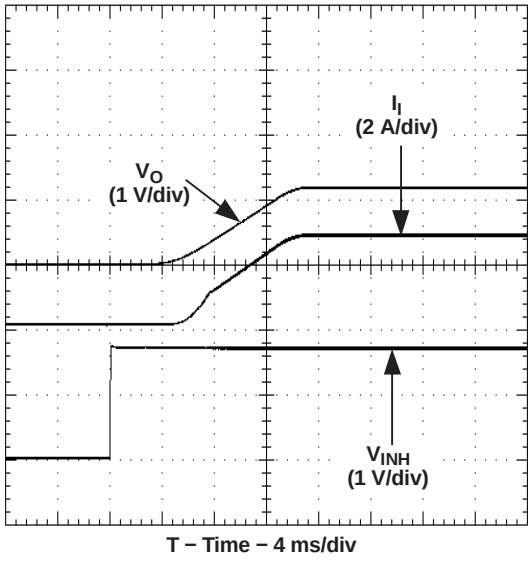


Figure 28. Power-Up Response from Inhibit Control

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Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up. This is described as a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Overtemperature Protection (OTP)

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's Inhibit control is internally pulled low. This turns the output off. The output voltage drops as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the sensed temperature decreases by about 10°C below the trip point.

The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and reduces the long-term reliability of the module. Always operate the regulator within the specified safe operating area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Differential Output Voltage Remote Sense

Differential remote sense improves the load regulation performance of the module by allowing it to compensate for any IR voltage drop between its output and the load in either the positive or return path. An IR drop is caused by the output current flowing through the small amount of pin and trace resistance. With the sense pins connected, the difference between the voltage measured directly between the V_O and GND pins, and that measured at the Sense pins, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V. Connecting the +Sense (pin 6) to the positive load terminal improves the load regulation at the connection point. For optimal behavior the –Sense (pin 7) must be connected to GND (pin 4) close to the module (within 10 cm).

If the remote sense feature is not used at the load, connect the +Sense pin to V_O (pin 5) and connect the –Sense pin to the module GND (pin 4).

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

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Smart Sync

Smart Sync is a feature that allows multiple power modules to be synchronized to a common frequency. Driving the Smart Sync pins with an external oscillator set to the desired frequency, synchronizes all connected modules to the selected frequency. The synchronization frequency can be higher or lower than the nominal switching frequency of the modules within the range between 240 kHz and 400 kHz (see *Electrical Specifications* table for frequency limits). Synchronizing modules powered from the same bus, eliminates beat frequencies reflected back to the input supply, and also reduces EMI filtering requirements. Eliminating the low beat frequencies (usually < 10 kHz) allows the EMI filter to be designed to attenuate only the synchronization frequency. Power modules can also be synchronized out of phase to minimize source current loading and minimize input capacitance requirements. If unused, connect the Smart Sync pin to GND (pin 3). Figure 29 shows a standard circuit with two modules syncronized 180° out-of-phase using a D flip-flop.

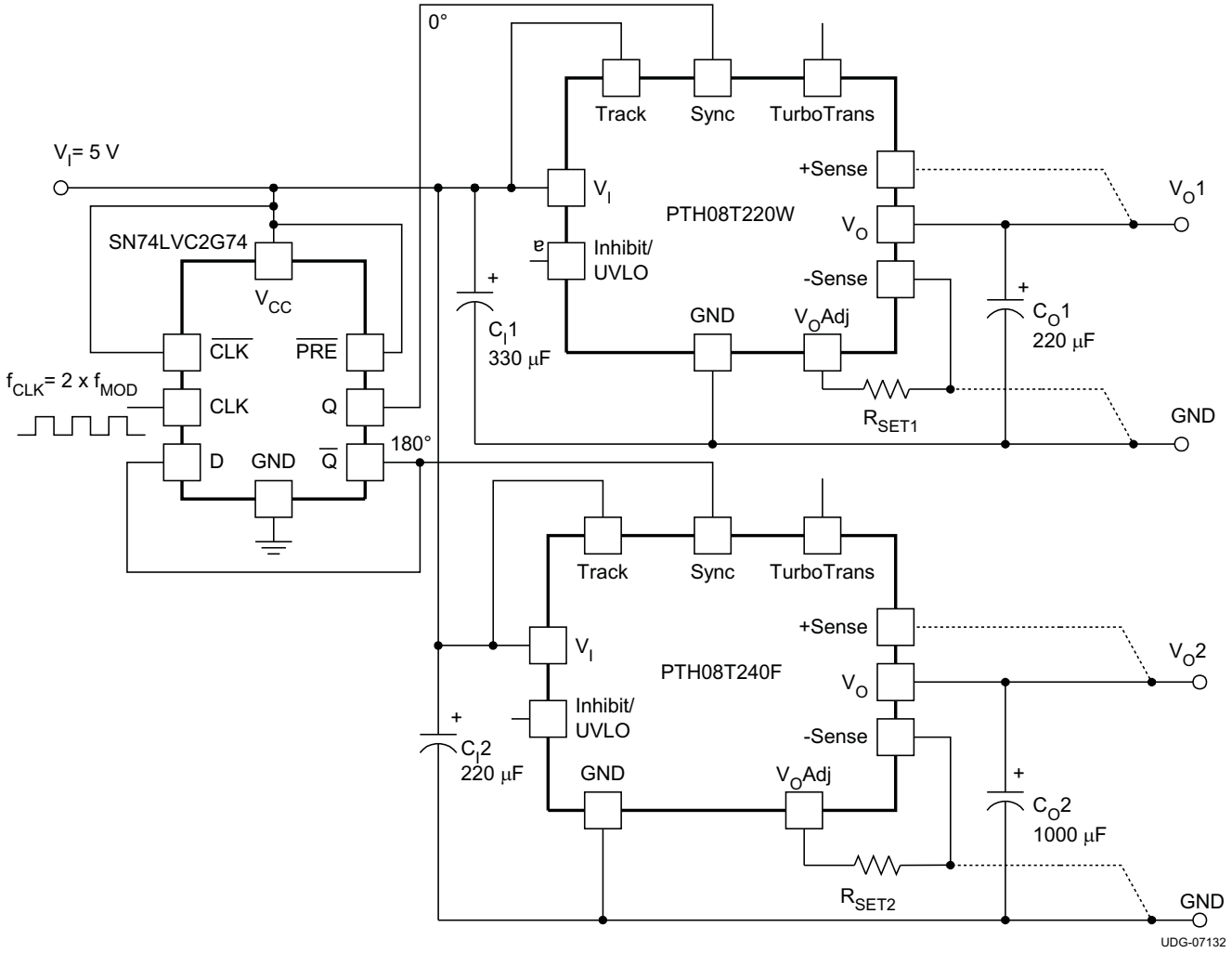


Figure 29. Smart Sync Schematic

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To achieve the output voltage ripple specified in the electrical characteristics table, the maximum input voltage for a given output voltage is limited. The input voltage to output voltage ratio limit is 11 to 1 for the PTH08T240F. However, when using SmartSync, the maximum allowable input voltage varies as a function of output voltage and switching frequency. Operationally, the maximum input voltage is inversely proportional to switching frequency. Synchronizing to a higher frequency causes greater restrictions on the input voltage range. For a given switching frequency, Figure 30 shows how the recommended maximum input voltage varies with output voltage.

For example, a module operating at 375 kHz and an output voltage of 0.9 V, the maximum input voltage is 8 V. Exceeding the maximum input voltage may cause in an increase in output ripple voltage and increased output voltage variation.

As shown in Figure 30, input voltages below 6 V can operate down to the minimum output voltage over the entire synchronization frequency range. See the Electrical Characteristics table for the synchronization frequency range and pulse limits.

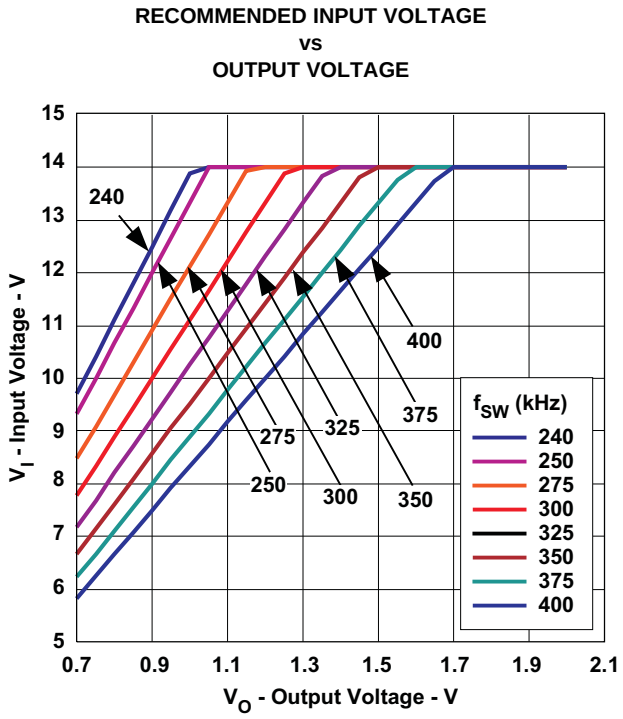


Figure 30.

Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI devices such as the TMS320™ DSP family, microprocessors, and ASICs.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin (1). This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module output remains at its set-point (2). As an example, if the *Track* pin of a 1.5-V regulator is at 1 V, the regulated output is 1 V. If the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 1.5 V.

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When under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit (3). For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

Typical Sequencing Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common Track control signal. This can be an open-collector (or open-drain) device, such as a power-up reset voltage supervisor IC. See U3 in Figure 31.

To coordinate a power-up sequence, the Track control must first be pulled to ground potential. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 20 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization (4), enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes a built-in time delay, is an ideal component for automatically controlling the Track inputs at power up.

Figure 31 shows how the TL7712A supply voltage supervisor IC (U3) can be used to coordinate the sequenced power up of PTH08T240F modules. The output of the TL7712A supervisor becomes active above an input voltage of 3.6 V, enabling it to assert a ground signal to the common track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 28 ms after the input voltage has risen above U3's voltage threshold, which is 4.3 V. The 28-ms time period is controlled by the capacitor C_T. The value of 2.2 µF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the track control voltage is allowed to rise. When U3 removes the ground signal, the track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

Figure 32 shows the output voltage waveforms after input voltage is applied to the circuit. The waveforms, V_O1 and V_O2, represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. V_{TRK}, V_O1, and V_O2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is re-applied to the common track control. This pulls the track inputs to 0 V, forcing the output of each module to follow, as shown in Figure 33. Power down is normally complete before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that an input voltage is no longer present, their outputs can no longer follow the voltage applied at their track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the Auto-Track slew rate capability.

Notes on Use of Auto-Track™

1. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage V_I.
4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 20 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises according to its soft-start rate after input power has been applied.
6. The Auto-Track pin should never be used to regulate the module's output voltage for long-term, steady-state operation.

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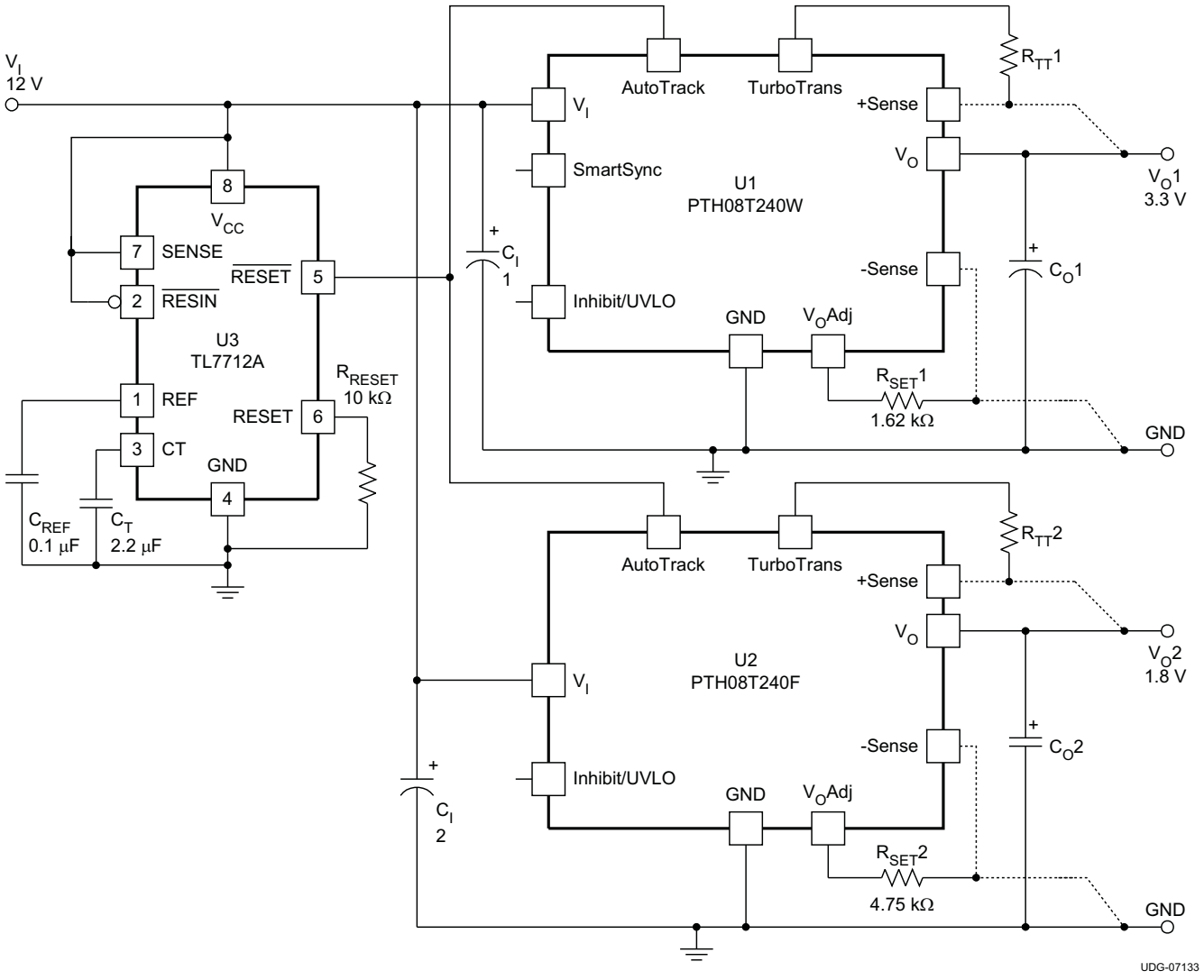


Figure 31. Sequenced Power Up and Power Down Using Auto-Track

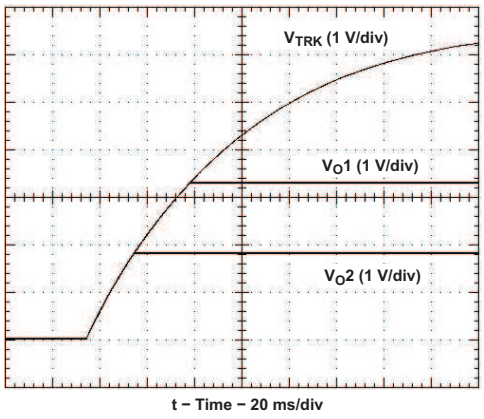


Figure 32. Simultaneous Power Up With Auto-Track Control

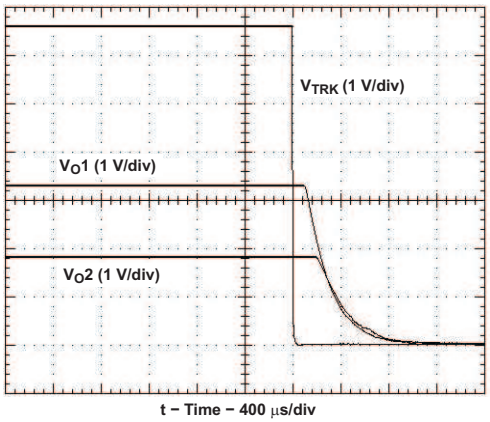


Figure 33. Simultaneous Power Down With Auto-Track Control

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Prebias Startup Capability

A prebias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, these types of modules can sink as well as source output current.

The PTH family of power modules incorporate synchronous rectifiers, but does not sink current during startup(1), or whenever the Inhibit pin is held low. However, to ensure satisfactory operation of this function, certain conditions must be maintained(2). Figure 34 shows an application demonstrating the prebias startup capability. The startup waveforms are shown in Figure 35. Note that the output current (I_O) is negligible until the output voltage rises above the voltage backfed through the intrinsic diodes.

The prebias start-up feature is not compatible with Auto-Track. When the module is under Auto-Track control, it sinks current if the output voltage is below that of a back-feeding source. To ensure a pre-bias hold-off one of two approaches must be followed when input power is applied to the module. The Auto-Track function must either be disabled(3), or the module's output held off (for at least 50 ms) using the Inhibit pin. Either approach ensures that the Track pin voltage is above the set-point voltage at start up.

1. Startup includes the short delay (approximately 10 ms) prior to the output voltage rising, followed by the rise of the output voltage under the module's internal soft-start control. Startup is complete when the output voltage has risen to either the set-point voltage or the voltage at the Track pin, whichever is lowest.
2. To ensure that the regulator does not sink current when power is first applied (even with a ground signal applied to the Inhibit control pin), the input voltage must always be greater than the output voltage *throughout* the power-up and power-down sequence.
3. The Auto-Track function can be disabled at power up by immediately applying a voltage to the module's Track pin that is greater than its set-point voltage. This can be easily accomplished by connecting the Track pin to V_I.

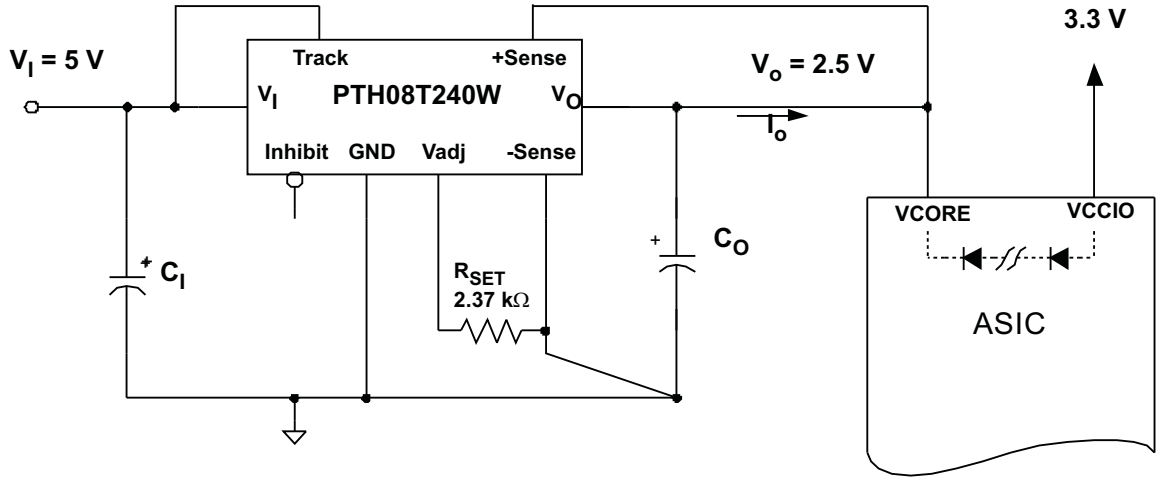


Figure 34. PreBias Startup Application Circuit

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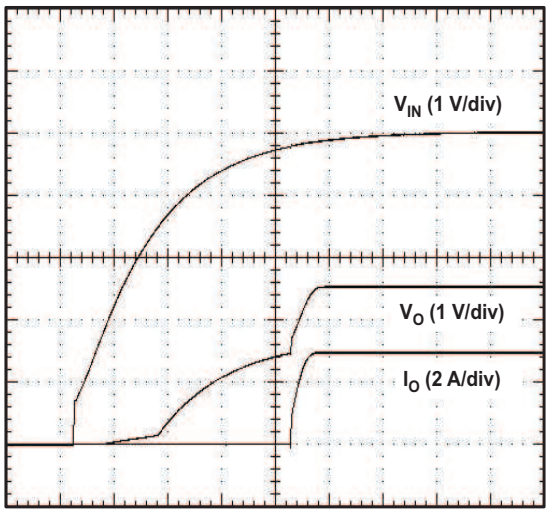
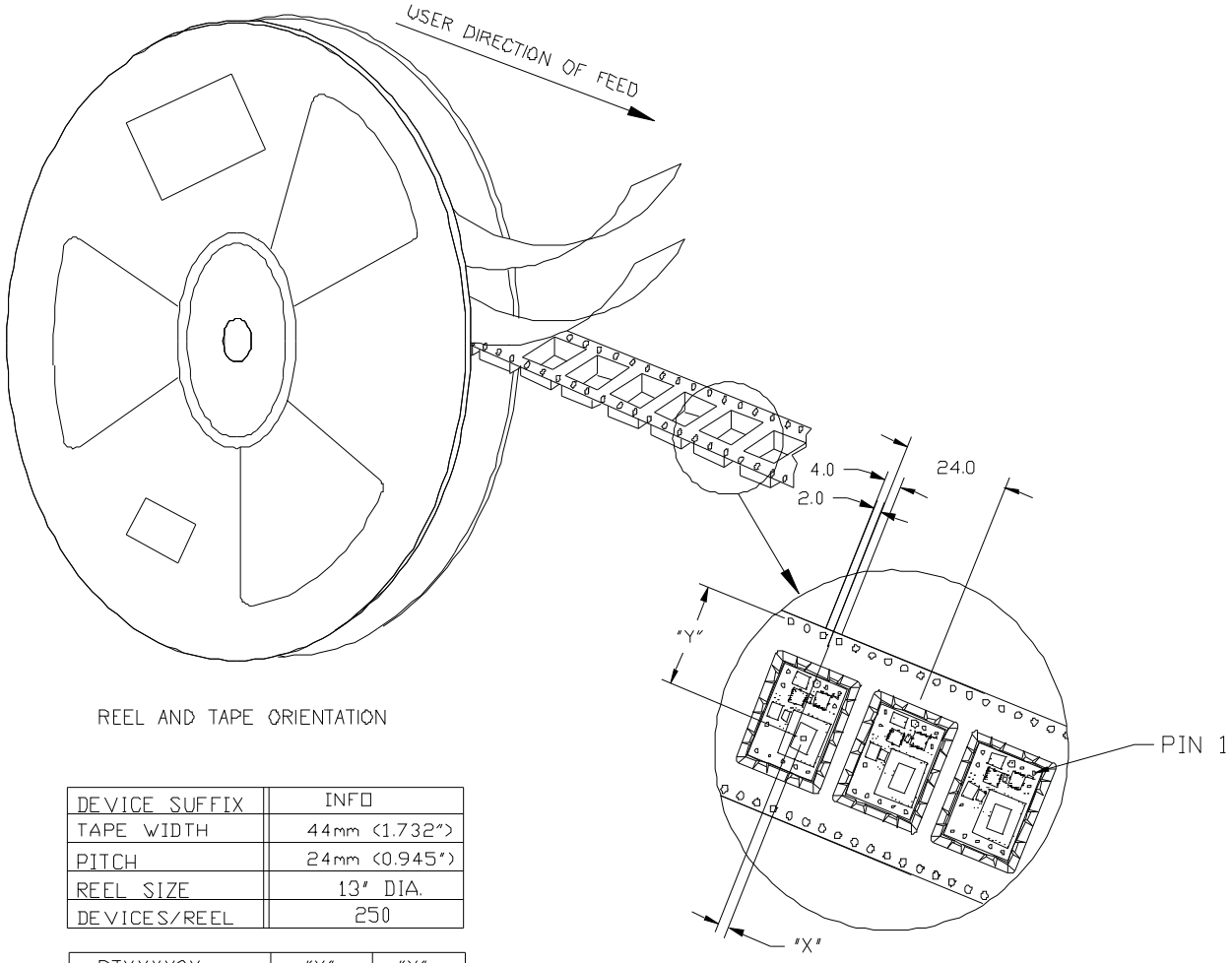


Figure 35. Prebias Startup Waveforms

TAPE AND REEL



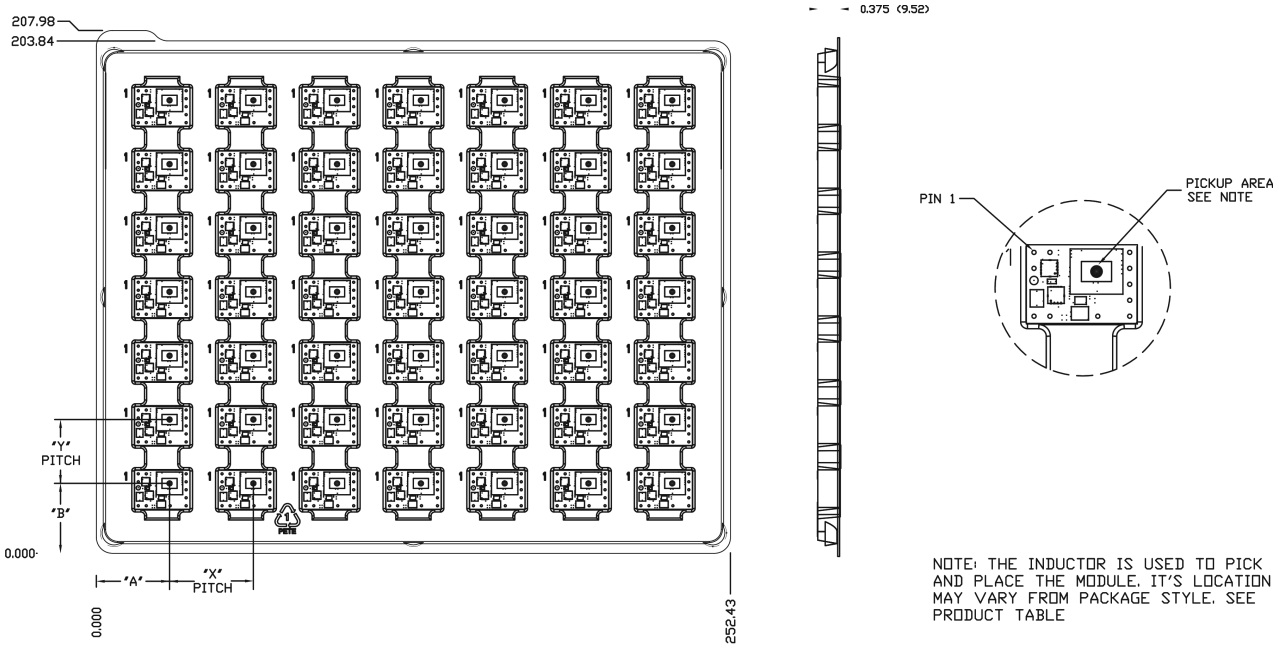
REEL AND TAPE ORIENTATION

DEVICE SUFFIX	INFO
TAPE WIDTH	44mm (1.732")
PITCH	24mm (0.945")
REEL SIZE	13" DIA.
DEVICES/REEL	250

PTXXXX0X	"X"	"Y"
PTH08T240	2.54mm	23.12mm

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TRAY



PTXXXX6X	"A"	"B"	"X"	"Y"
PTH08T240	29.12	27.81	33.35	25.40
ALL DIMENSIONS ARE IN MILLIMETER.				

DEVICES/TRAY	49

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTH08T240FAD	ACTIVE	Through-Hole Module	EBS	11	49	RoHS Exempt & Green	SN	N / A for Pkg Type	-40 to 85		Samples
PTH08T240FAZ	ACTIVE	Surface Mount Module	BBT	11	49	RoHS Exempt & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH08T240FAZT	ACTIVE	Surface Mount Module	BBT	11	250	RoHS Exempt & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples

(1) The marketing status values are defined as follows:
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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

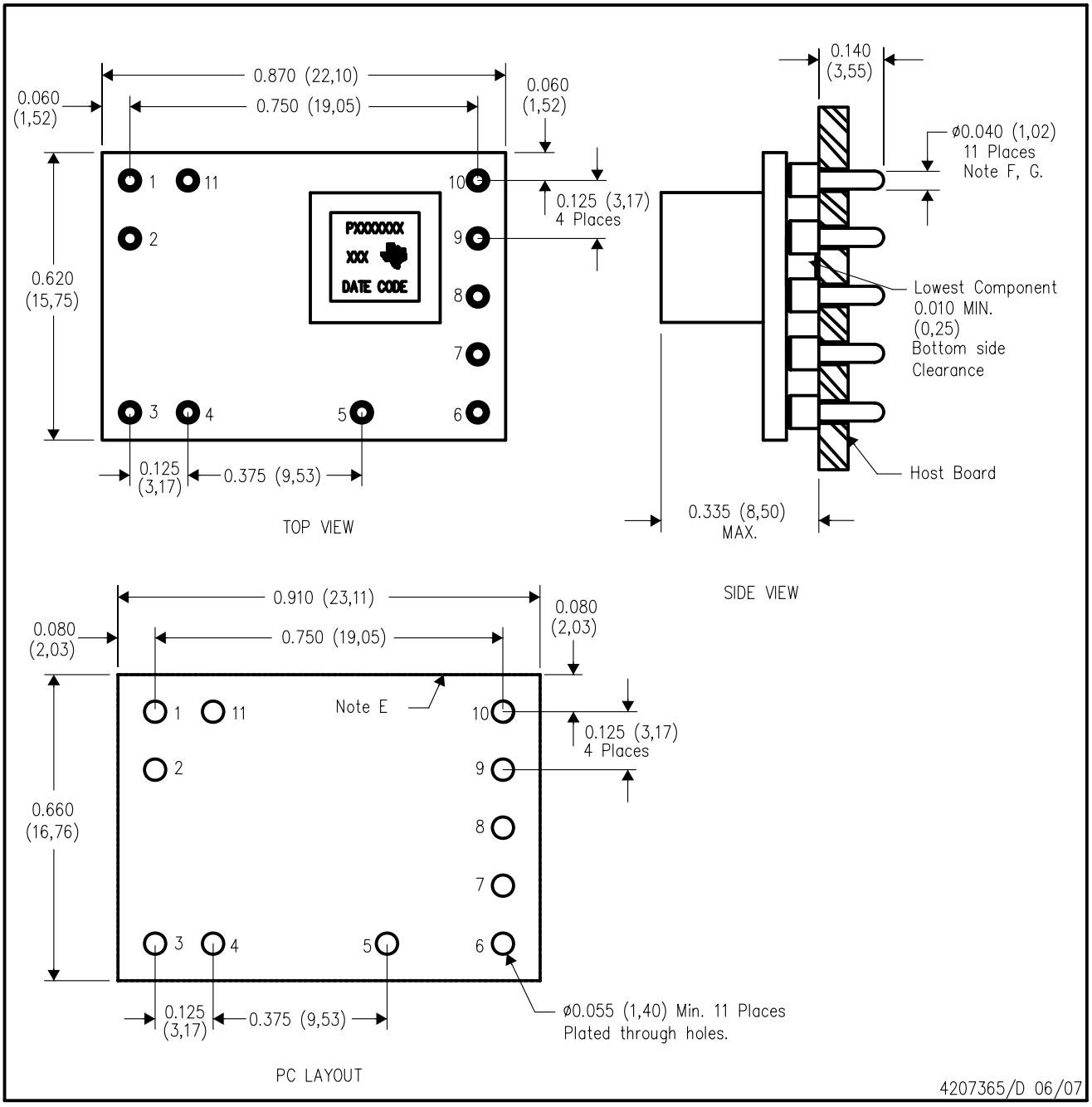
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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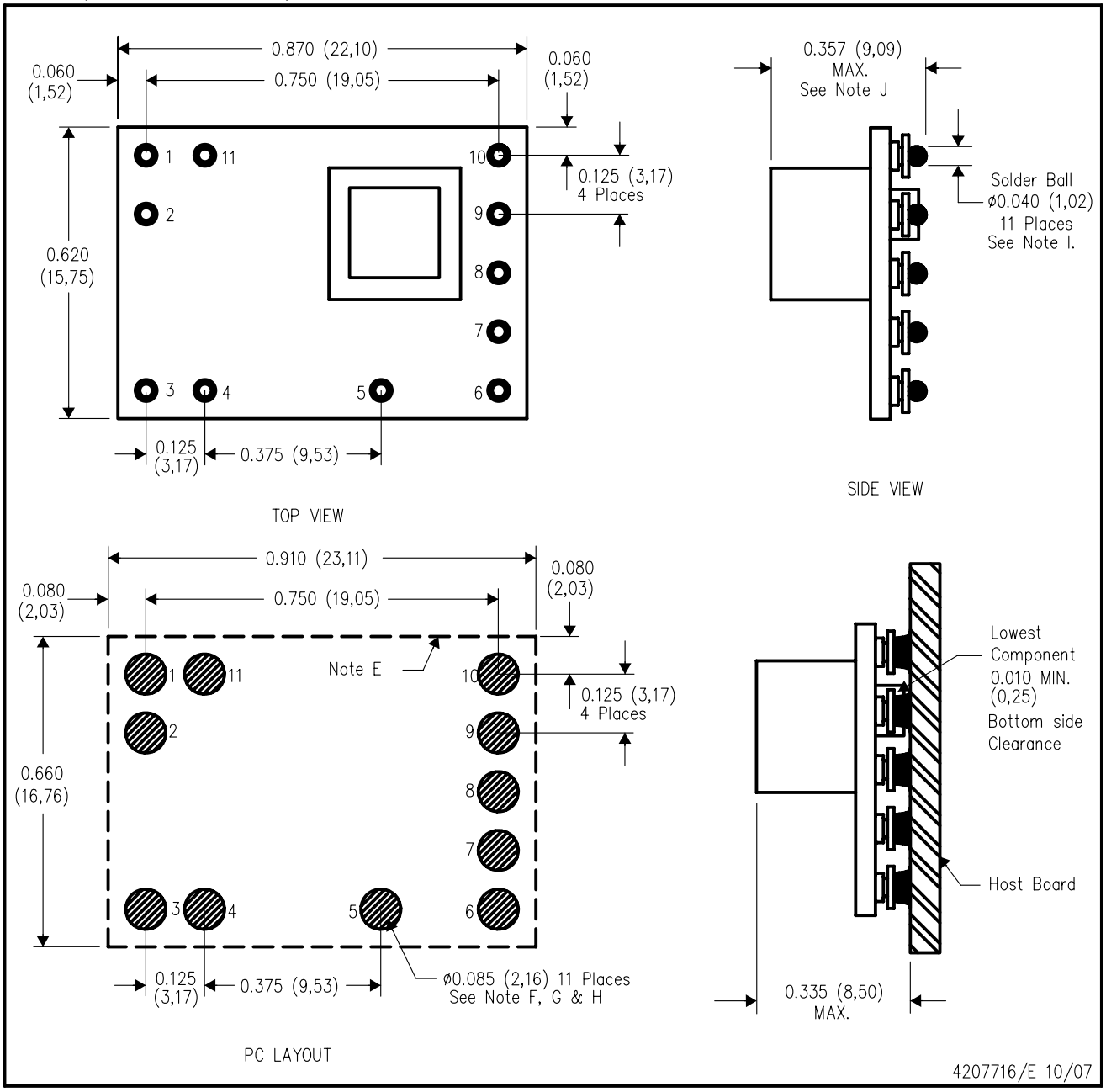
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EBS (R–PDSS–T11) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

BBT (R–PDSS–B11) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – 96.5 Sn/3.0 Ag/0.5 Cu
J. Dimension prior to reflow solder.

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