Texas Instruments

SLK2501 Serdes EVM Kit Setup and Usage

User's Guide

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Preface

Read This First

About This Manual

This manual presents the setup and usage of the Texas Instruments (TI) SLK2501 Serdes evaluation module (EVM). This board is used to evaluate the SLK2501 device(VQFP) and associated optical interface (SCM6028) for point-to-point data transmission applications.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—SLK2501 EVM Kit Contents and Board Configuration
- Chapter 3—Typical Test and Setup Configurations
- Appendix A—Schematics, Board Layouts, and Suggested Optics and Cable Assembly Specifications.

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Chapter 1

Introduction

The Texas Instruments (TI) SLK2501 Serdes evaluation module (EVM) board is used to evaluate the SLK2501 multirate transceiver device (100-pin VQFP) and associated optical interface (SCM6028) for point-to-point data transmission applications.

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1.1 EVM PCB

The SLK2501 EVM board enables designers to connect 50-Ω parallel buses to both the transmitter and receiver parallel connectors. Using high-speed PLL technology, the SLK2501 transceiver serializes and transmits data along a differential pair. The receiver part of the device deserializes, detects the data frame, and presents the data on the parallel bus together with a frame sync signal. The high-speed (up to 2.5 Gbps) data lines interface to four 50-Ω controlled-impedance SMA connectors. Designers can either use this copper interface directly or loop back to the laser module section for an optical interface (not provided, see Appendix A).

1.2 Using the EVM

The board can be used to evaluate device parameters while acting as a guide for high-speed board layout. Evaluation boards can be used as daughterboards that are plugged into new or existing designs. The SLK2501 supports different frequency ranges (OC3 – OC48).

1.3 Design of Serial High-Speed Traces

1.3.1 Differential Traces

As the frequency of operation increases, board designers must take special care to maintain the highest signal integrity. This applies to both the high-speed differential serial and parallel data connections.

To cover a wide range of usage, each trace of the differential signal pair is matched to maintain a 50-Ω line impedance. The separation of each trace from its complementary differential trace is chosen to be wider then 3W (three-times the trace width). Therefore, almost no coupling exists between lines (traces are treated as in single-ended applications). The differential impedance of a differential-signal pair calculates to two-times the single-ended impedance (50 Ω + 50 Ω = 100 Ω).

The trace width of all impedance-controlled lines is 152 µm (6mil) on the EVM. All differential lines are routed as strip lines on layer 3.

1.3.2 Other Considerations

Impedance mismatches must be minimized to maintain a flat 50-Ω impedance along the transmission line. Therefore, the component pad size of the high-speed pads has been shrunk to a size similar to the width of the connecting transmission lines. Vias are minimized and, when necessary, placed as close as possible to the device drivers. Since the board contains both serial and parallel transmission lines, care is taken to control both impedance and trace-length mismatch (board skew).

Overall, the board layout is designed and optimized to support high-speed operation. Thus, understanding impedance control and transmission line effects is crucial when designing high-speed boards.

This board includes the following advanced features:

- ❑ The PCB (printed-circuit board) is designed for high-speed signal integrity.
- ❑ Flexibility—the PCB can be configured for copper or optical interfaces.
- ❑ SMA and parallel fixtures are easily connected to test equipment.
- ❑ All input/output signals are accessible for rapid prototyping.
- ❑ Analog and digital power planes can be supplied through separate banana jacks for isolation, or can be combined using ferrite bridging networks.
- ❑ Onboard capacitors (next to SMA connectors) provide ac coupling of high-speed signals.

1.4 Design Considerations

In addition to the features incorporated into the EVM, designers may wish to use blind and buried vias to minimize stub lines if the interconnect is critical in terms of overall attenuation and signal degradation. Since the SLK2501 supports different frequency ranges (OC3 – OC48), designers must optimize their design for the frequencies of interest. Since most board layouts are very space critical, designers may want to route each signal trace of a differential pair tightly close to each other. This increases coupling between differential traces. To compensate for this additional coupling, the trace width can be shrank accordingly to maintain 100-Ω differential-line impedance. The internal receiver termination of the SLK2501 matches particularly well with a strong coupling type differential-input line.

Chapter 2

SLK2501 EVM Kit Contents and Board Configuration

This chapter describes the SLK2501 EVM kit contents and board configuration.

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2.2 SLK2501 EVM Board Configuration 2-2

2.1 SLK2501 EVM Kit Contents

The SLK2501 EVM kit contains the following:

- ❑ SLK2501 EVM board
- ❑ SLK2501 EVM kit documentation (this document)

2.2 SLK2501 EVM Board Configuration

The SLK2501 EVM board provides developers with various options for operation, many of which are jumper selectable. Other options can be either soldered into the EVM or connected through input connectors.

2.2.1 TX/RX Signals

Each of the TX and RX parallel signals (TXDATA, TXCLK, RXDATA, RXCLK, FRAME, etc.) are placed separately as a 4-pin connector (bird sticks). This simple solution can ensure good functionality for the differential signals running up to 622 MHz. The high-speed serial-data traces are routed very carefully, and each one interfaces to an SMA connector. They can also be disconnected from the trace and routed to the optical module instead. Please refer to the *Interface—Optical Module vs Copper Cable* section for specific information. The reference-clock input also uses SMA connectors. This minimizes line reflections and ensures low jitter.

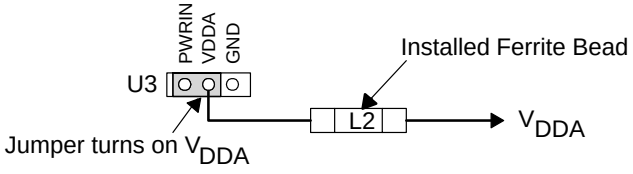
2.2.2 Control Header

Headers U6 and U11 provide static signals (normally pulled high) to configure the device for different modes of operation. The *Outputs* header carries all LVTTL static output. The U9 header indicates that the optical transmitter has detected a signal. This signal can be connected to the SIGDET input of header U11 with a small wire. The Dis header allows the operator to disable the optical transceiver.

2.2.3 Power Planes

The power planes are split six ways to provide power to different parts of the board. This prevents coupling of switching noise between the analog and digital sections of the SLK2501 and provides voltage isolation for the laser section. The laser section of the board requires 3.3 V and is energized through the V_{CC} connector. The J1 (PWR IN) connector requires 2.5 V. All other power planes (V_{DD}, V_{DDA}, V_{DDPLL} and V_{DDLVDS}) are supplied off the PWR IN plane by removable ferrite beads L1 – L4 installed in the default configuration.

Figure 2–1. Installing Power Planes



In all sections of the board, the ground planes are common and each ground plane is tied together at every component-ground connection. The EVM has

two ground planes on layers 2 and 4. Furthermore, empty space on the TOP and BOTTOM planes is filled with ground-plane trace. See *SLK2501EVM Schematic* and *Board Layer Stack-up* in Appendix A for detail schematics and layout drawings.

2.2.4 Default EVM Delivery Settings

The board is normally delivered in a default configuration that requires external clock and data inputs. The SLK2501 is shipped with jumpers for default operation. Table 1 shows the default configuration for sending data.

Table 2–1. Default Transceiver Board Configuration

Designator	Function	Condition
U11	RLOOP	Jumper installed (logic 0) Remote loop-back of serial data disabled
	LLOOP	Jumper installed (logic 0) Serial loop-back disabled
	RSVD	Jumper installed (logic 0) Always high to GND
	LOOPTIME	Jumper installed (logic 0) PLL not bypassed
	$\overline{\text{RESET}}$	Jumper not installed (logic 1) Reset disabled
	RXMONITOR	Jumper not installed (logic 1) – For repeater mode only. In repeater mode, parallel data is presented at RXOUT terminals.
	ENABLE	Jumper not installed (logic 1) Normal device operation
	TESTEN	Jumper not installed (logic 1) Production mode disabled
	PRBS_EN	Jumper not installed (logic 1) PRBS pattern generator disabled
	REFCLKSEL (V_{DD} pin on SLK2511, GND pin on SLK2501)	Jumper not installed (logic 1) Supplied oscillator frequency at REFCLK is 622.08 MHz
	RSEL0	Jumper not installed (logic 1) Serial data rate at 2.488 Gbps (OC48) if autorate detection is disabled
	RSEL1	

Table 2–1. Default Transceiver Board Configuration as Shipped (Continued)

Designator	Function	Condition
U6	*AUTO_DETECT*	Jumper not installed (logic 1) Autorate detection enabled
	FRAME_EN	Jumper not installed (logic 1) Frame synch enabled
	LCKREFN	Jumper not installed (logic 1) Receiver clock RXCLKP/N presents recovered data clock of receiver input stream
	PS	Jumper not installed (logic 1) Receiver is activated
	SIGDET	
	CONFIG1	Jumper not installed (logic 1) Transceiver mode
	CONFIG0	
	PRE2	Jumpers not installed (logic 11) Preemphasis 30% (highest drive)
	PRE1	
DIS	DIS	Jumper not installed (logic 1) Optical module enabled
C51, C52, C53, C54	Serial out to SMA	Installed High-speed serial data tight to STXDOx and SRXDOx SMA connectors
C47, C48, C49, C50	Serial out to optics	Not installed High-speed serial data not connected to the optical module
L1, L2, L3, L4	PWR IN bridge to all power planes	Installed All power planes supplied through J1 (PWR IN) supply

Note: See SLK2501 data sheet for details

Table 2–2. Configuration Changes Necessary for Use of the Optical Module

Designator	Function	Condition
C51, C52, C53, C54	Serial out to SMA	Remove capacitors
C47, C48, C49, C50	Serial out to optics	Install capacitors

Chapter 3

Typical Test and Setup Configurations

Many test setups can be used to evaluate the operation of the SLK2501. This chapter explains some of these options.

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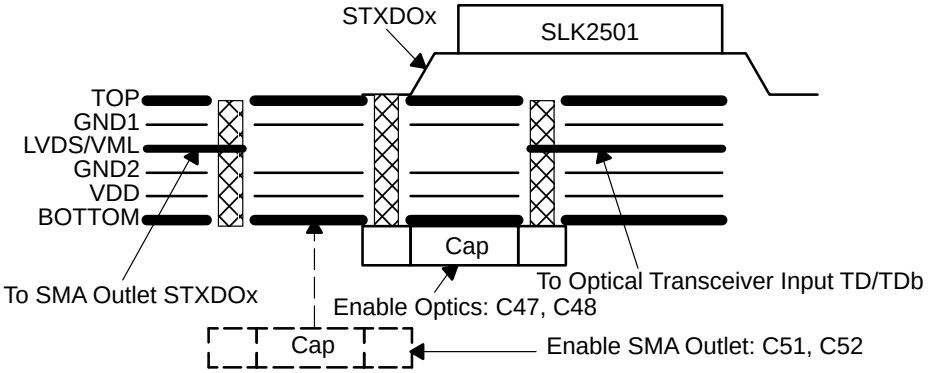
3.1 Interface—Optical Module vs Copper Cable

Before discussing different test configurations, the operator of the EVM must decide between installing the SCM6028 optical module or interfacing the serial Sonet/SDH stream over a copper cable using the SMA connectors STXON, STXOP, SRXDIP, and SRXDIN. The SLK2501 high-speed I/O can be connected to both, the onboard optical module and the SMA connectors. The EVM design has been optimized to prevent stub lines.

Installation advice:

- ❑ Using the onboard optical transceiver: install C47–C50, leave C51–C54 open.
- ❑ Using the SMA connectors: install C41–C54, leave C47–C50 open.

Figure 3–1. PCB Design of the High-Speed I/O to Minimize Stub-Line Effects



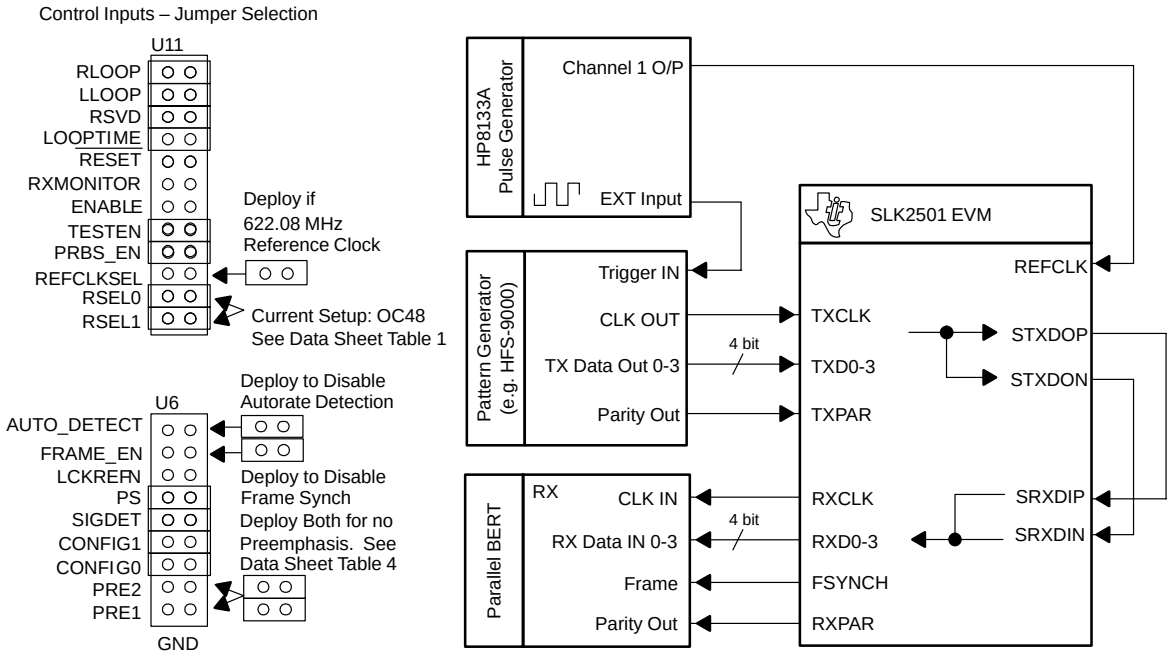
3.2 Serial Loopback, Test With Parallel BERT

The first configuration is a serial loopback of the high-speed signals shown in Figure 3–2. It only requires one SLK2501 EVM. The serial loopback allows designers to evaluate most of the functions of the transmitter and receiver sections of the SLK2501 device. To test a system, a parallel bit-error-rate tester (BERT) or pattern generator generates a predefined parallel-bit pattern. The pattern is connected to the transmitter through LVDS pin connectors TXD0–TXD3. The data clock goes into TXCLK. The reference clock (most accurate clock, low jitter) is connected to the two SMA REFCLK inputs.

Optionally, a parity pattern can be applied to the TXPAR input that can check the correct receive status of the transmitter input on output pin Par Valid. Additionally, control pins $\overline{\text{RESET}}$ and FRAME_EN can be operated by the BERT. However, the simplest solution is to pull $\overline{\text{RESET}}$ to V_{DD} and choose to enable the frame synchronization upon the available features on the receiver BERT. Asserting FRAME_EN enables the frame synchronization of the SLK2501 data output and presents the frame information at the FSYNCH output.

The SLK2501 device serializes and presents the data on the high-speed serial pair. The serial TX data is then looped back to the receiver side and the device deserializes and presents the data on the receive side RXD0–RXD3 together with the frame start information (if FRAMEN=1) and the recovered receive clock RXCLK. The differential output FSYNCH can be used to align input and output words of an synchronous BERT to compensate for the signal delay over the link. The parity of the RX data can be monitored on the RXPAR output pins. If any bit errors are received, the bit error rate is evaluated at the parallel receive BERT.

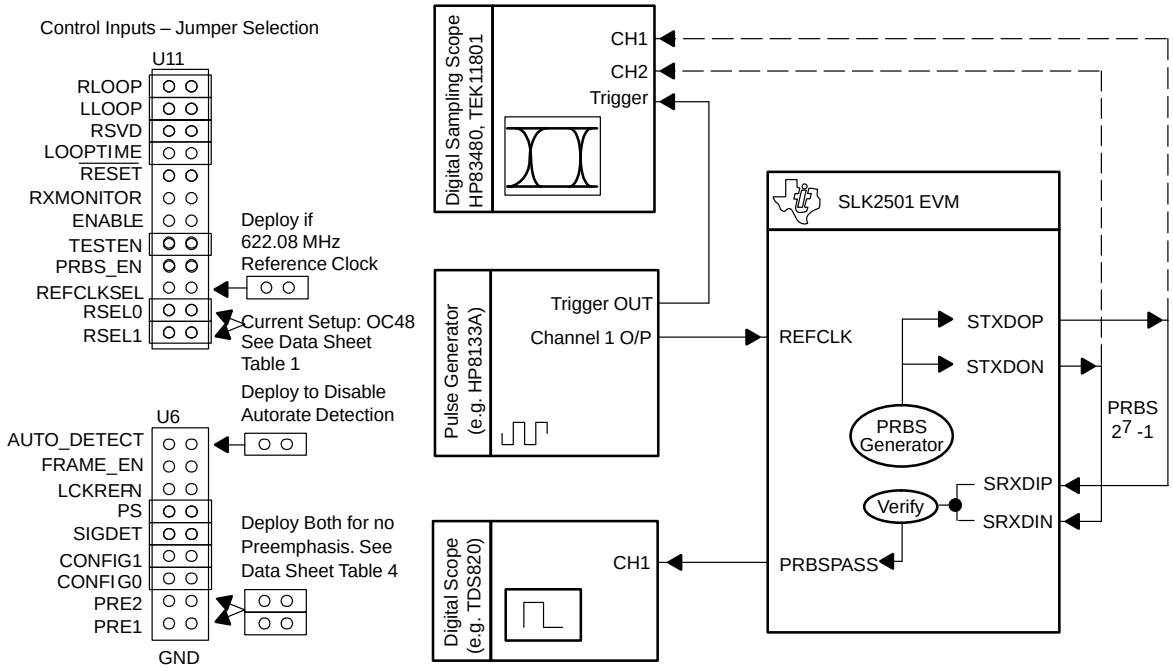
Figure 3–2. SLK2501 Serial Loopback Test Configuration Using the Parallel BERT



3.3 Built-In Self-Test Using the PRBS Pattern Generator

If a parallel BERT is not available, the designer can take advantage of the built-in test mode of the device, see Figure 3–3. When the PRBSEN pin is asserted high, a pseudorandom bit pattern is transmitted (2^7–1 pattern). This pin also puts the receiver in the proper mode to detect a valid PRBS pattern. A valid pattern is indicated by the PRBSPASS being high. This test only validates the high-speed serial portion of the device and system interconnects. The PRBS pattern is compatible with most serial BERT test equipment. This function allows the operator to isolate and test the transmitter and receiver independently. A typical configuration is shown in Figure 3–4. The dashed lines represent optional connections that can be made while monitoring eye patterns and measuring jitter.

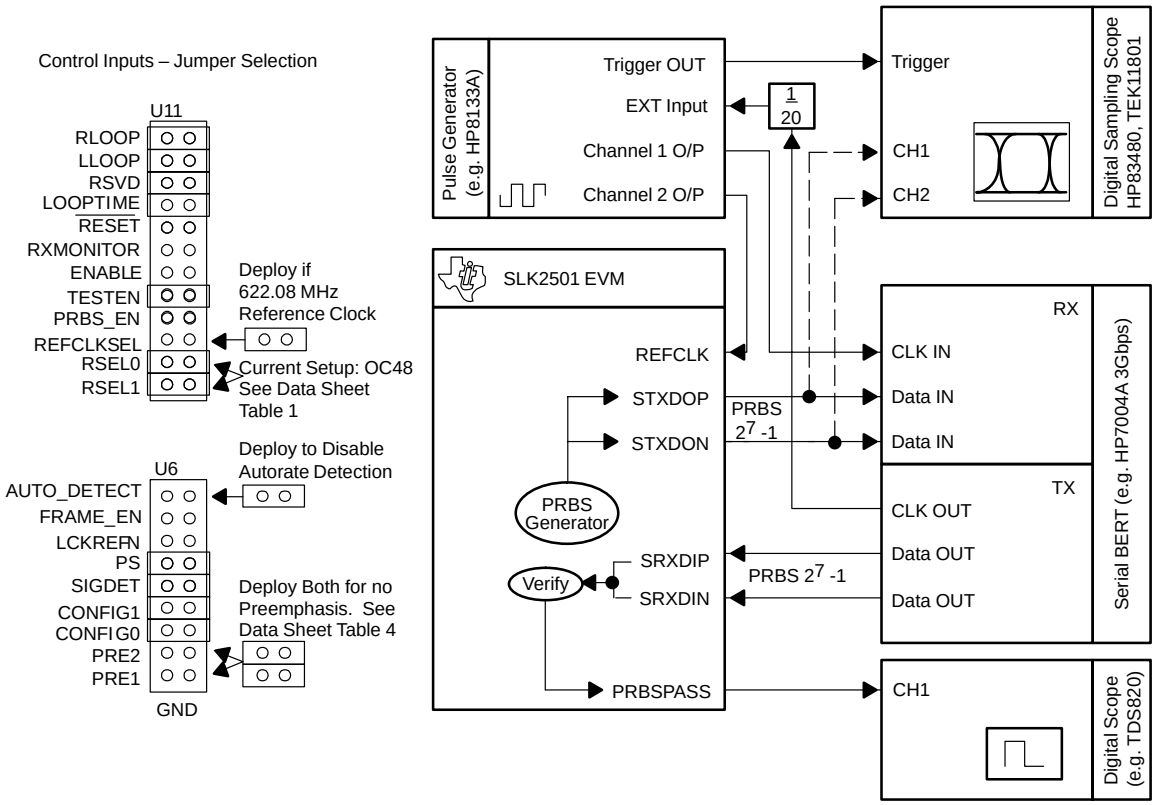
Figure 3–3. SLK2501EVM Serial PRBS Self-Test Configuration



3.4 Checking the Serial Interface With a Serial BERT

The next setup allows to test the serial interface. A serial BERT verifies the PRBS transmit data generated by the internal SLK2501 PRBS pattern generator. The opposite direction of data flow can be driven by a serial BERT generating the same 2^7–1 pattern. The SLK2501 receiver signals proper reception of these data by asserting the PRBSPASS pin.

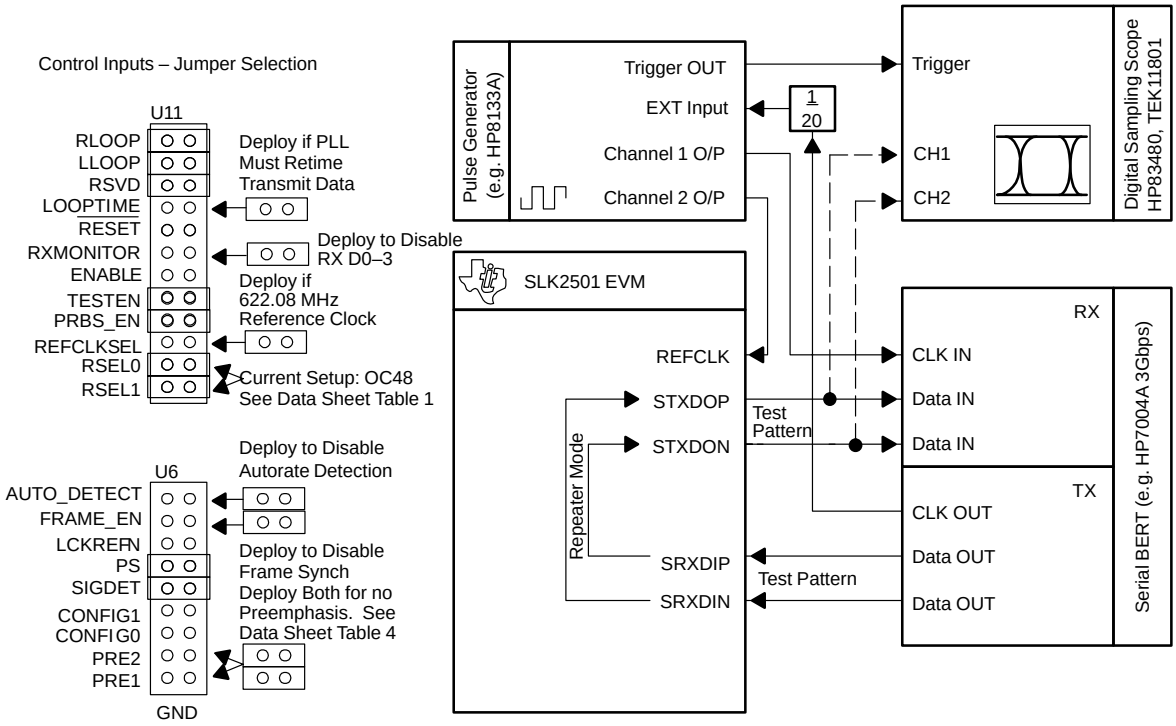
Figure 3–4. SLK2501EVM Serial PRBS BERT Test Configuration



3.5 Checking the Serial Interface With a Serial BERT and Random Pattern

A similar option to the last paragraph is the use of a serial BERT transmitting random data. These data are fed into the SLK2501 serial input, recovered internally, and sent back to the serial output of the same SLK2501. The serial receiver BERT can now verify the pattern. Again, the dotted lines could be used to observe the transmitter's data eye.

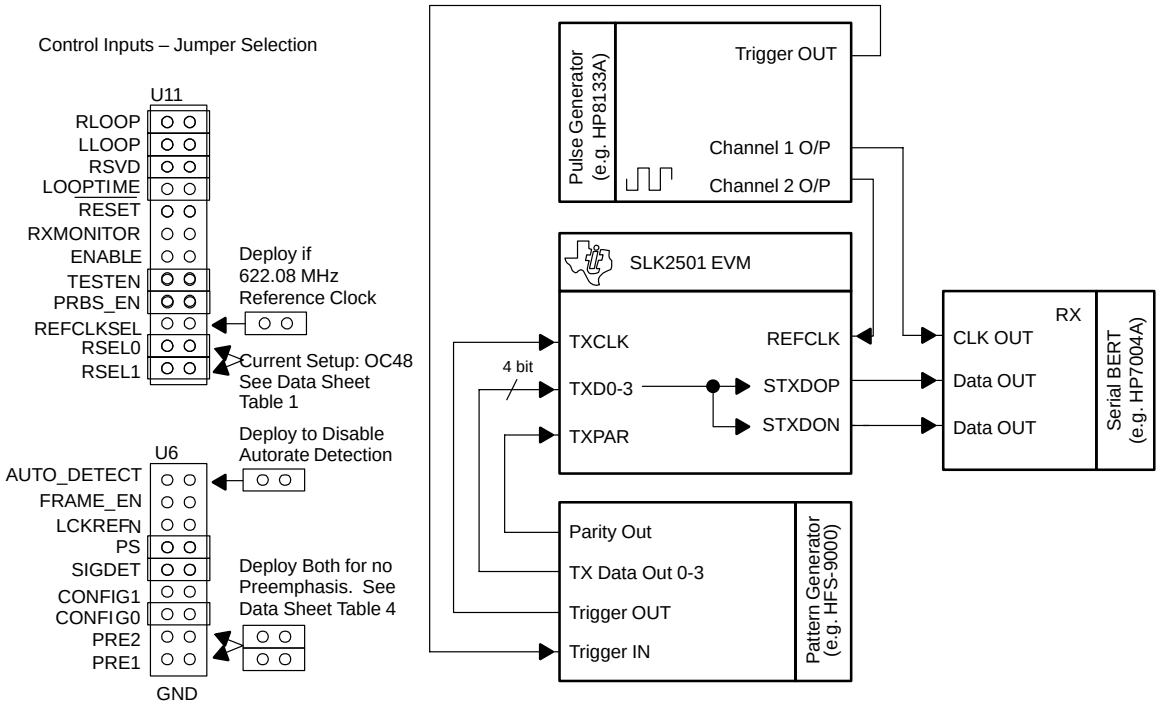
Figure 3–5. Serial BERT and SLK2501 in Repeater Mode



3.6 Transmitter Test Only

Use the following procedure to test the transmitter portion of the SLK2501 only: Apply a pattern to the four-bit parallel input of the device. Set the SLK2501 to transmit only mode. The SLK2501 transmits the applied data to the serial output. A serial BERT is used to verify the transmit pattern.

Figure 3–6. Transmitter Characterization



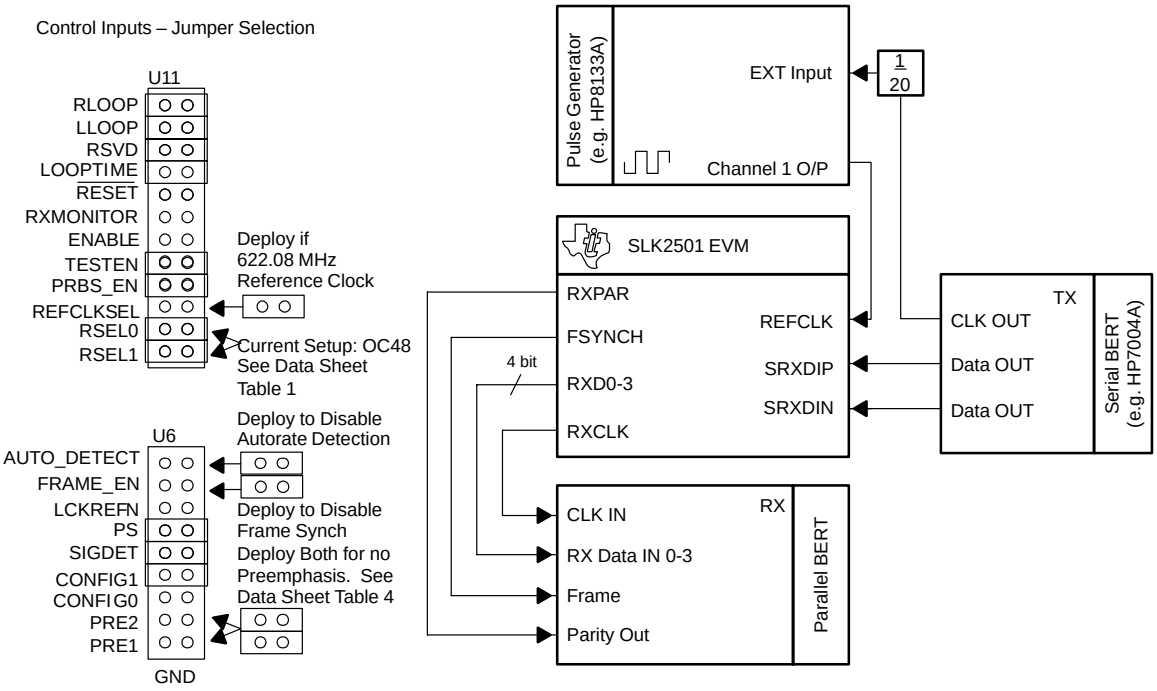
3.7 Receiver Test

Figure 3–7 shows a setup to check out the receiver operation only. The SLK2501 is set to receive mode. A high-speed serial byte is applied to the receiver input of the SERDES and the recovered byte appears at the parallel output of the receiver.

Note: FSYNCH Detection

When FRAME_EN is enabled (high), the SLK2501 searches for a A1A1A1A2 repetitive pattern each 125 µs. If this pattern is found, the FSYNCH output toggles high for one LVDS bit time. On a scope screen monitoring all four LVDS outputs, the user can observe the alignment of the first four bits of the A1 pattern (for example, if A1=1111 0110, all four outputs show high at the same time).

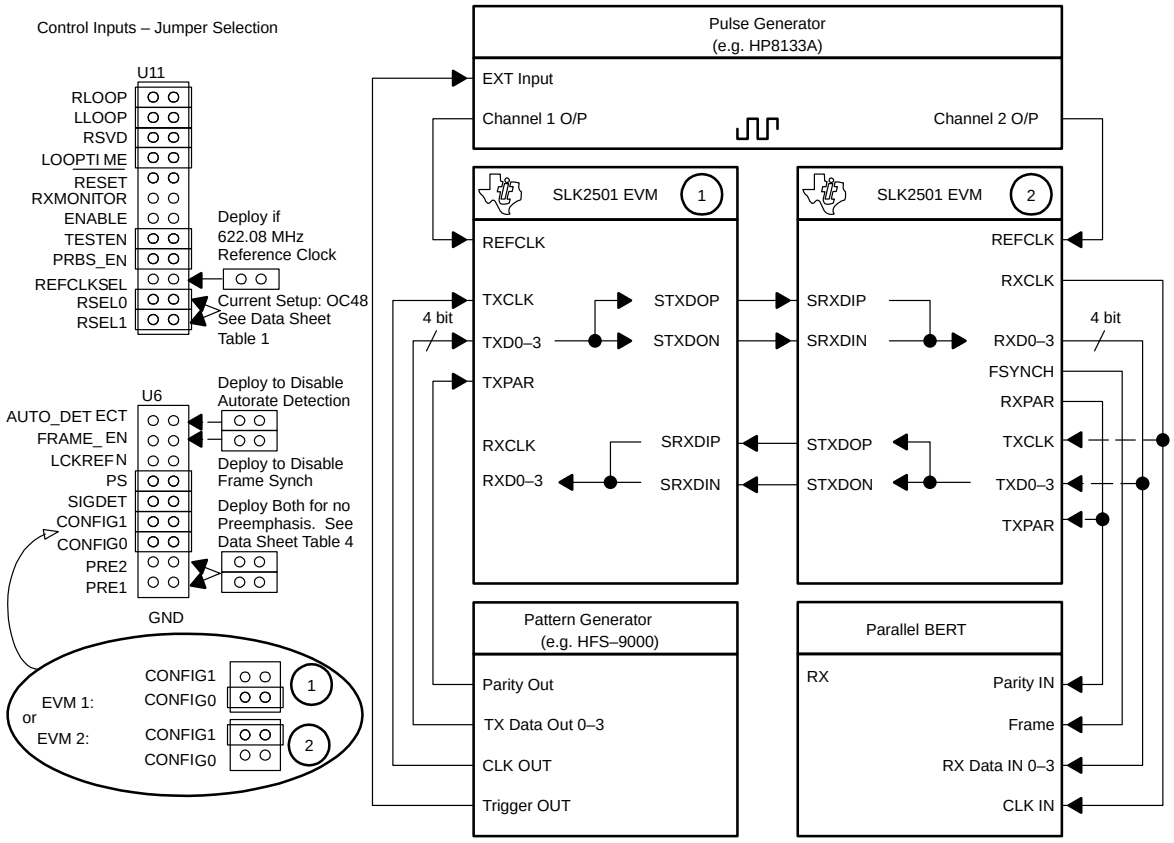
Figure 3–7. SLK2501 in Receiver Mode



3.8 Two-Device Communication Test

A board-to-board communication link is a practical method of evaluating the SLK2501 in a system-like environment. This is illustrated in Figure 3–8. A parallel BERT or a logic analyzer can be used to provide and monitor the signals to and from the transceiver pairs. Both REFCLK sources must have the same frequency within 150 PPM for asynchronous operation. Otherwise, the PLL indicates out-of-lock and assert the LOL pin. Synchronous operation can be achieved by using the BERT or by using a synchronized pulse generator to supply both boards with REFCLK inputs.

Figure 3–8. Communication Between Two Serdes Devices



3.9 Use of the Optical Module in the Loopback

The following setup can be used to test the influence of the optical interconnect on overall performance. The SLK2501 uses basically the same setup as shown in section 3.2, *Serial Loopback*. The only user intervention required is to remove from the board all capacitors that connect the SMA connectors to the SLK2501's serial I/O and then replace them with four capacitors to connect the SLK2501's serial I/O to the optical module's PECL I/O.

Figure 3–9. Communication With the Optical Module in the Loopback

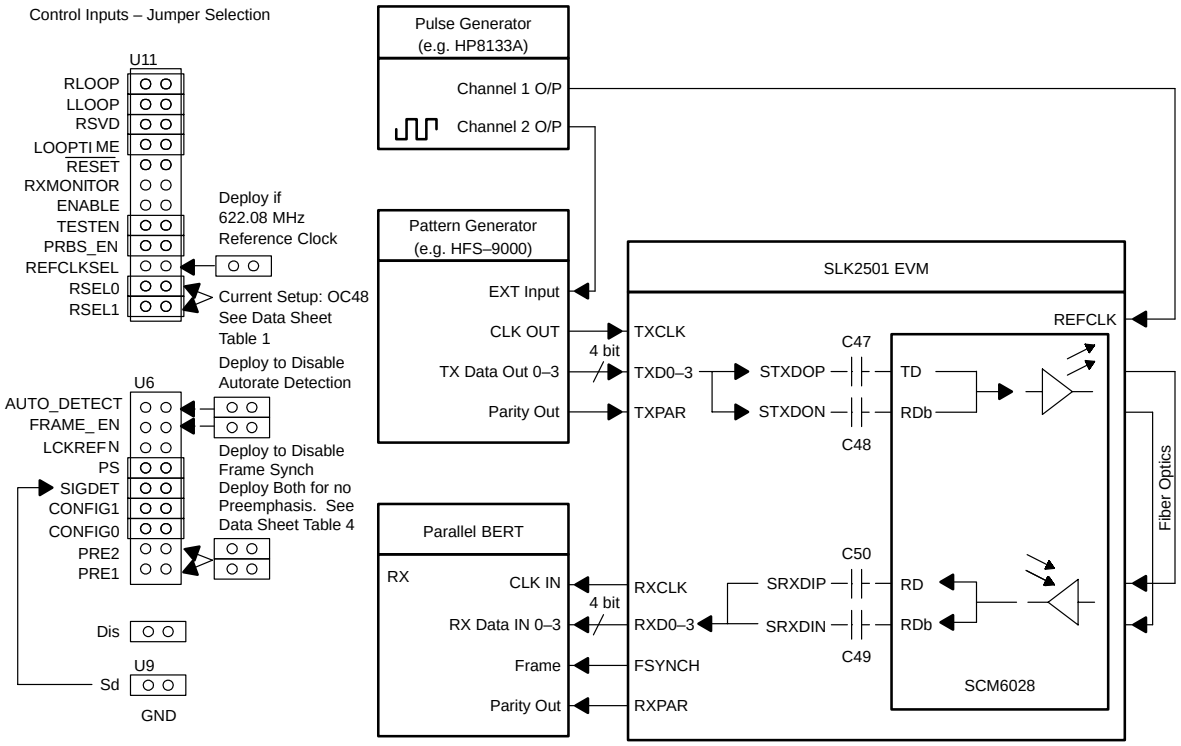
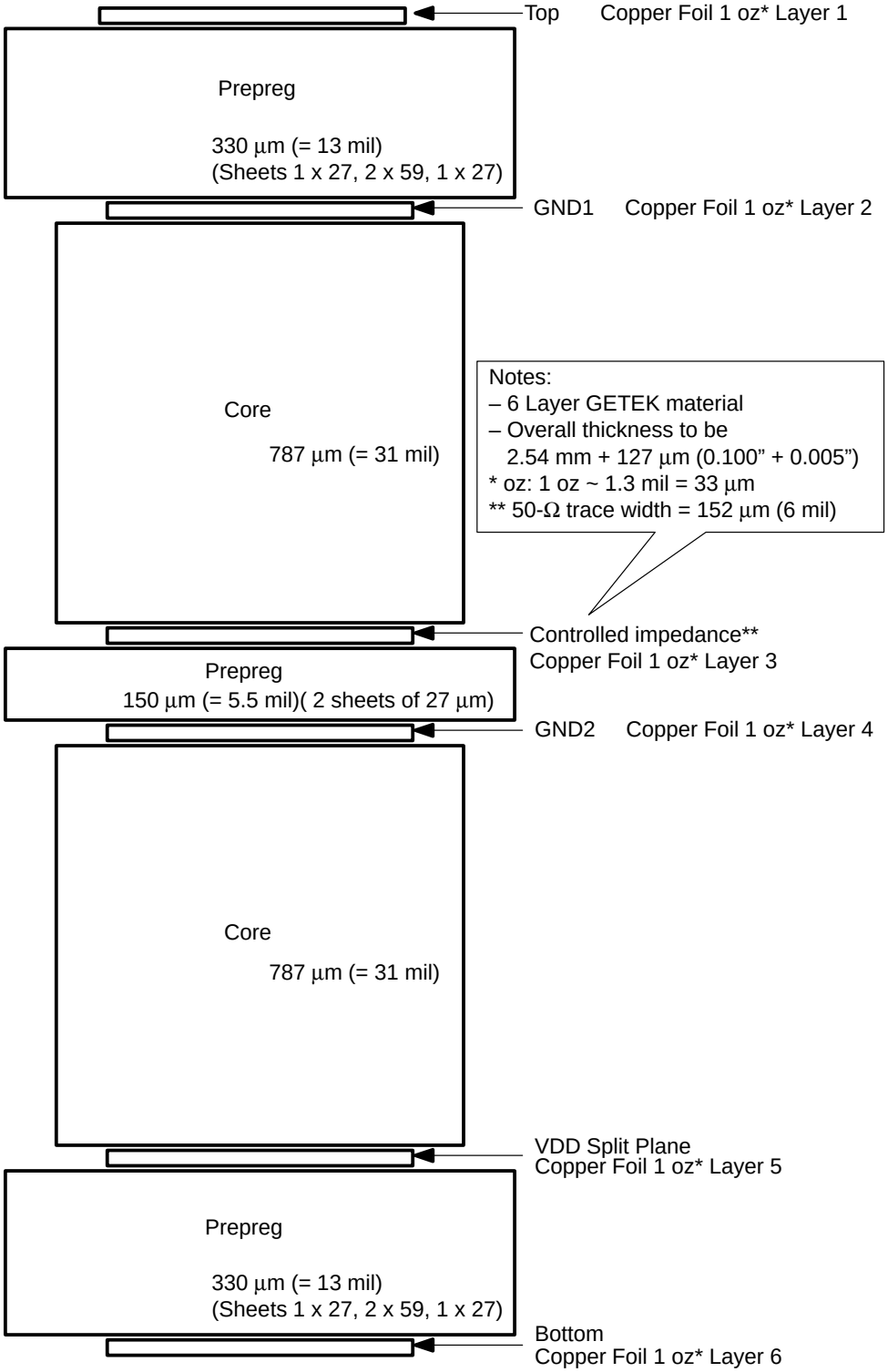


Table 3–1. SLK2501 Differential Pair PCB Transmission Line Characteristics

Device Pin No.	Connector Pin No.	Trace Width μm (mil)	Length mm (inches)
STXDON	8	152 (6)	36.8 (1.449)
STXOP	9	152 (6)	36.8 (1.449)
SRXDIP	15	152 (6)	36.8 (1.449)
SRXDIN	14	152 (6)	36.7 (1.445)
REFCLKN	95	152 (6)	53.9 (2.122)
REFCLKP	94	152 (6)	53.9 (2.122)

Note: All values presented in this table are theoretically calculated values and may not reflect actual measured parameters.

Figure 3–10. SLK2501EVM Layer Construction



Appendix A

Schematics, Board Layouts, and Suggested Optics and Cable Assembly Specifications

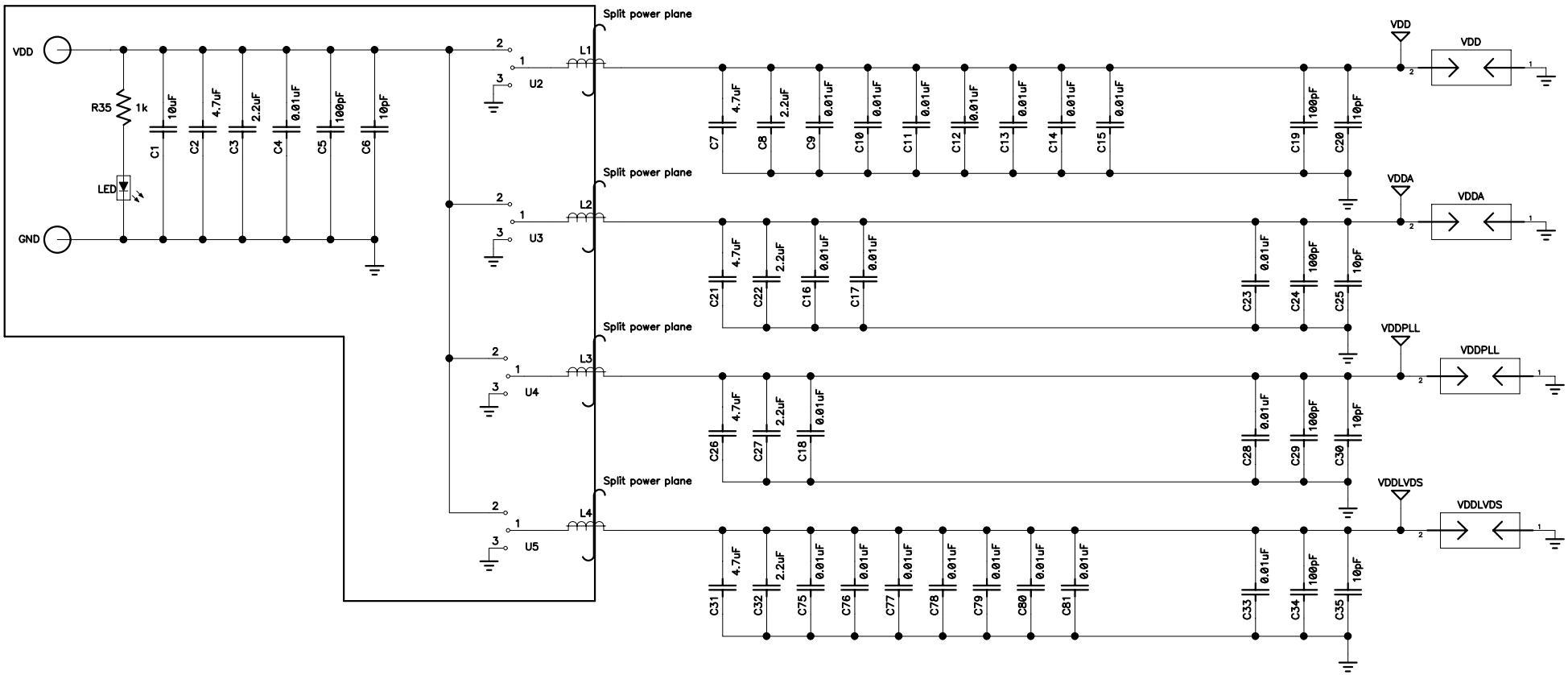
This appendix contains schematics, bill of materials, board layout, and suggested optics and cable assembly specifications for the SLK2501EVM EVM transmitter and receiver boards.

A.1 Schematics

Figure A–1. SLK2501EVM Transceiver Schematic—Sheet 1

Figure A–2. SLK2501EVM Transceiver Schematic—Sheet 2

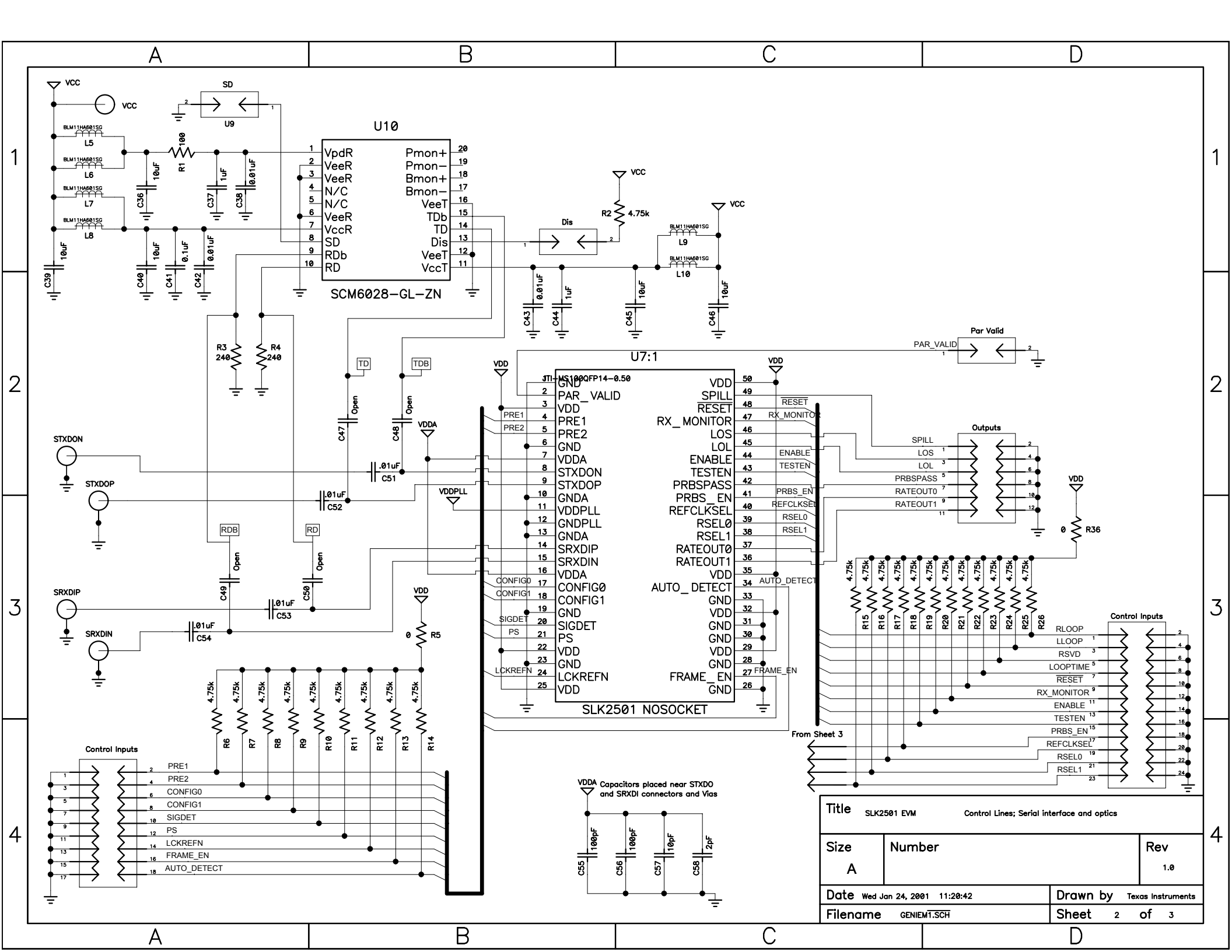
Figure A–3. SLK2501EVM Transceiver Schematic—Power Supply Circuit—Sheet 3

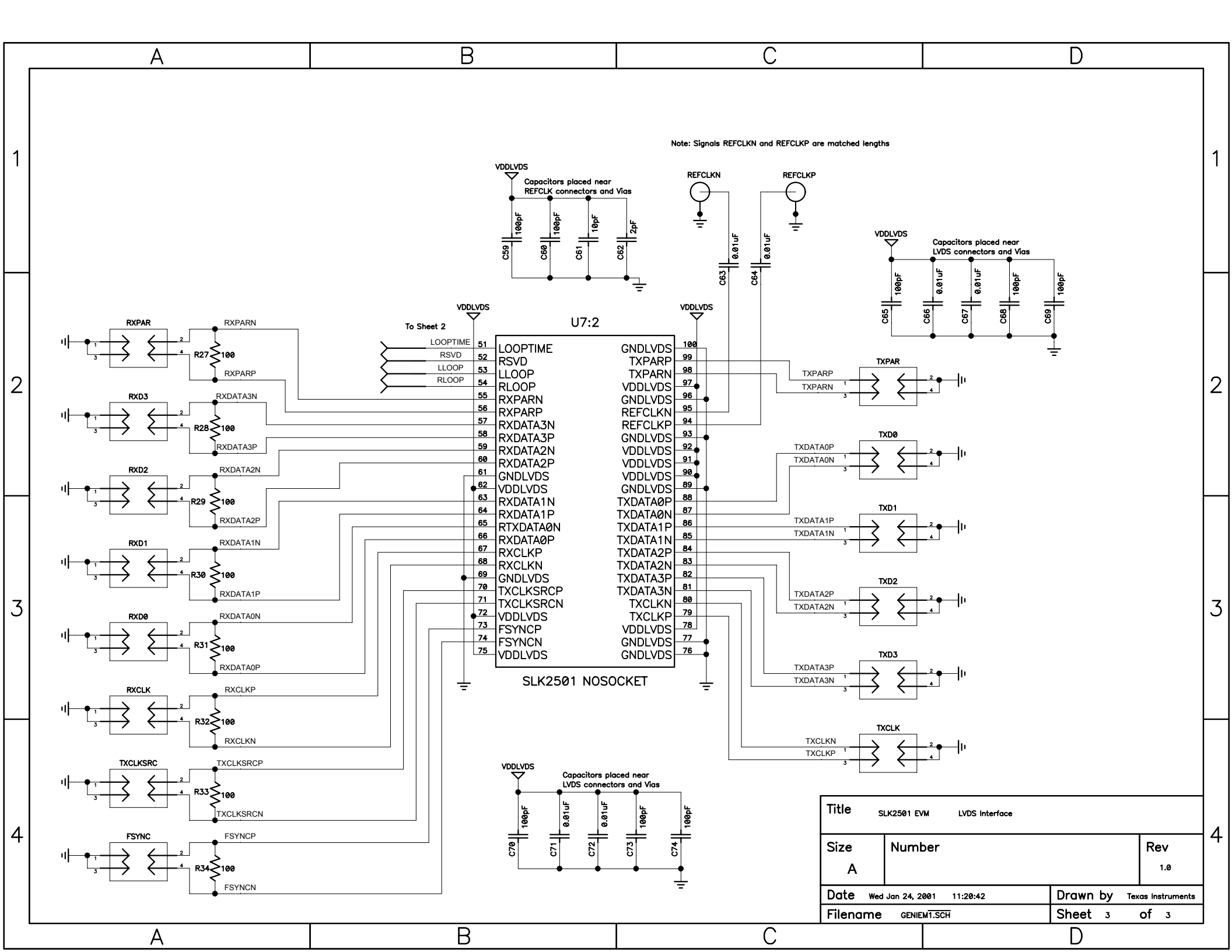


Decoupling General Guidelines:

1. Place capacitors such that smaller value capacitors are nearer the DUT and then successively place larger value capacitors as you move away form the DUT.

Title SLK2501 EVM Power		
Size A	Number	Rev 1.0
Date Wed Jan 24, 2001 11:20:42		Drawn by Texas Instruments
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U10
SCM6028-GL-ZN
VpdR
VeeR
VeeR
N/C
N/C
VeeR
VccR
SD
RDb
RD
Pmon+
Pmon-
Bmon+
Bmon-
VeeT
TDb
TD
Dis
VeeT
VccT
U7:1
SLK2501 NOSOCKET
JTI-MS100QFP14-0.50
GND
PAR_VALID
VDD
PRE1
PRE2
GND
VDDA
STXDON
STXDOP
GNDA
VDDPLL
GNDPLL
GNDA
SRXDIP
SRXDIN
VDDA
CONFIG0
CONFIG1
GND
SIGDET
PS
VDD
GND
LCKREFN
VDD
VDD
SPILL
RESET
RX_MONITOR
LOS
LOL
ENABLE
TESTEN
PRBSPASS
PRBS_EN
REFCLKSEL
RSEL0
RSEL1
RATEOUT0
RATEOUT1
VDD
AUTO_DETECT
GND
VDD
GND
GND
VDD
GND
FRAME_EN
GND
Par Valid
Outputs
Control Inputs
From Sheet 3
VDDA Capacitors placed near STXDO and SRXDI connectors and Vias
Title SLK2501 EVM Control Lines; Serial interface and optics
Size A
Number
Rev 1.0
Date Wed Jan 24, 2001 11:20:42
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Sheet 2 of 3


Note: Signals REFCLKN and REFCLKP are matched lengths
VDDLVDS
Capacitors placed near
REFCLK connectors and Vias
C59 100pF
C60 100pF
C61 10pF
C62 2pF
REFCLKN
REFCLKP
C63 0.01uF
C64 0.01uF
VDDLVDS
Capacitors placed near
LVDS connectors and Vias
C65 100pF
C66 0.01uF
C67 0.01uF
C68 100pF
C69 100pF
To Sheet 2
LOOPTIME
RSVD
LLOOP
RLOOP
U7:2
LOOPTIME 51
RSVD 52
LLOOP 53
RLOOP 54
RXPARN 55
RXPARP 56
RXDATA3N 57
RXDATA3P 58
RXDATA2N 59
RXDATA2P 60
GNDLVDS 61
VDDLVDS 62
RXDATA1N 63
RXDATA1P 64
RTXDATA0N 65
RXDATA0P 66
RXCLKP 67
RXCLKN 68
GNDLVDS 69
TXCLKSRCP 70
TXCLKSRCN 71
VDDLVDS 72
FSYNCP 73
FSYNCN 74
VDDLVDS 75
GNDLVDS 100
TXPARP 99
TXPARN 98
VDDLVDS 97
GNDLVDS 96
REFCLKN 95
REFCLKP 94
GNDLVDS 93
VDDLVDS 92
VDDLVDS 91
VDDLVDS 90
GNDLVDS 89
TXDATA0P 88
TXDATA0N 87
TXDATA1P 86
TXDATA1N 85
TXDATA2P 84
TXDATA2N 83
TXDATA3P 82
TXDATA3N 81
TXCLKN 80
TXCLKP 79
VDDLVDS 78
GNDLVDS 77
GNDLVDS 76
SLK2501 NOSOCKET
RXPAR
R27 100
RXPARN
RXPARP
RXD3
R28 100
RXDATA3N
RXDATA3P
RXD2
R29 100
RXDATA2N
RXDATA2P
RXD1
R30 100
RXDATA1N
RXDATA1P
RXD0
R31 100
RXDATA0N
RXDATA0P
RXCLK
R32 100
RXCLKP
RXCLKN
TXCLKSRC
R33 100
TXCLKSRCP
TXCLKSRCN
FSYNC
R34 100
FSYNCP
FSYNCN
TXPAR
TXPARP
TXPARN
TXD0
TXDATA0P
TXDATA0N
TXD1
TXDATA1P
TXDATA1N
TXD2
TXDATA2P
TXDATA2N
TXD3
TXDATA3P
TXDATA3N
TXCLK
TXCLKN
TXCLKP
VDDLVDS
Capacitors placed near
LVDS connectors and Vias
C70 100pF
C71 0.01uF
C72 0.01uF
C73 100pF
C74 100pF
Title SLK2501 EVM LVDS Interface
Size A
Number
Rev 1.0
Date Wed Jan 24, 2001 11:20:42
Drawn by Texas Instruments
Filename GENIEM1.SCH
Sheet 3 of 3

A.2 Bill of Materials

Table A–1 SLK2501EVM Transceiver Bill of Materials

COUNT	COMPONENT-NAME	REFDES	PATTERN NAME	VALUE	PART NUMBER	VENDOR	MAN. PART #	MAN.	DESCRIPTION
3	BJACK	J1, J3,J15	BJACK		J147–ND	Digi–Key	108–0740–001	Johnson Components	STANDARD BANANA JACK
34	CAP0402	C66, C67, C71, C72, C4, C23, C28, C33, C63, C64, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C38, C42, C43, C75, C76, C77, C78, C79, C80, C81C51, C52, C53, C54	402	0.01µF	PCC1738CT–ND	Digi–Key	ECJ–0EF1E103Z	Panasonic	CAP 10000PF 25V CERM Y5V 0402
4	OPEN	C47, C48, C49, C50	OPEN	——	——	——		Panasonic	
2	CAP0402	C58, C62	402	2pF	PCC020CQCT–ND	Digi–Key	ECJ–0EC1H020C	Panasonic	CAP 2.0PF 50V CERAMIC 0402 SMD
7	CAP0402	C6, C20, C25, C30, C35, C57, C61	402	10pF	PCC100CQCT–ND	Digi–Key	ECJ–0EC1H100D	Panasonic	CAP 10PF 50V CERAMIC 0402 SMD
15	CAP0402	C5, C19, C24, C29, C34, C55, C56, C59, C60, C65, C68, C69, C70, C73, C74	402	100pF	PCC101CQCT–ND	Digi–Key	ECJ–0EC1H101J	Panasonic	CAP 100PF 50V CERAMIC 0402 SMD
1	CAP0603	C41	603	0.1µF	PCC1762CT–ND	Digi–Key	ECJ–1VB1C104K	Panasonic	CAP .1UF 16V CERAMIC X7R 0603
2	CAP0805	C37, C44	805	1µF	PCC1807CT–ND	Digi–Key	ECJ–2YB1A105K	Panasonic	CAP 1UF 10V CERAMIC X7R 0805
5	CAP0805	C3, C8, C22, C27, C32	805	2.2µF	PCC1851CT–ND	Digi–Key	ECJ–2YF1C225Z	Panasonic	CAP 2.2UF 16V CERAMIC Y5V 0805
5	CAP0805	C2, C7, C21, C26, C31	805	4.7µF	PCC1842CT–ND	Digi–Key	ECJ–2YF1A475Z	Panasonic	CAP 4.7UF 10V CERAMIC Y5V 0805
6	CAP1206	C1, C36, C39, C40, C45, C46	1206	10µF	PCC1894CT–ND	Digi–Key	ECJ–3YF1A106Z	Panasonic	CAP 10UF 10V CERAMIC Y5V 1206

Table A–1 SLK2501EVM Transceiver Bill of Materials (continued)

COUNT	COMPONENT-NAME	REFDES	PATTERN NAME	VALUE	PART NUMBER	VEN-DOR	MAN. PART #	MAN.	DESCRIPTION
14	DRHDR4	FSYNC, RXCLK, RXD0, RXD1, RXD2, RXD3, RXPAR, TXCLK, TXCLKSRC, TXD0, TXD1, TXD2, TXD3, TXPAR	DRHDR4		S2011–04–ND	Digi–Key	PZC04DAAN	Sullins	ST DUAL ROW M HEADER GOLD 8 PIN
1	DRHDR12	U1	DRHDR12		S2011–12–ND	Digi–Key	PZC12DAAN	Sullins	ST DUAL ROW M HEADER GOLD 24 PIN
1	DRHDR18	U6	DRHDR18		S2011–18–ND	Digi–Key	PZC18DAAN	Sullins	ST DUAL ROW M HEADER GOLD 36 PIN
1	DRHDR24	U11	DRHDR24		S2011–24–ND	Digi–Key	PZC24DAAN	Sullins	ST DUAL ROW M HEADER GOLD 48 PIN
10	F–BEAD 0805	L1, L2, L3, L4, L5, L6, L7, L8, L9, L10	F–BEAD 0805		240–1018–1–ND	Digi–Key	HZ0805E601R–00	Steward	FERRITE SMT 0805 500MA 600 OHMS
1	LED SM	LED	LED SM		L62711CT–ND	Digi–Key	CMD28–21SRC/ TR8/T1		LED RED CLEAR LC GULL WING SMD
2	RES0402	R5, R36	402	0	P0.0JCT–ND	Digi–Key	ERJ–2GE0R00X	Panasonic	RES ZERO OHM 1/16W 5% 0402 SMD
1	RES0402	R35	402	1K	P1.00KLCT–ND	Digi–Key	ERJ–2RKF1001X	Panasonic	RES 1.00K OHM 1/16W 1% 0402 SMD
22	RES0402	R2, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26	402	4.75k	P4.75KLCT–ND	Digi–Key	ERJ–2RKF4751X	Panasonic	RES 4.75K OHM 1/16W 1% 0402 SMD
9	RES0402	R1, R27, R28, R29, R30, R31, R32, R33, R34	402	100	P100LCT–ND	Digi–Key	ERJ–2RKF1000X	Panasonic	RES 100 OHM 1/16W 1% 0402 SMD
2	RES0402	R3, R4	402	243	P243LCT–ND	Digi–Key	ERJ–2RKF2430X	Panasonic	RES 243 OHM 1/16W 1% 0402 SMD

Table A–1 SLK2501EVM Transceiver Bill of Materials (continued)

COUNT	COMPONENT-NAME	REFDES	PATTERN NAME	VALUE	PART NUMBER	VENDOR	MAN. PART #	MAN.	DESCRIPTION
1	SCM6028–GL–ZN	U10	SCM6028–GL–ZN		SCM6028–GL–ZN	Sumitomo		Sumitomo	
1	SLK2501	U7	SLK2501		SLK2501	Texas Instruments		Texas Instruments	
6	SMA THROUGH HOLE	REFCLKN1, REFCLKP1, J7, 78, J10, J6	SMA_TH		J608–ND	Digi–Key	142–0701–231	Johnson Components	CONN SMA JACK PCB VERT .110 LEGS
7	SRHDR2	U8, U12, U9, J2, J4, J9, J5	SRHDR2		S1011–02–ND	Digi–Key	PZC02SAAN	Sullins	ST SINGLE M HEADER GOLD 02 POS
4	SRHDR3	U2, U3, U4, U5	SRHDR3		S1011–03–ND	Digi–Key	PZC03SAAN	Sullins	ST SINGLE M HEADER GOLD 03 POS
4	STANDOFF				4830K–ND	Digi–Key	4830	Keystone Electronics	STANDOFF M/F HX NYLON 8/32 .500”
4	MACHINE SCREW				H146–ND	Digi–Key	PMS 440 0050 SL	Building Fasteners	4–40X1/2 MACHINE SCREW

Total Part Count: 155

Note: For this board design RREF(R34) was chosen to be 100 ohms to optimize performance across a wide range of interconnect systems. TI recommends starting with a RREF value of 200 ohms and adjusting this value, by using the data sheet formulas, as necessary to achieve desired output swings and optimal performance.

A.3 Board Layouts

Figure A–4. Top Layer 1

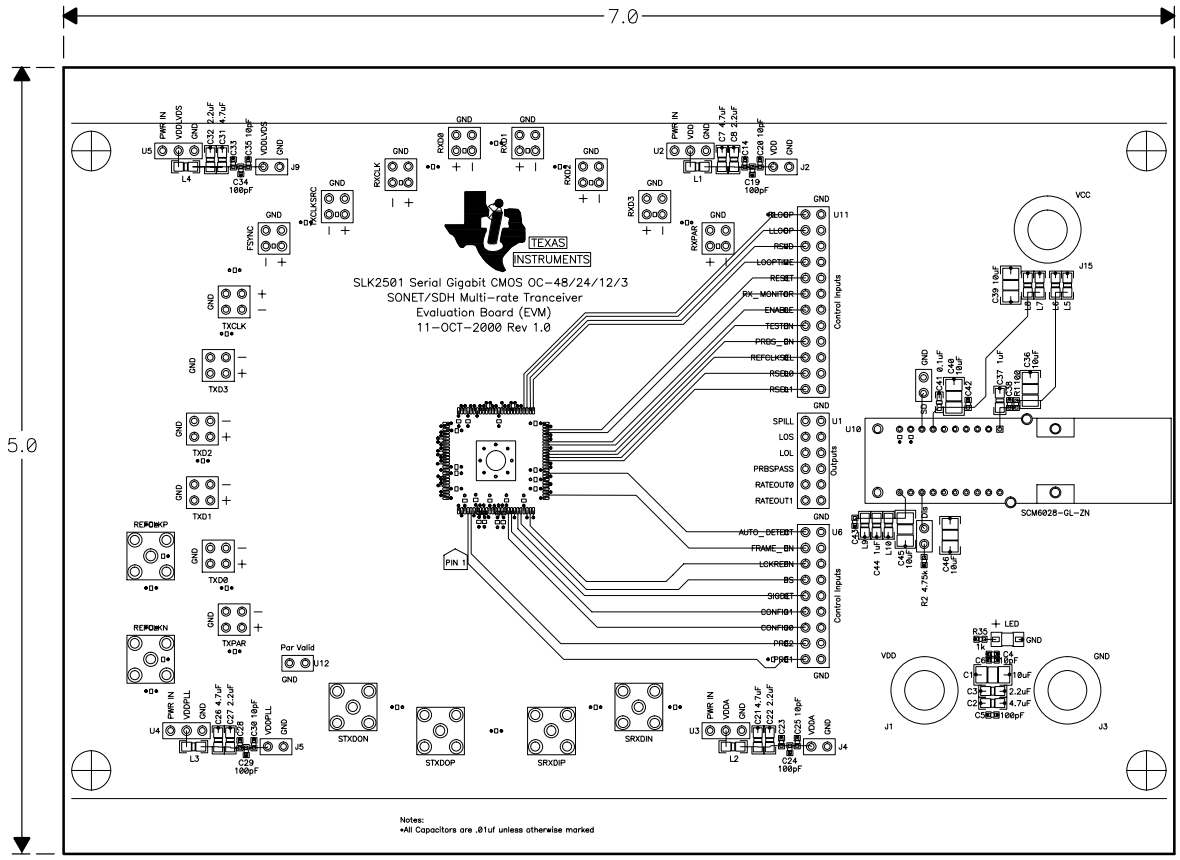


Figure A–5. GND Layers 2 and 4

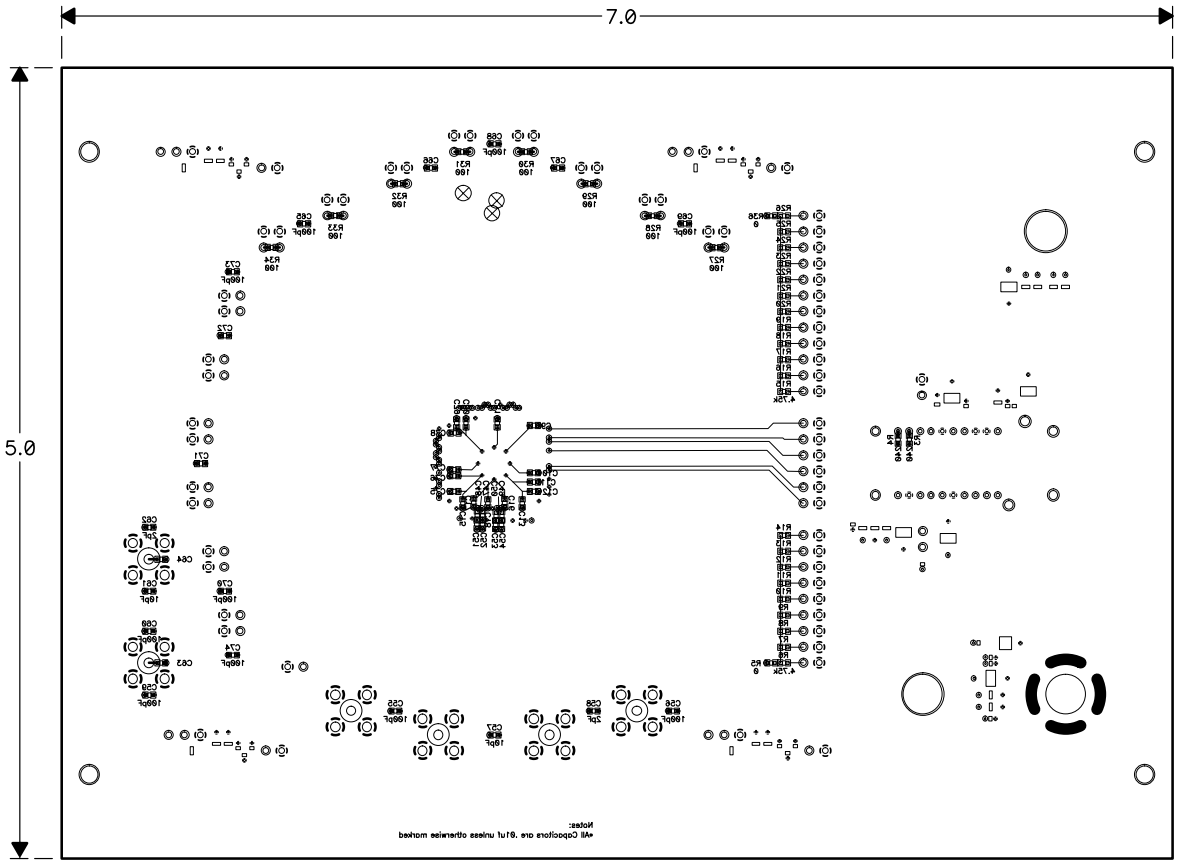


Figure A–6. LVDS Layer 3

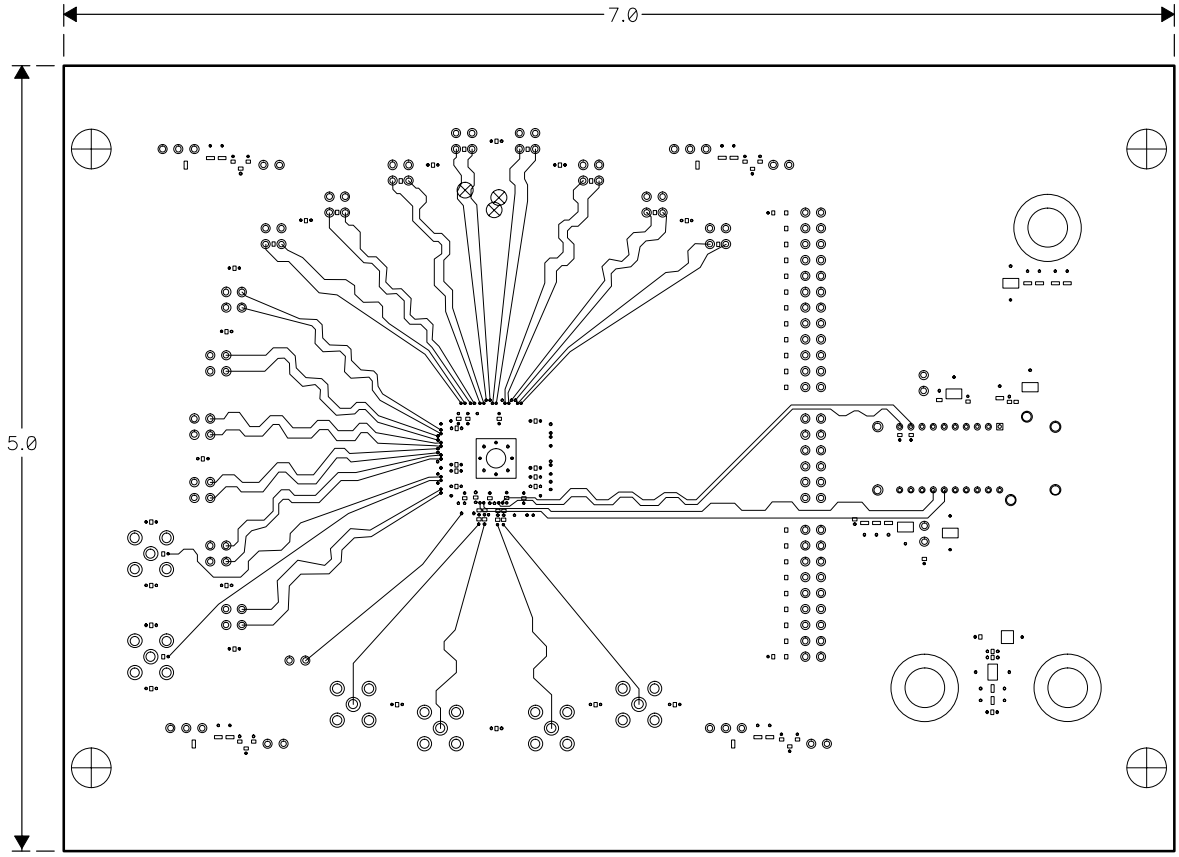


Figure A–7. Power Plane Layer 5

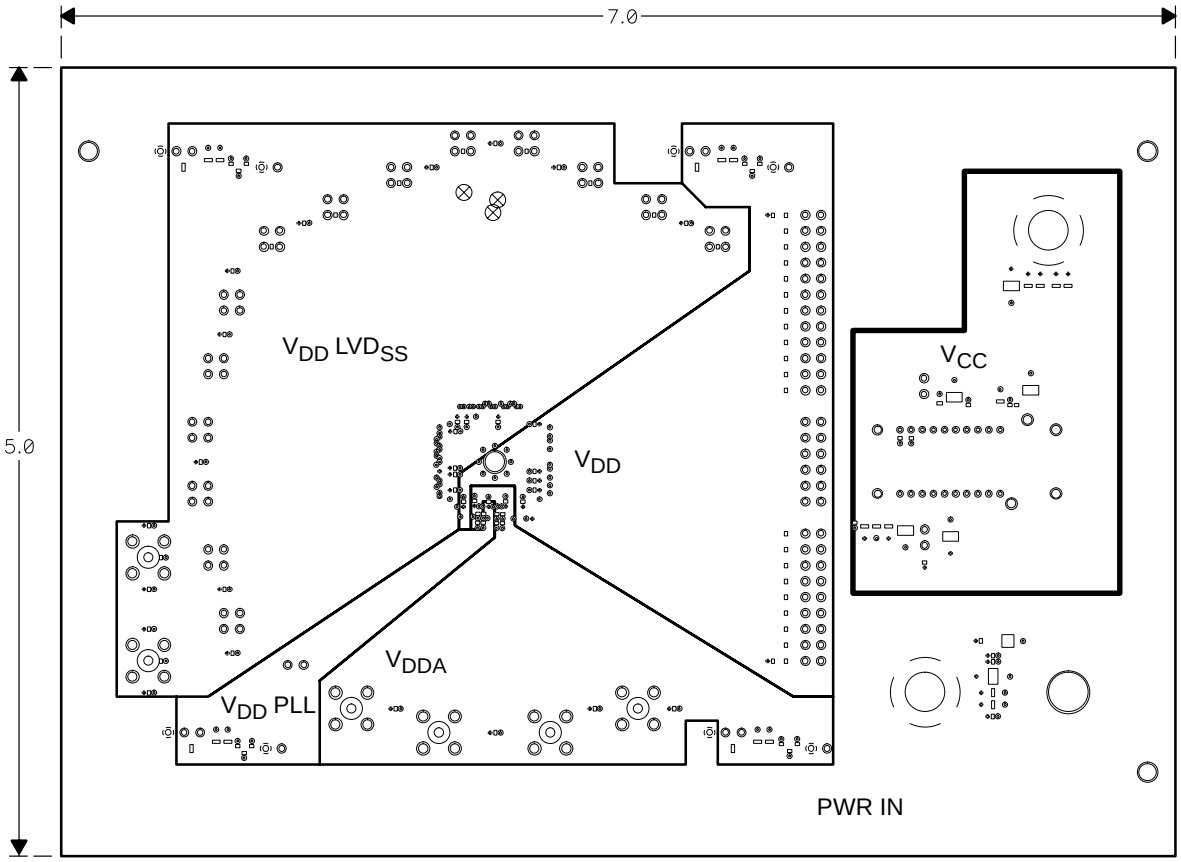


Figure A–8. Bottom Layer 6

