# SN74AUP1G125 Low-Power Single Bus Buffer Gate With 3-State Output

## 1 Features

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ($I_{CC}$ = 0.9 µA Maximum)
- Low Dynamic-Power Consumption ($C_{pd}$ = 4 pF Typical at 3.3 V)
- Low Input Capacitance ($C_I$ = 1.5 pF Typical)
- Low Noise – Overshoot and Undershoot < 10% of $V_{CC}$
- Input-Disable Feature Allows Floating Input Conditions
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input
- Wide Operating $V_{CC}$ Range of 0.8 V to 3.6 V
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd}$ = 4.6 ns Maximum at 3.3 V

## 2 Applications

- Audio Dock: Portable
- BluRay™ Players and Home Theaters
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid-State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Wireless Headsets, Keyboards, and Mice

## 3 Description

The SN74AUP1G125 bus buffer gate is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high. This device has the input-disable feature, which allows floating input signals.

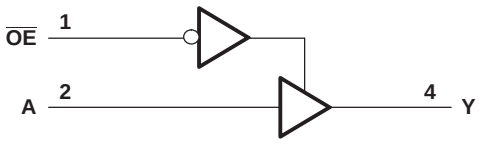
To ensure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74AUP1G125DBV | SOT-23 (5) | 2.90 mm × 1.60 mm |
| SN74AUP1G125DCK | SC70 (5) | 2.00 mm × 1.25 mm |
| SN74AUP1G125DRL | SOT (5) | 1.60 mm × 1.20 mm |
| SN74AUP1G125DRY | SON (6) | 1.45 mm × 1.00 mm |
| SN74AUP1G125DSF | | 1.00 mm × 1.00 mm |
| SN74AUP1G125YFP | DSBGA (6) | 0.76 mm × 1.16 mm |
| SN74AUP1G125YZP | DSBGA (5) | 0.89 mm × 1.39 mm |
| SN74AUP1G125YZT | DSBGA (5) | 0.89 mm × 1.39 mm |
| SN74AUP1G125DPW | X2SON (5) | 0.80 mm × 0.80 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**

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## Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics, $T_A$ = 25°C ... 6
6.6 Electrical Characteristics, $T_A$ = –40°C to +85°C ... 7
6.7 Switching Characteristics, $C_L$ = 5 pF ... 8
6.8 Switching Characteristics, $C_L$ = 10 pF ... 9
6.9 Switching Characteristics, $C_L$ = 15 pF ... 10
6.10 Switching Characteristics, $C_L$ = 30 pF ... 11
6.11 Operating Characteristics ... 12
6.12 Typical Characteristics ... 12
7 Parameter Measurement Information ... 13
8 Detailed Description ... 15
8.1 Overview ... 15
8.2 Functional Block Diagram ... 15
8.3 Feature Description ... 15
8.4 Device Functional Modes ... 16
9 Application and Implementation ... 17
9.1 Application Information ... 17
9.2 Typical Application ... 17
10 Power Supply Recommendations ... 18
11 Layout ... 18
11.1 Layout Guidelines ... 18
11.2 Layout Example ... 18
12 Device and Documentation Support ... 20
12.1 Documentation Support ... 20
12.2 Receiving Notification of Documentation Updates 20
12.3 Community Resources ... 20
12.4 Trademarks ... 20
12.5 Electrostatic Discharge Caution ... 20
12.6 Glossary ... 20
13 Mechanical, Packaging, and Orderable Information ... 20

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision M (December 2015) to Revision N** — **Page**

- Added DPW (X2SON) package ... 1
- Deleted *Device Comparison* table, see *Mechanical, Packaging, and Orderable Information* section at the end of the data sheet ... 1
- Changed *Simplified Schematic* with a new schematic ... 1
- Added column for X2SON (DPW) package and separated columns for DSBGA packages in *Pin Functions* table ... 3
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 5
- Added *Balanced High-Drive CMOS Push-Pull Outputs*, *Standard CMOS Inputs*, *Clamp Diodes*, *Partial Power Down* ($I_{off}$), and *Over-voltage Tolerant Inputs* ... 15
- Added *Trace Example* and revised *Layout Guidelines* ... 18
- Added *Receiving Notification of Documentation Updates* section ... 20

**Changes from Revision L (February 2013) to Revision M** — **Page**

- Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

**Changes from Revision K (November 2012) to Revision L** — **Page**

- Changed $\overline{Y}$ to Y for pin 4 in DSF Package pin out ... 3


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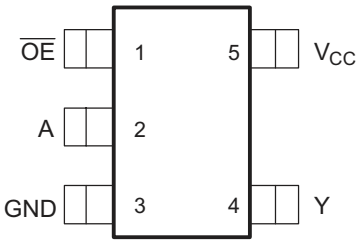
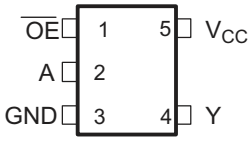
# 5 Pin Configuration and Functions

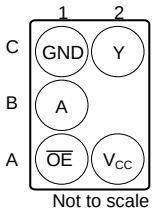
**DBV Package**
**5-Pin SOT-23**
**Top View**




**DRL Package**
**5-Pin SOT**
**Top View**

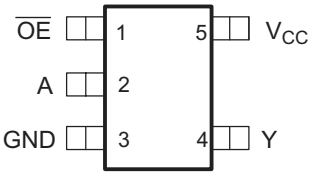



**YZP or YZT Package**
**5-Pin DSBGA**
**Bottom View**

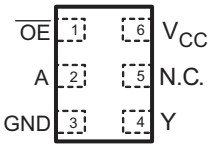



Not to scale

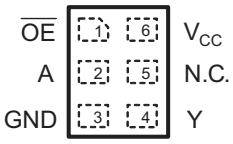
**DCK Package**
**5-Pin SC70**
**Top View**



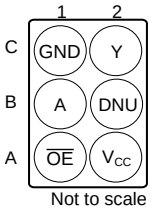

**DSF Package**
**6-Pin SON**
**Top View**




**DRY Package**
**6-Pin SON**
**Top View**

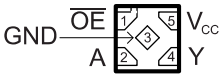



**YFP Package**
**6-Pin DSBGA**
**Bottom View**




Not to scale

**DPW Package**
**5-Pin X2SON**
**Top View**




**Pin Functions**

| PIN | | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|---|
| NAME | SOT-23 (DBV), SC70 (DCK), SOT (DRL), X2SON (DPW) | SON (DRY or DSF) | DSBGA (YZP or YZT) | DSBGA (YFP) | | |
| A | 2 | 2 | B1 | B1 | I | Input |
| DNU | — | — | — | B2 | — | Do not use |
| GND | 3 | 3 | C1 | C1 | — | Ground |
| N.C. | — | 5 | — | — | — | No connection |
| $\overline{OE}$ | 1 | 1 | A1 | A1 | I | Output enable (active low) |
| $V_{CC}$ | 5 | 6 | A2 | A2 | — | Positive supply |
| Y | 4 | 4 | C2 | C2 | O | Output |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 4.6 | V |
| $V_I$ | Input voltage(2) | | –0.5 | 4.6 | V |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state(2) | | –0.5 | 4.6 | V |
| $V_O$ | Output voltage in the high or low state(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±20 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | 2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.


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## 6.3 Recommended Operating Conditions

See (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 0.8 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 0.8 V | $V_{CC}$ | 3.6 | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | 0.65 × $V_{CC}$ | 3.6 | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.6 | 3.6 | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | 3.6 | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 0.8 V | | 0 | V |
| | | $V_{CC}$ = 1.1 V to 1.95 V | 0 | 0.35 × $V_{CC}$ | |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0 | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | 0 | 0.9 | |
| $V_O$ | Output voltage | Active state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 3.6 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 0.8 V | | –20 | μA |
| | | $V_{CC}$ = 1.1 V | | –1.1 | mA |
| | | $V_{CC}$ = 1.4 V | | –1.7 | |
| | | $V_{CC}$ = 1.65 V | | –1.9 | |
| | | $V_{CC}$ = 2.3 V | | –3.1 | |
| | | $V_{CC}$ = 3 V | | –4 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 0.8 V | | 20 | μA |
| | | $V_{CC}$ = 1.1 V | | 1.1 | mA |
| | | $V_{CC}$ = 1.4 V | | 1.7 | |
| | | $V_{CC}$ = 1.65 V | | 1.9 | |
| | | $V_{CC}$ = 2.3 V | | 3.1 | |
| | | $V_{CC}$ = 3 V | | 4 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 0.8 V to 3.6 V | | 200 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See the TI application report, *Implications of Slow of Floating CMOS Inputs*, SCBA004.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74AUP1G125 | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | DCK (SC70) | DBV (SOT-23) | DRL (SOT) | DRY (SON) | DSF (SON) | YFP (DSBGA) | YZP (DSBGA) | DPW (X2SON) | |
| | | 5 PINS | 5 PINS | 5 PINS | 6 PINS | 6 PINS | 6 PINS | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 303.6 | 230.5 | 295.1 | 342.1 | 377.1 | 125.4 | 146.2 | 504.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 203.8 | 172.7 | 131.0 | 233.1 | 187.7 | 1.9 | 1.4 | 234.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 100.9 | 62.2 | 143.9 | 206.7 | 236.6 | 37.2 | 39.3 | 370.3 | °C/W |
| $\psi_{\theta Jt}$ | Junction-to-top characterization parameter | 76.1 | 49.3 | 14.7 | 63.4 | 29.0 | 0.5 | 0.7 | 44.5 | °C/W |
| $\psi_{\theta JB}$ | Junction-to-board characterization parameter | 99.3 | 61.6 | 144.4 | 206.7 | 236.3 | 37.5 | 39.8 | 369.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | N/A | N/A | N/A | 165.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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## 6.5 Electrical Characteristics, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –20 µA | 0.8 V to 3.6 V | $V_{CC}$ – 0.1 | | | V |
| | | $I_{OH}$ = –1.1 mA | 1.1 V | 0.75 × $V_{CC}$ | | | |
| | | $I_{OH}$ = –1.7 mA | 1.4 V | 1.11 | | | |
| | | $I_{OH}$ = –1.9 mA | 1.65 V | 1.32 | | | |
| | | $I_{OH}$ = –2.3 mA | 2.3 V | 2.05 | | | |
| | | $I_{OH}$ = –3.1 mA | | 1.9 | | | |
| | | $I_{OH}$ = –2.7 mA | 3 V | 2.72 | | | |
| | | $I_{OH}$ = –4 mA | | 2.6 | | | |
| $V_{OL}$ | | $I_{OL}$ = 20 µA | 0.8 V to 3.6 V | | | 0.1 | V |
| | | $I_{OL}$ = 1.1 mA | 1.1 V | | | 0.3 × $V_{CC}$ | |
| | | $I_{OL}$ = 1.7 mA | 1.4 V | | | 0.31 | |
| | | $I_{OL}$ = 1.9 mA | 1.65 V | | | 0.31 | |
| | | $I_{OL}$ = 2.3 mA | 2.3 V | | | 0.31 | |
| | | $I_{OL}$ = 3.1 mA | | | | 0.44 | |
| | | $I_{OL}$ = 2.7 mA | 3 V | | | 0.31 | |
| | | $I_{OL}$ = 4 mA | | | | 0.44 | |
| $I_I$ | A or $\overline{OE}$ input | $V_I$ = GND to 3.6 V | 0 V to 3.6 V | | | 0.1 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 0 V to 3.6 V | 0 V | | | 0.2 | µA |
| $\Delta I_{off}$ | | $V_I$ or $V_O$ = 0 V to 3.6 V | 0 V to 0.2 V | | | 0.2 | µA |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND | 3.6 V | | | 0.1 | µA |
| $I_{CC}$ | | $V_I$ = GND or ($V_{CC}$ to 3.6 V), $\overline{OE}$ = GND, $I_O$ = 0 | 0.8 V to 3.6 V | | | 0.5 | µA |
| $\Delta I_{CC}$ | A input | $V_I$ = $V_{CC}$ – 0.6 V[1], $I_O$ = 0 | 3.3 V | | | 40 | µA |
| | $\overline{OE}$ input | | | | | 110 | |
| | All inputs | $V_I$ = GND to 3.6 V, $\overline{OE}$ = $V_{CC}$ [2] | 0.8 V to 3.6 V | | | 0 | |
| $C_I$ | | $V_I$ = $V_{CC}$ or GND | 0 V | | 1.5 | | pF |
| | | | 3.6 V | | 1.5 | | |
| $C_o$ | | $V_O$ = $V_{CC}$ or GND | 3.6 V | | 3 | | pF |

(1) One input at $V_{CC}$ – 0.6 V, other input at $V_{CC}$ or GND
(2) To show $I_{CC}$ is very low when the input-disable feature is enabled


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## 6.6 Electrical Characteristics, $T_A$ = –40°C to +85°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = –20 µA | 0.8 V to 3.6 V | $V_{CC}$ – 0.1 | | | V |
| | | $I_{OH}$ = –1.1 mA | 1.1 V | 0.7 × $V_{CC}$ | | | |
| | | $I_{OH}$ = –1.7 mA | 1.4 V | 1.03 | | | |
| | | $I_{OH}$ = –1.9 mA | 1.65 V | 1.3 | | | |
| | | $I_{OH}$ = –2.3 mA | 2.3 V | 1.97 | | | |
| | | $I_{OH}$ = –3.1 mA | | 1.85 | | | |
| | | $I_{OH}$ = –2.7 mA | 3 V | 2.67 | | | |
| | | $I_{OH}$ = –4 mA | | 2.55 | | | |
| $V_{OL}$ | | $I_{OL}$ = 20 µA | 0.8 V to 3.6 V | | | 0.1 | V |
| | | $I_{OL}$ = 1.1 mA | 1.1 V | | | 0.3 × $V_{CC}$ | |
| | | $I_{OL}$ = 1.7 mA | 1.4 V | | | 0.37 | |
| | | $I_{OL}$ = 1.9 mA | 1.65 V | | | 0.35 | |
| | | $I_{OL}$ = 2.3 mA | 2.3 V | | | 0.33 | |
| | | $I_{OL}$ = 3.1 mA | | | | 0.45 | |
| | | $I_{OL}$ = 2.7 mA | 3 V | | | 0.33 | |
| | | $I_{OL}$ = 4 mA | | | | 0.45 | |
| $I_I$ | A or $\overline{OE}$ input | $V_I$ = GND to 3.6 V | 0 V to 3.6 V | | | 0.5 | µA |
| $I_{off}$ | | $V_I$ or $V_O$ = 0 V to 3.6 V | 0 V | | | 0.6 | µA |
| $\Delta I_{off}$ | | $V_I$ or $V_O$ = 0 V to 3.6 V | 0 V to 0.2 V | | | 0.6 | µA |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND | 3.6 V | | | 0.5 | µA |
| $I_{CC}$ | | $V_I$ = GND or ($V_{CC}$ to 3.6 V), $\overline{OE}$ = GND, $I_O$ = 0 | 0.8 V to 3.6 V | | | 0.9 | µA |
| $\Delta I_{CC}$ | A input | $V_I$ = $V_{CC}$ – 0.6 V[1], $I_O$ = 0 | 3.3 V | | | 50 | µA |
| | $\overline{OE}$ input | | | | | 120 | |
| | All inputs | $V_I$ = GND to 3.6 V, $\overline{OE}$ = $V_{CC}$ [2] | 0.8 V to 3.6 V | | | 0 | |

(1) One input at $V_{CC}$ – 0.6 V, other input at $V_{CC}$ or GND
(2) To show $I_{CC}$ is very low when the input-disable feature is enabled

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## 6.7 Switching Characteristics, $C_L$ = 5 pF

over recommended operating free-air temperature range, $C_L$ = 5 pF (unless otherwise noted) (see Figure 2 and Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A | Y | 0.8 V | $T_A$ = 25°C | | 18.1 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 4.3 | 7.4 | 12.6 | |
| | | | | $T_A$ = –40°C to +85°C | 2.7 | | 15.3 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 3.3 | 5.2 | 8.5 | |
| | | | | $T_A$ = –40°C to +85°C | 1 | | 10.2 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 2.6 | 4.1 | 6.8 | |
| | | | | $T_A$ = –40°C to +85°C | 1.3 | | 8.3 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 2 | 2.9 | 4.7 | |
| | | | | $T_A$ = –40°C to +85°C | 1.1 | | 5.8 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 1.7 | 2.4 | 3.8 | |
| | | | | $T_A$ = –40°C to +85°C | 1 | | 4.6 | |
| $t_{en}$ | $\overline{OE}$ | Y | 0.8 V | $T_A$ = 25°C | | 19.1 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 5.1 | 9.3 | 15.9 | |
| | | | | $T_A$ = –40°C to +85°C | 3.6 | | 19.2 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 4.1 | 6.6 | 10.5 | |
| | | | | $T_A$ = –40°C to +85°C | 2.5 | | 12.7 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 3.2 | 5.3 | 8.7 | |
| | | | | $T_A$ = –40°C to +85°C | 2.1 | | 10.3 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 2.5 | 3.8 | 6 | |
| | | | | $T_A$ = –40°C to +85°C | 1.6 | | 7.2 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 2.1 | 3.2 | 4.9 | |
| | | | | $T_A$ = –40°C to +85°C | 1.4 | | 5.9 | |
| $t_{dis}$ | $\overline{OE}$ | Y | 0.8 V | $T_A$ = 25°C | | 12.1 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 2.4 | 4.1 | 6.9 | |
| | | | | $T_A$ = –40°C to +85°C | 2.2 | | 7.7 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 1.8 | 2.9 | 4.5 | |
| | | | | $T_A$ = –40°C to +85°C | 1.7 | | 5.1 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 1 | 2.9 | 4.3 | |
| | | | | $T_A$ = –40°C to +85°C | 1.5 | | 4.7 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 1 | 1.8 | 2.7 | |
| | | | | $T_A$ = –40°C to +85°C | 1 | | 3.3 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 1.2 | 2.2 | 3.2 | |
| | | | | $T_A$ = –40°C to +85°C | 1.1 | | 4 | |


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## 6.8 Switching Characteristics, $C_L$ = 10 pF

over recommended operating free-air temperature range, $C_L$ = 10 pF (unless otherwise noted) (see Figure 2 and Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A or B | Y | 0.8 V | $T_A$ = 25°C | | 20.5 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 4.6 | 8.4 | 13.7 | |
| | | | | $T_A$ = –40°C to +85°C | 3.6 | | 16.6 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 3.5 | 5.9 | 9.3 | |
| | | | | $T_A$ = –40°C to +85°C | 2.4 | | 11.1 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 3.9 | 4.7 | 7.5 | |
| | | | | $T_A$ = –40°C to +85°C | 1.3 | | 9.1 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 2.3 | 3.4 | 5.3 | |
| | | | | $T_A$ = –40°C to +85°C | 1.6 | | 6.4 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 2.1 | 2.8 | 4.3 | |
| | | | | $T_A$ = –40°C to +85°C | 1.4 | | 5.2 | |
| $t_{en}$ | $\overline{OE}$ | Y | 0.8 V | $T_A$ = 25°C | | 21.8 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 4.9 | 10.2 | 16.8 | |
| | | | | $T_A$ = –40°C to +85°C | 4.4 | | 20.2 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 3.9 | 7.3 | 11.2 | |
| | | | | $T_A$ = –40°C to +85°C | 3.3 | | 13.5 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 3.4 | 5.8 | 9.2 | |
| | | | | $T_A$ = –40°C to +85°C | 2.7 | | 11 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 2.5 | 4.3 | 6.4 | |
| | | | | $T_A$ = –40°C to +85°C | 2.1 | | 7.8 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 2.1 | 3.7 | 5.4 | |
| | | | | $T_A$ = –40°C to +85°C | 1.9 | | 6.4 | |
| $t_{dis}$ | $\overline{OE}$ | Y | 0.8 V | $T_A$ = 25°C | | 13 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 3.8 | 6.6 | 11.7 | |
| | | | | $T_A$ = –40°C to +85°C | 1.2 | | 14 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 2.2 | 4.7 | 7.9 | |
| | | | | $T_A$ = –40°C to +85°C | 1.3 | | 9.3 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 2.4 | 4.4 | 6.4 | |
| | | | | $T_A$ = –40°C to +85°C | 2.2 | | 7.5 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 1.3 | 3.1 | 4.9 | |
| | | | | $T_A$ = –40°C to +85°C | 1.2 | | 5.4 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 1.9 | 3.4 | 5 | |
| | | | | $T_A$ = –40°C to +85°C | 1.9 | | 5.6 | |

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## 6.9 Switching Characteristics, $C_L$ = 15 pF

over recommended operating free-air temperature range, $C_L$ = 15 pF (unless otherwise noted) (see Figure 2 and Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A or B | Y | 0.8 V | $T_A$ = 25°C | | 22.5 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 5.8 | 9.3 | 15.1 | |
| | | | | $T_A$ = –40°C to +85°C | 4.3 | | 17.9 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 4.4 | 6.6 | 10.2 | |
| | | | | $T_A$ = –40°C to +85°C | 3 | | 12.1 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 3.5 | 5.3 | 8.3 | |
| | | | | $T_A$ = –40°C to +85°C | 2.3 | | 9.9 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 2.7 | 3.9 | 5.8 | |
| | | | | $T_A$ = –40°C to +85°C | 1.9 | | 7 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 2.4 | 3.2 | 4.7 | |
| | | | | $T_A$ = –40°C to +85°C | 1.8 | | 5.7 | |
| $t_{en}$ | $\overline{OE}$ | Y | 0.8 V | $T_A$ = 25°C | | 25.2 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 7 | 11.3 | 18.1 | |
| | | | | $T_A$ = –40°C to +85°C | 5.4 | | 21.4 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 5.5 | 8.1 | 12.2 | |
| | | | | $T_A$ = –40°C to +85°C | 4.1 | | 14.5 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 4.3 | 6.5 | 10.1 | |
| | | | | $T_A$ = –40°C to +85°C | 3.3 | | 12 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 3.4 | 4.8 | 7.1 | |
| | | | | $T_A$ = –40°C to +85°C | 2.6 | | 8.4 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 2.9 | 4.1 | 5.9 | |
| | | | | $T_A$ = –40°C to +85°C | 2.3 | | 6.9 | |
| $t_{dis}$ | $\overline{OE}$ | Y | 0.8 V | $T_A$ = 25°C | | 14 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 3.7 | 5.8 | 8.2 | |
| | | | | $T_A$ = –40°C to +85°C | 3.3 | | 11 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 5.5 | 3.9 | 5.9 | |
| | | | | $T_A$ = –40°C to +85°C | 2.1 | | 8 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 3.3 | 4.5 | 6.6 | |
| | | | | $T_A$ = –40°C to +85°C | 2.9 | | 7.4 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 2.3 | 3.2 | 4.3 | |
| | | | | $T_A$ = –40°C to +85°C | 1.8 | | 5.1 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 2.4 | 4.8 | 6.2 | |
| | | | | $T_A$ = –40°C to +85°C | 3.1 | | 6.7 | |


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## 6.10 Switching Characteristics, $C_L$ = 30 pF

over recommended operating free-air temperature range, $C_L$ = 30 pF (unless otherwise noted) (see Figure 2 and Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{pd}$ | A or B | Y | 0.8 V | $T_A$ = 25°C | | 29 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 7.4 | 12 | 18.7 | |
| | | | | $T_A$ = –40°C to +85°C | 6.6 | | 21.4 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 5.7 | 8.6 | 12.5 | |
| | | | | $T_A$ = –40°C to +85°C | 4.9 | | 14.7 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 4.8 | 6.9 | 10.1 | |
| | | | | $T_A$ = –40°C to +85°C | 3.1 | | 12 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 3.9 | 5.1 | 7.2 | |
| | | | | $T_A$ = –40°C to +85°C | 3.3 | | 8.7 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 3.5 | 4.8 | 6 | |
| | | | | $T_A$ = –40°C to +85°C | 3 | | 7 | |
| $t_{en}$ | $\overline{OE}$ | Y | 0.8 V | $T_A$ = 25°C | | 33.4 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 8.8 | 14.1 | 21.8 | |
| | | | | $T_A$ = –40°C to +85°C | 7.4 | | 25.5 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 6.9 | 10.1 | 14.6 | |
| | | | | $T_A$ = –40°C to +85°C | 5.6 | | 17.4 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 5.6 | 8.1 | 12 | |
| | | | | $T_A$ = –40°C to +85°C | 4.7 | | 14.1 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 4.3 | 6.1 | 8.5 | |
| | | | | $T_A$ = –40°C to +85°C | 3.8 | | 10 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 3.7 | 5.2 | 7.1 | |
| | | | | $T_A$ = –40°C to +85°C | 3.4 | | 8.3 | |
| $t_{dis}$ | $\overline{OE}$ | Y | 0.8 V | $T_A$ = 25°C | | 17.7 | | ns |
| | | | 1.2 V ± 0.1 V | $T_A$ = 25°C | 5.8 | 10 | 16 | |
| | | | | $T_A$ = –40°C to +85°C | 3.7 | | 16 | |
| | | | 1.5 V ± 0.1 V | $T_A$ = 25°C | 5.7 | 7.7 | 10.9 | |
| | | | | $T_A$ = –40°C to +85°C | 1 | | 10.7 | |
| | | | 1.8 V ± 0.15 V | $T_A$ = 25°C | 4.5 | 7.7 | 9.8 | |
| | | | | $T_A$ = –40°C to +85°C | 4.4 | | 12.5 | |
| | | | 2.5 V ± 0.2 V | $T_A$ = 25°C | 3.9 | 5.6 | 7.4 | |
| | | | | $T_A$ = –40°C to +85°C | 3.2 | | 9 | |
| | | | 3.3 V ± 0.3 V | $T_A$ = 25°C | 3.3 | 8.4 | 10.7 | |
| | | | | $T_A$ = –40°C to +85°C | 6.6 | | 10.8 | |

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## 6.11 Operating Characteristics

$T_A$ = 25°c

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | f = 10 MHz | 0.8 V | 3.8 | pF |
| | | | | 1.2 V ± 0.1 V | 3.8 | |
| | | | | 1.5 V ± 0.1 V | 3.7 | |
| | | | | 1.8 V ± 0.15 V | 3.8 | |
| | | | | 2.5 V ± 0.2 V | 3.9 | |
| | | | | 3.3 V ± 0.3 V | 4 | |
| | | Outputs disabled | f = 10 MHz | 0.8 V | 0 | |
| | | | | 1.2 V ± 0.1 V | 0 | |
| | | | | 1.5 V ± 0.1 V | 0 | |
| | | | | 1.8 V ± 0.15 V | 0 | |
| | | | | 2.5 V ± 0.2 V | 0 | |
| | | | | 3.3 V ± 0.3 V | 0 | |

## 6.12 Typical Characteristics

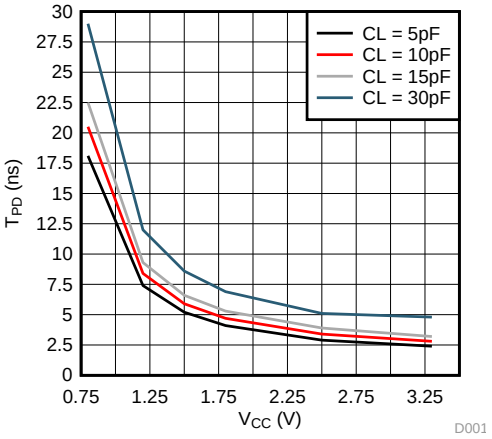


**Figure 1. Propagation Delay vs. Supply Voltage and Load Capacitance**


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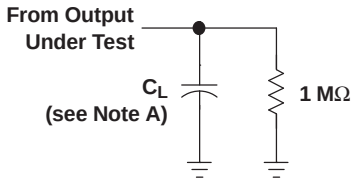
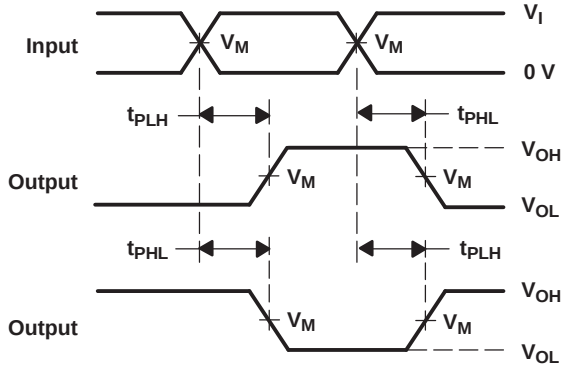
# 7 Parameter Measurement Information

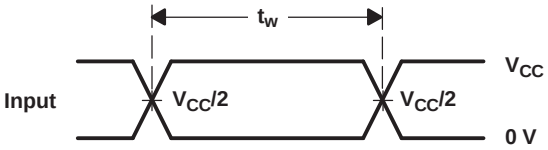



**LOAD CIRCUIT**

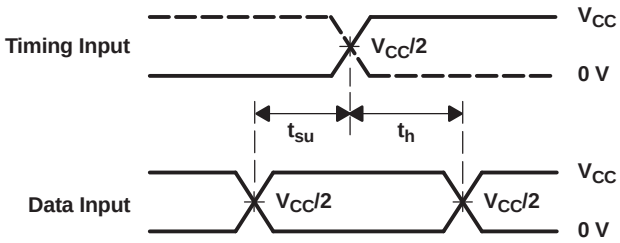
| | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | $V_{CC}$ = 1.5 V ± 0.1 V | $V_{CC}$ = 1.8 V ± 0.15 V | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V |
|---|---|---|---|---|---|---|
| $C_L$ | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| $V_M$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_I$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |




**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**
**INVERTING AND NONINVERTING OUTPUTS**




**VOLTAGE WAVEFORMS**
**PULSE DURATION**




**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
E. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

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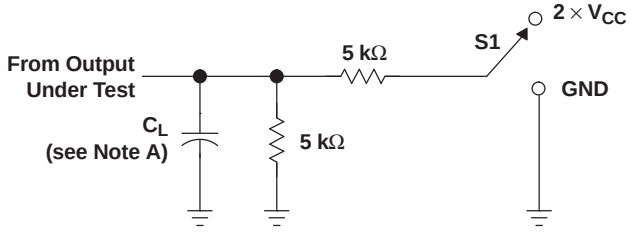
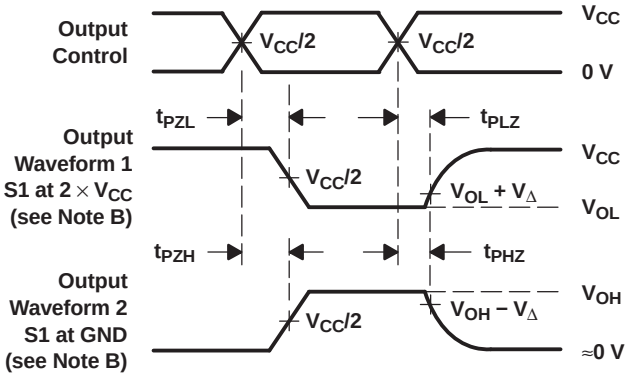
## Parameter Measurement Information (continued)




LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | 2 × $V_{CC}$<br>GND |

| | $V_{CC}$ = 0.8 V | $V_{CC}$ = 1.2 V ± 0.1 V | $V_{CC}$ = 1.5 V ± 0.1 V | $V_{CC}$ = 1.8 V ± 0.15 V | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V |
|---|---|---|---|---|---|---|
| $C_L$ | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| $V_M$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| $V_I$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| $V_\Delta$ | 0.1 V | 0.1 V | 0.1 V | 0.15 V | 0.15 V | 0.3 V |




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r/t_f$ = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms (Enable and Disable Times)**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# 8 Detailed Description

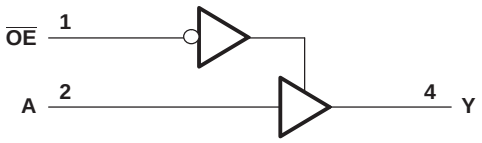
## 8.1 Overview

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family of devices is specified for low static and dynamic power consumption across the entire $V_{CC}$ range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figure 2 and Figure 3).

The SN74AUP1G125 device contains one buffer gate device with output enable control and performs the Boolean function Y = A. This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device, which prevents damage to the device.

To assure the high-impedance state during power up or power down, $\overline{OE}$ must be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* table must be followed at all times.

### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics, $T_A$ = 25°C* table. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics, $T_A$ = 25°C* table, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in the *Recommended Operating Conditions* table to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

### 8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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## Feature Description (continued)

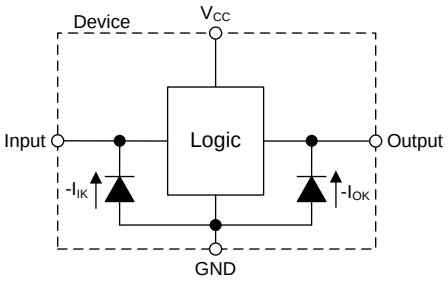


**Figure 4. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.3.4 Partial Power Down ($I_{off}$)

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by $I_{off}$ in the *Electrical Characteristics, $T_A$ = 25°C* table.

### 8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings* table.

## 8.4 Device Functional Modes

Table 1 lists the functional modes for SN74AUP1G125.

**Table 1. Function Table**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Hi-Z |


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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74AUP1G125 device is a high-drive CMOS device that is used as a output enabled buffer with a high output drive, such as an LED application. The device can produce 24 mA of drive current at 3.3 V, which is ideal for driving multiple outputs and good for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant, allowing it to translate down to $V_{CC}$.

## 9.2 Typical Application

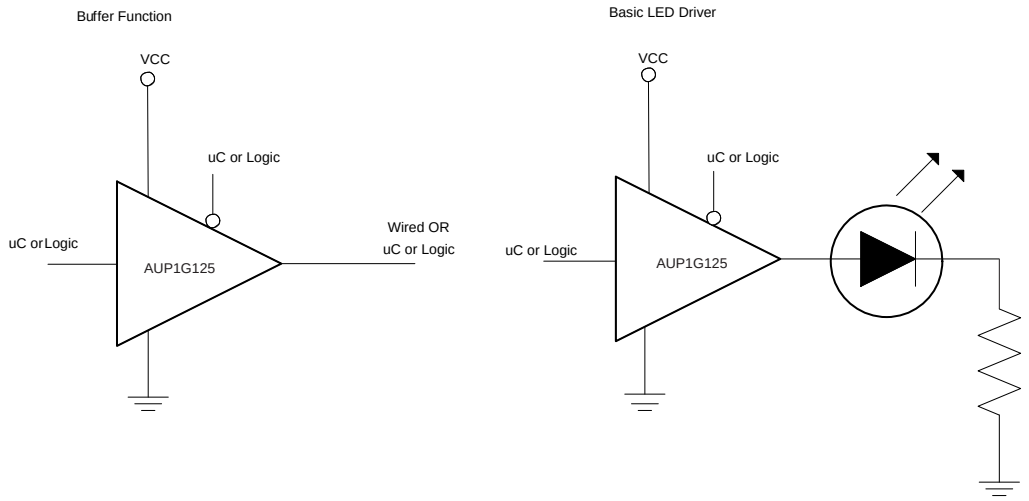


**Figure 5. Application Schematic**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as ($V_I$ max) in the *Recommended Operating Conditions* table at any valid $V_{CC}$.
2. Recommended Output Conditions
   - Load currents should not exceed ($I_O$ max) per output and should not exceed (Continuous current through $V_{CC}$ or GND) total current for the part. These limits are located in the *Absolute Maximum Ratings* table.
   - Outputs should not be pulled above $V_{CC}$.

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## Typical Application (continued)

### 9.2.3 Application Curve

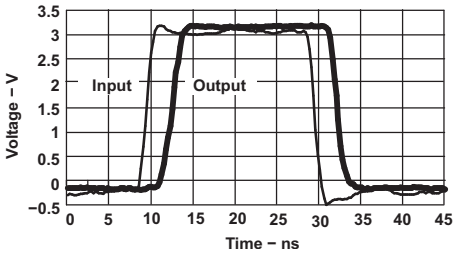


**Figure 6. Switching Characteristics at 25 MHz**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

The VCC pin must have a good bypass capacitor to prevent power disturbance. TI recommends to use a 0.1-µF capacitor for this device. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. Install the bypass capacitor as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent the inputs from floating. The logic level that should be applied to any particular unused input depends on the function of the device. The inputs should be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient.

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

### 11.2 Layout Example

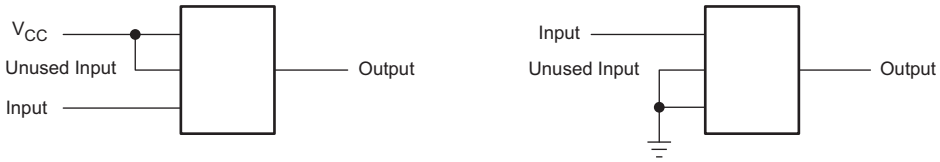


**Figure 7. Proper Multi-Gate Input Termination Diagram**


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## Layout Example (continued)

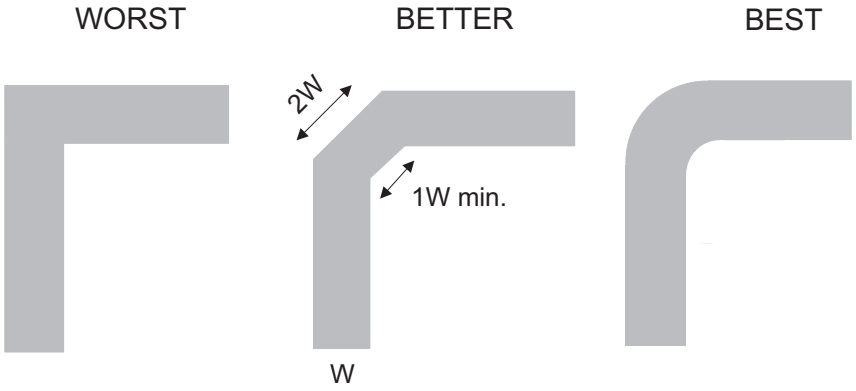


**Figure 8. Trace Example**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

*Implications of Slow or Floating CMOS Inputs*, SCBA004

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

NanoStar, E2E are trademarks of Texas Instruments.
BluRay is a trademark of Blu-ray Disc Association (BDA).
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 74AUP1G125DCKRG4 | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HM5 |
| 74AUP1G125DCKRG4.B | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HM5 |
| SN74AUP1G125DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN \| NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H25R |
| SN74AUP1G125DBVR.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H25R |
| SN74AUP1G125DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| SN \| NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H25R |
| SN74AUP1G125DBVT.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H25R |
| SN74AUP1G125DCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN \| NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HM5, HMF, HMK, HMR) |
| SN74AUP1G125DCKR.B | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | (HM5, HMF, HMK, HMR) |
| SN74AUP1G125DCKT | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU \| NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HM5, HMR) |
| SN74AUP1G125DCKT.B | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HM5, HMR) |
| SN74AUP1G125DCKTG4 | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HM5 |
| SN74AUP1G125DCKTG4.B | Active | Production | SC70 (DCK) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HM5 |
| SN74AUP1G125DPWR | Active | Production | X2SON (DPW) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (B, B1) |
| SN74AUP1G125DPWR.B | Active | Production | X2SON (DPW) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (B, B1) |
| SN74AUP1G125DRLR | Active | Production | SOT-5X3 (DRL) \| 5 | 4000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (HM7, HMR) |
| SN74AUP1G125DRLR.B | Active | Production | SOT-5X3 (DRL) \| 5 | 4000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (HM7, HMR) |
| SN74AUP1G125DRYR | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HM |
| SN74AUP1G125DRYR.B | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HM |
| SN74AUP1G125DRYRG4 | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HM |
| SN74AUP1G125DRYRG4.B | Active | Production | SON (DRY) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HM |
| SN74AUP1G125DSFR | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG \| NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HM |
| SN74AUP1G125DSFR.B | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HM |
| SN74AUP1G125DSFRG4 | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HM |
| SN74AUP1G125DSFRG4.B | Active | Production | SON (DSF) \| 6 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HM |
| SN74AUP1G125YFPR | Active | Production | DSBGA (YFP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | - | HMN |
| SN74AUP1G125YFPR.B | Active | Production | DSBGA (YFP) \| 6 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | HMN |
| SN74AUP1G125YZPR | Active | Production | DSBGA (YZP) \| 5 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | HMN |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1G125YZPR.B | Active | Production | DSBGA (YZP) \| 5 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | HMN |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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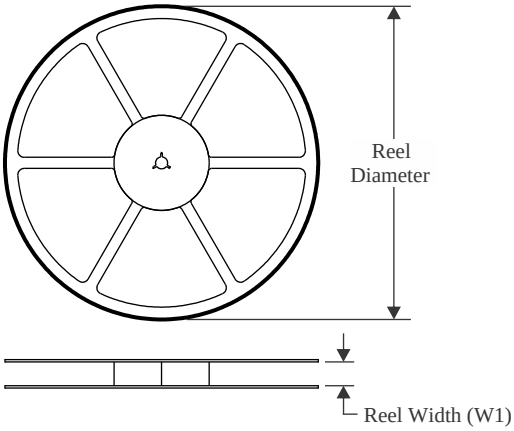
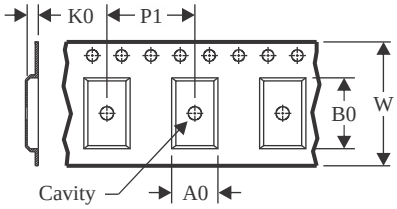
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

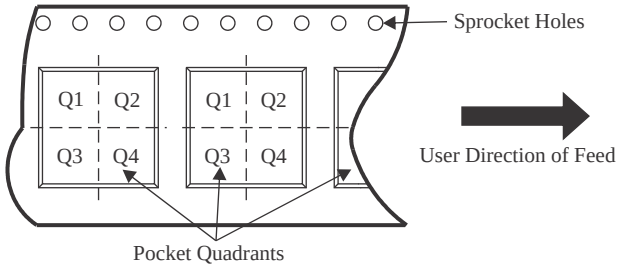



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

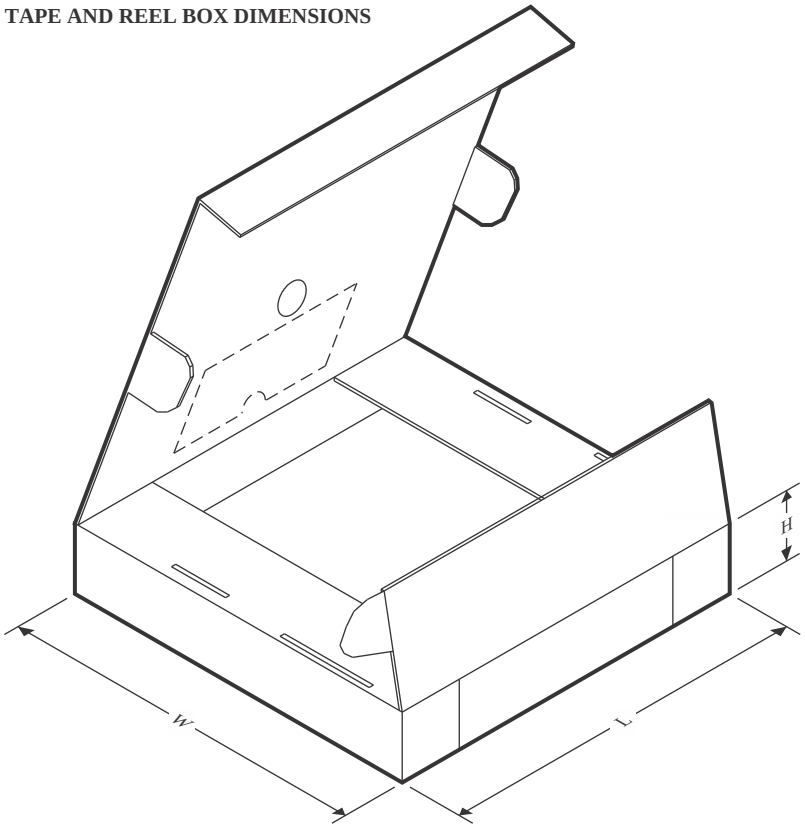



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74AUP1G125DCKRG4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUP1G125DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AUP1G125DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AUP1G125DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AUP1G125DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AUP1G125DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUP1G125DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74AUP1G125DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUP1G125DCKTG4 | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUP1G125DPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q3 |
| SN74AUP1G125DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74AUP1G125DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74AUP1G125DRYRG4 | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74AUP1G125DSFR | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74AUP1G125DSFRG4 | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74AUP1G125YFPR | DSBGA | YFP | 6 | 3000 | 178.0 | 9.2 | 0.89 | 1.29 | 0.62 | 4.0 | 8.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AUP1G125YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

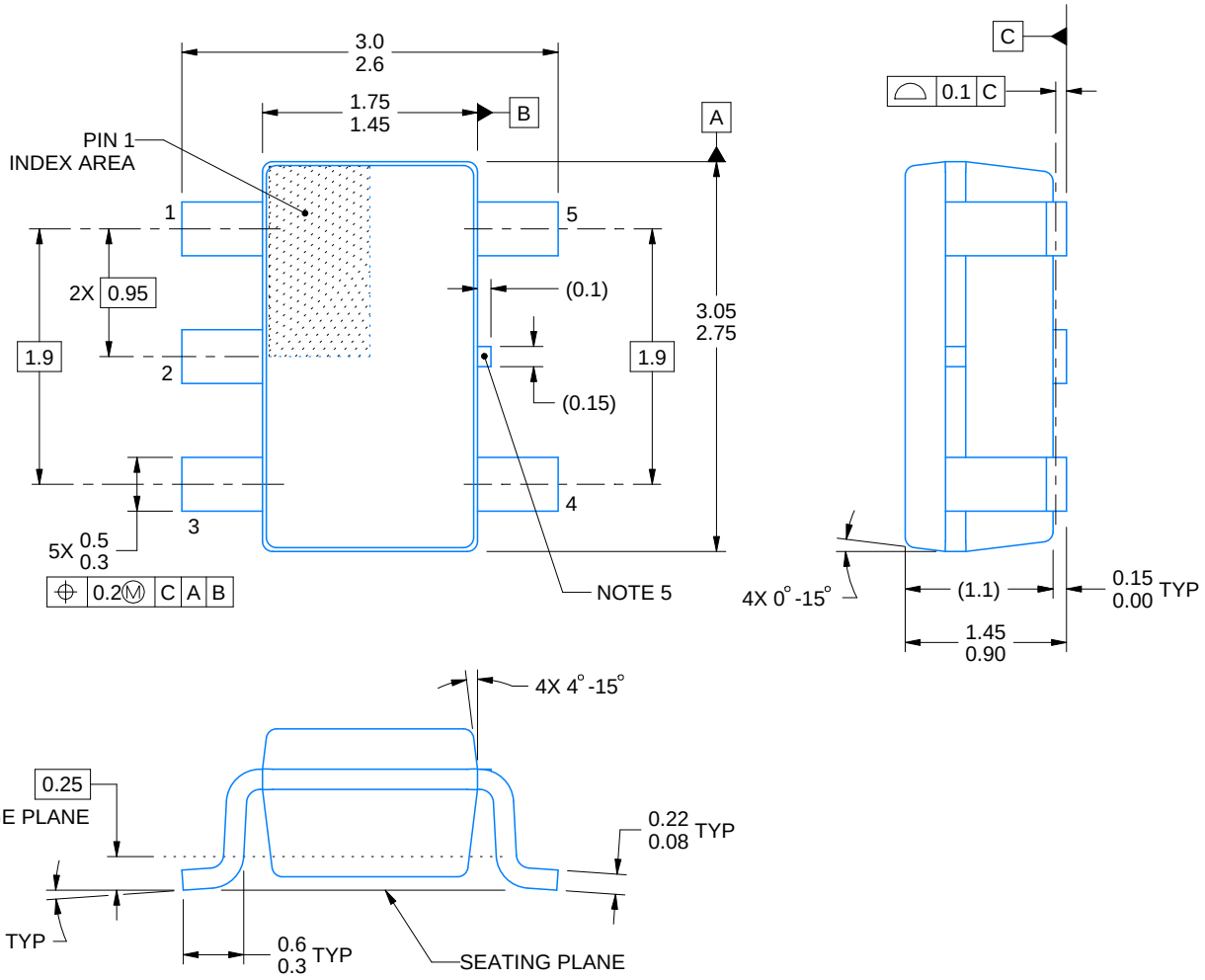
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74AUP1G125DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G125DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G125DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G125DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G125DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G125DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G125DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G125DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G125DCKTG4 | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G125DPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74AUP1G125DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G125DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G125DRYRG4 | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G125DSFR | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G125DSFRG4 | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G125YFPR | DSBGA | YFP | 6 | 3000 | 220.0 | 220.0 | 35.0 |
| SN74AUP1G125YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

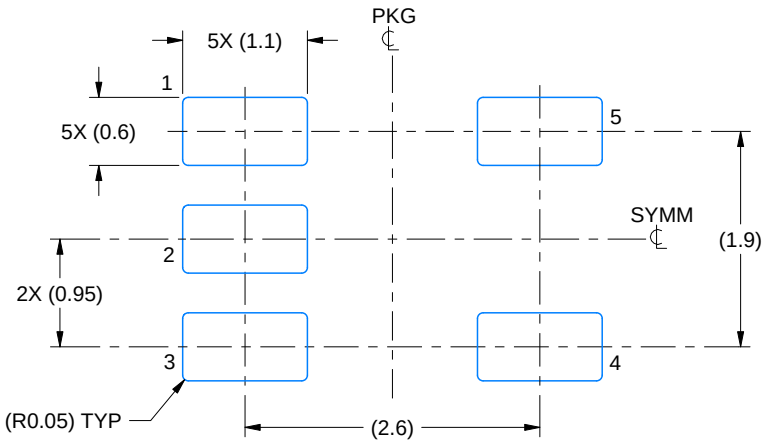
SMALL OUTLINE TRANSISTOR



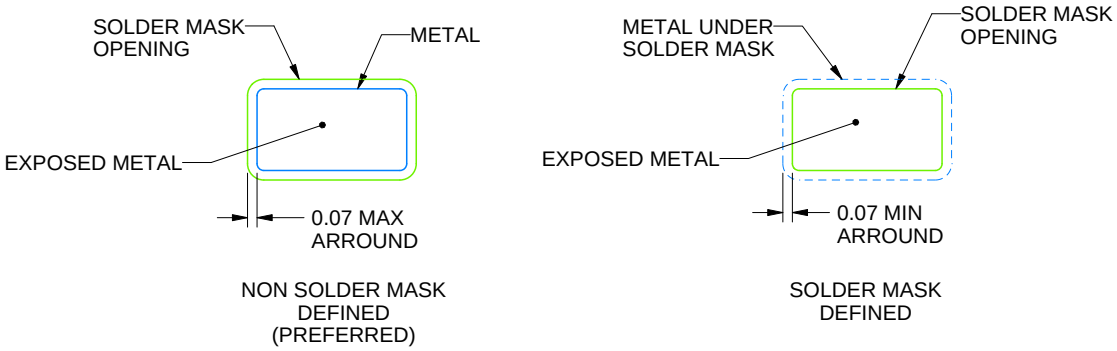

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

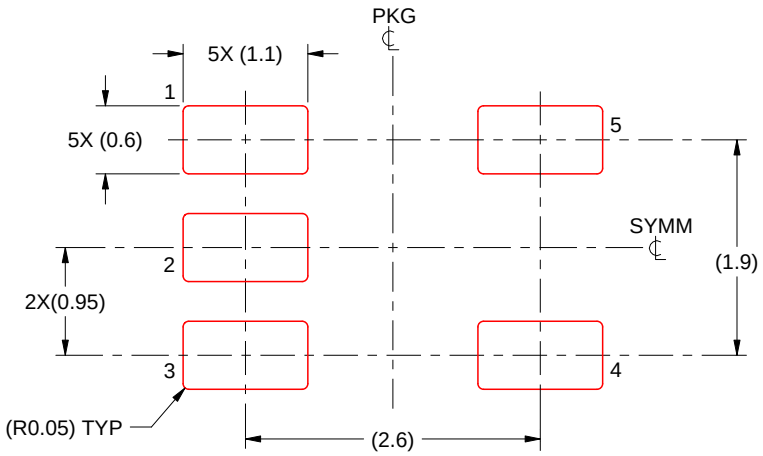



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

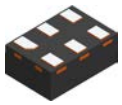
# DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

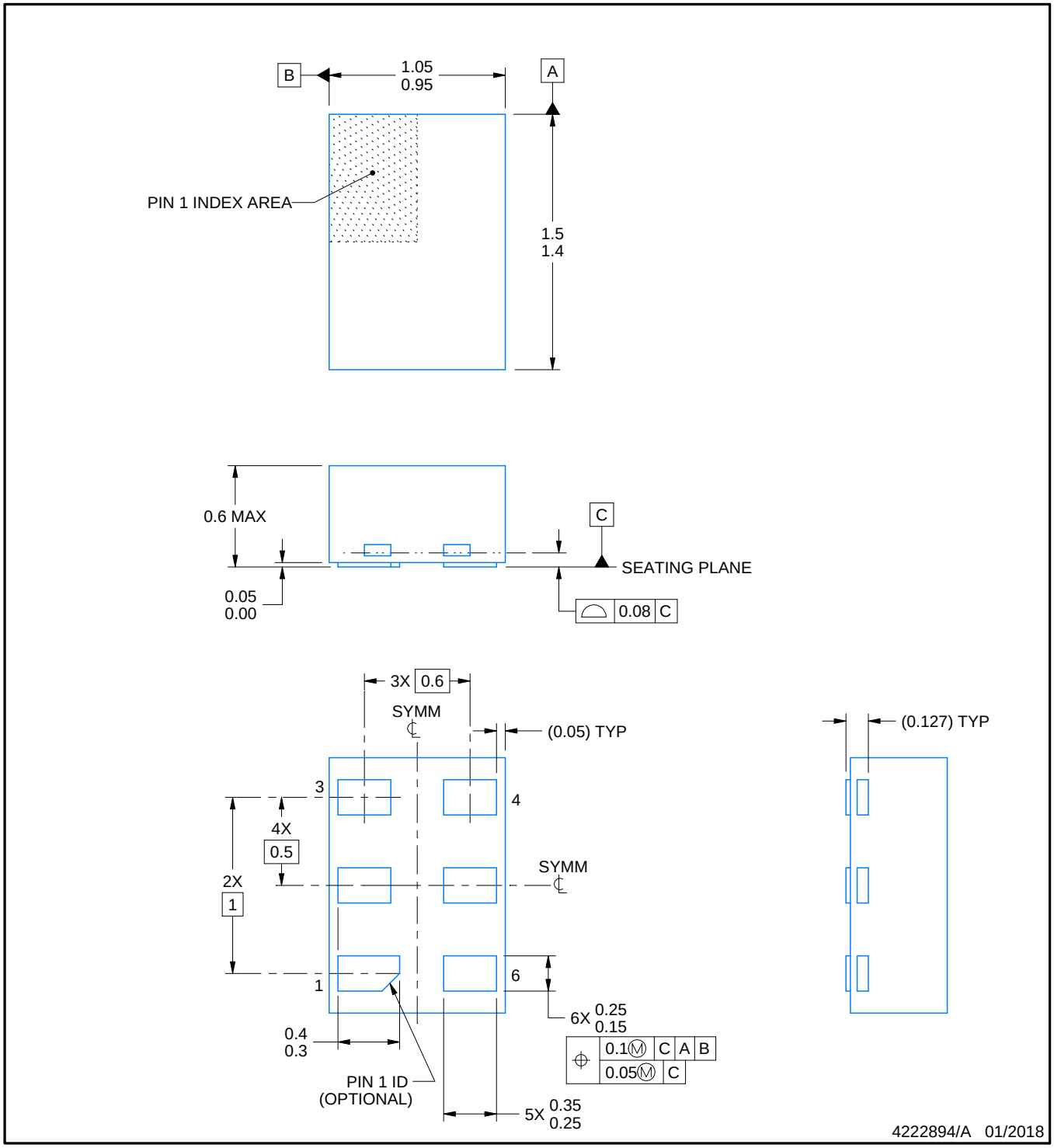
# DRY0006A



# PACKAGE OUTLINE

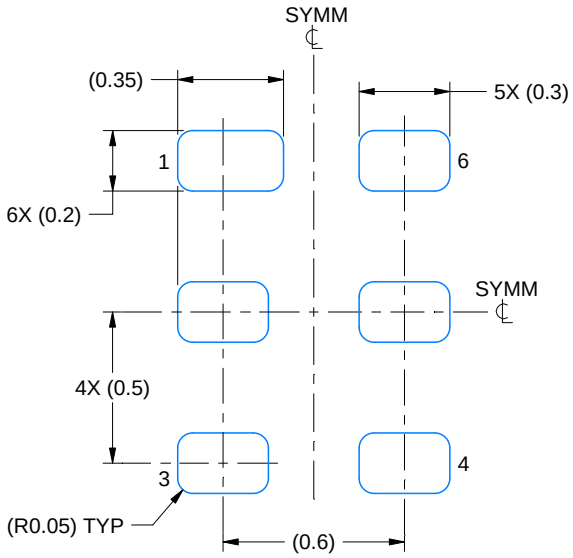
## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

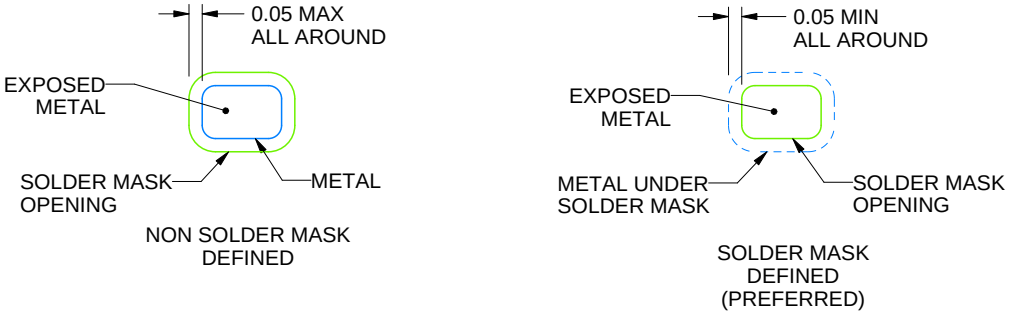



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

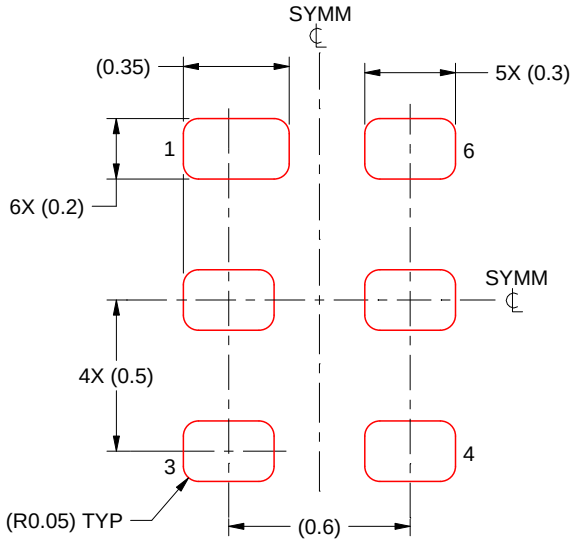
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DRY0006A

## USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

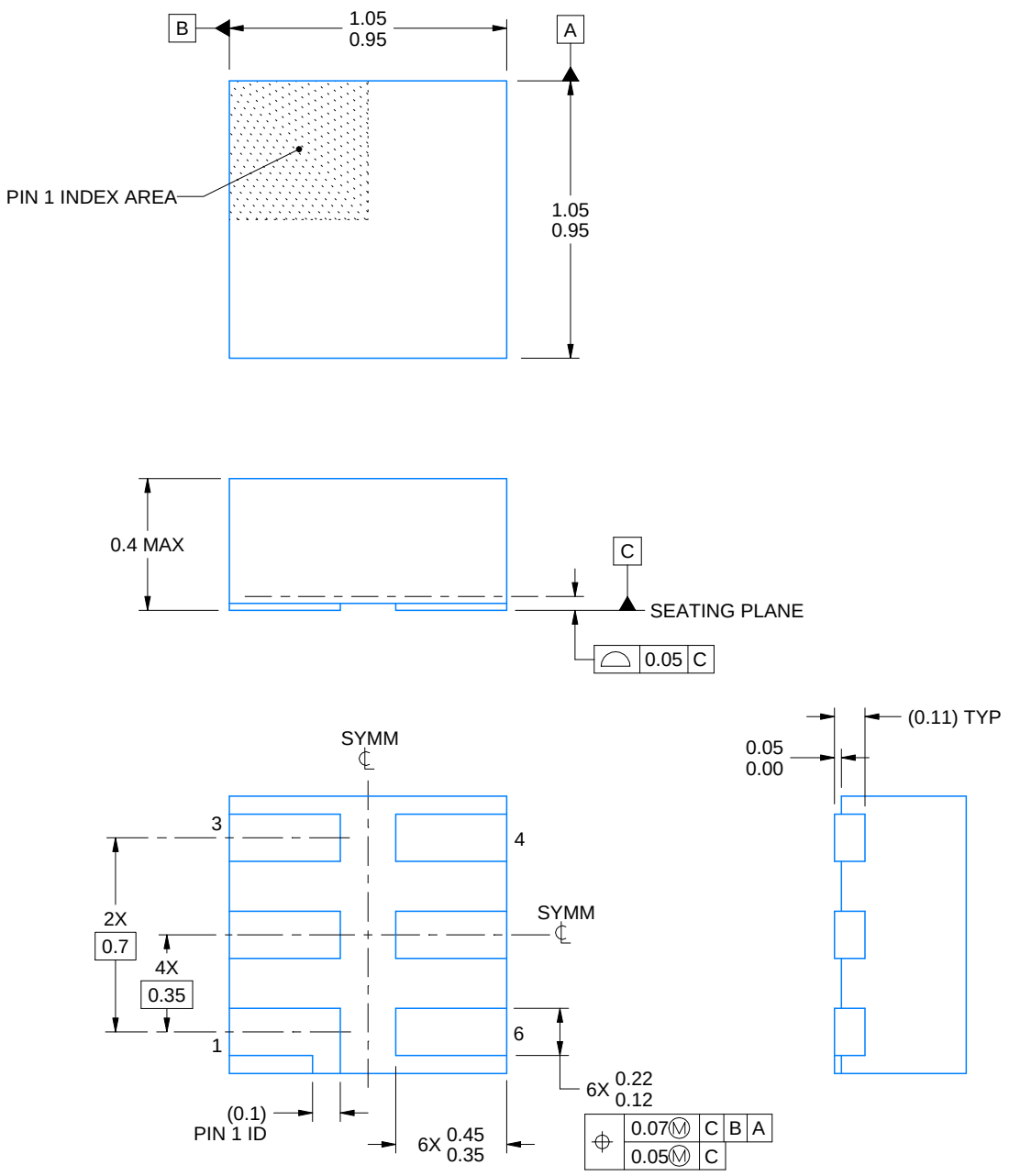
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DSF0006A

## X2SON - 0.4 mm max height

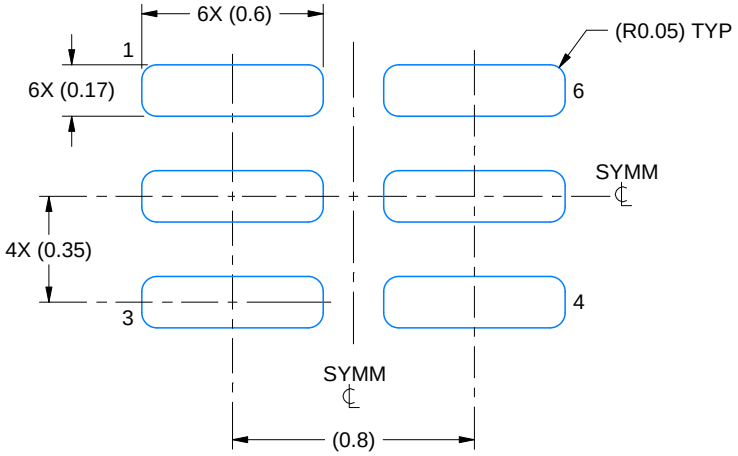
PLASTIC SMALL OUTLINE - NO LEAD



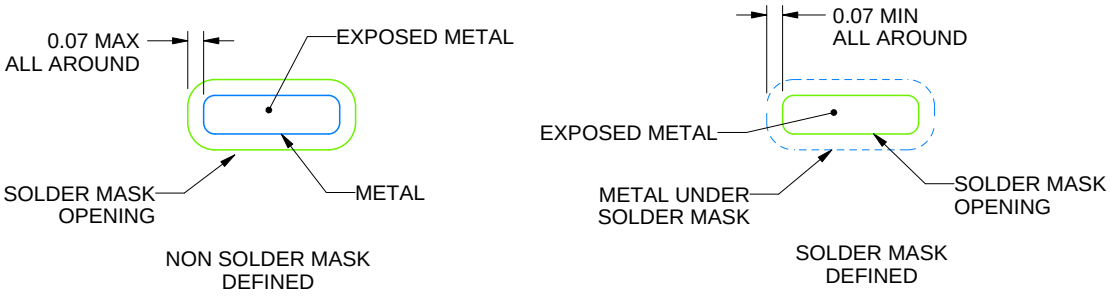

4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X




SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

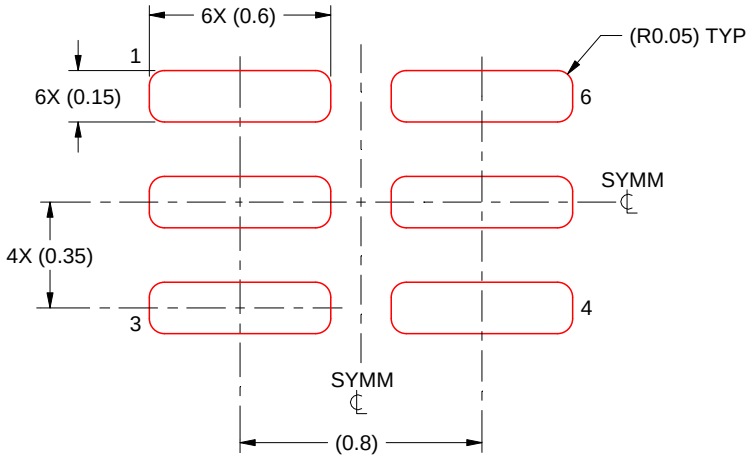
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DSF0006A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

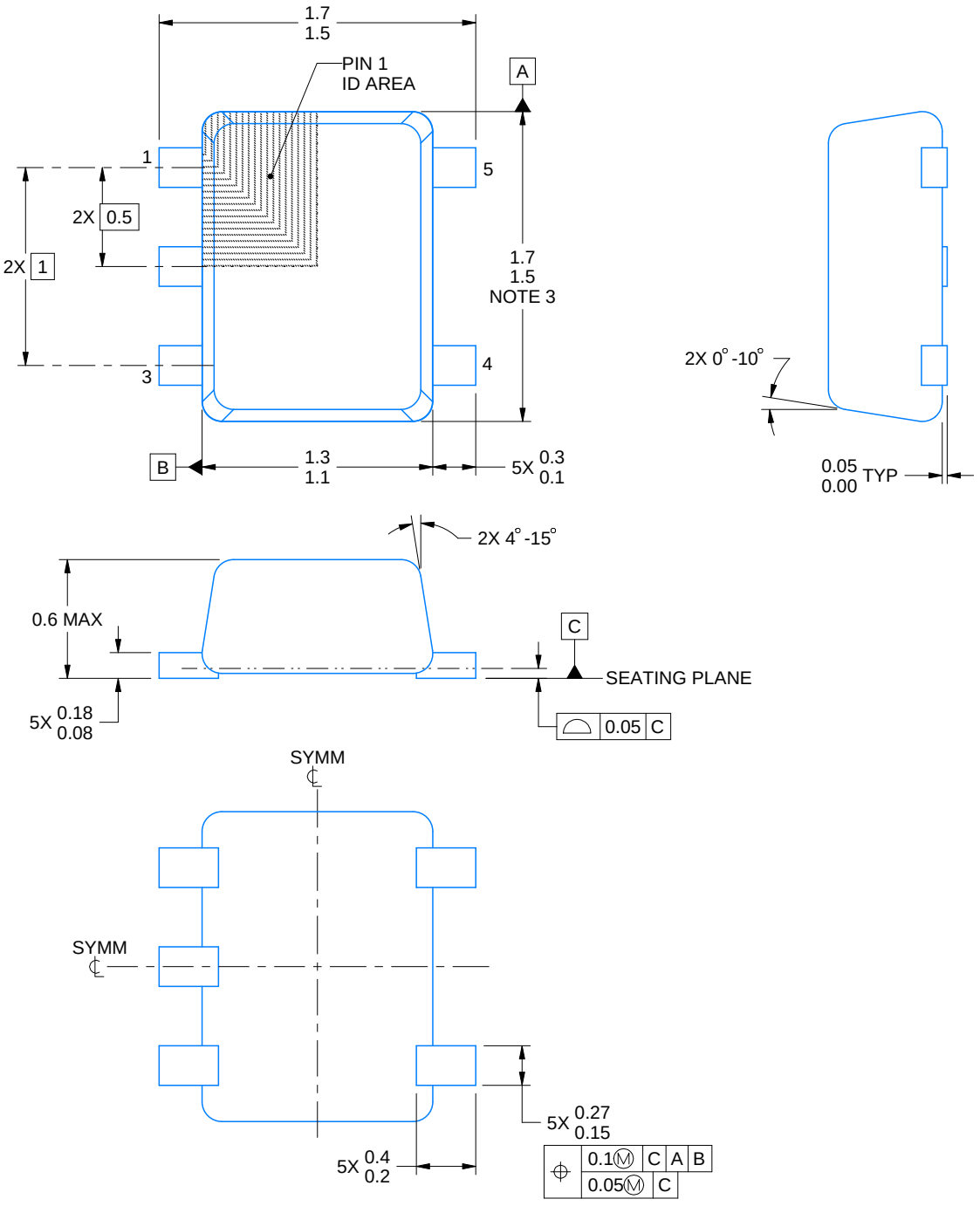
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## DRL0005A

## SOT - 0.6 mm max height

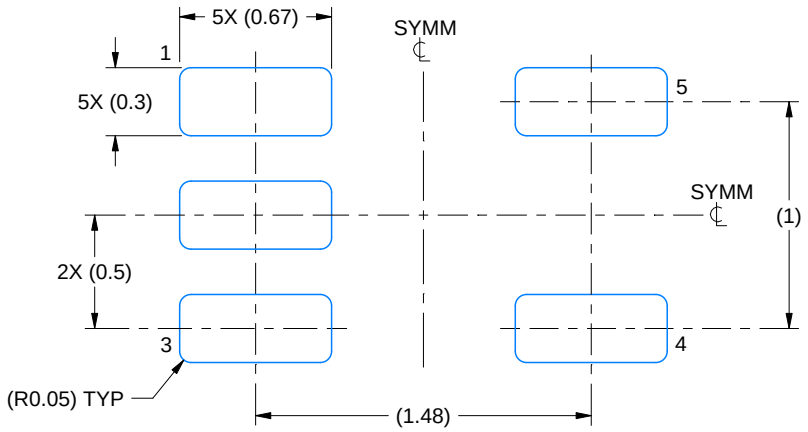
PLASTIC SMALL OUTLINE



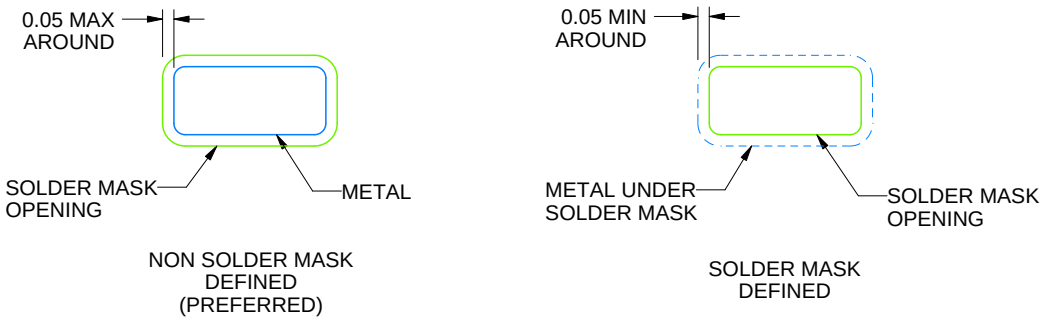

4220753/E 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1




LAND PATTERN EXAMPLE
SCALE:30X

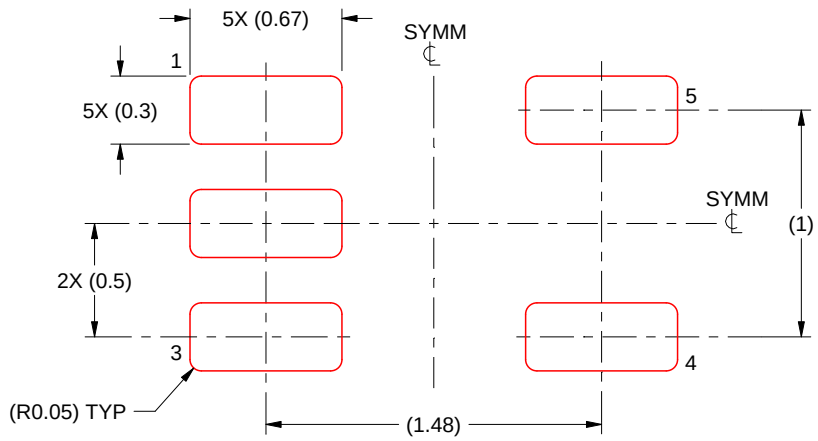



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

## DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

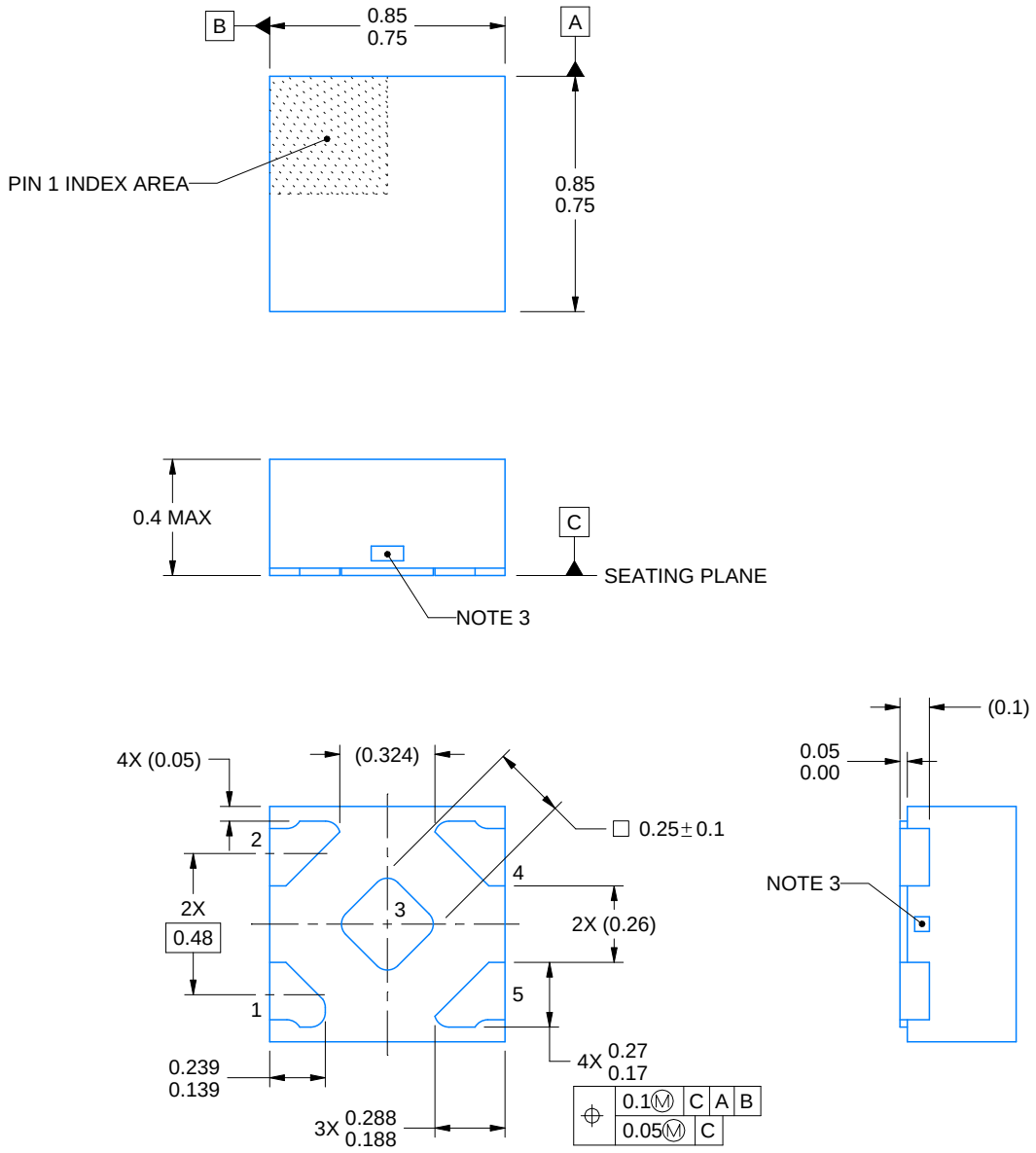
4211218-3/D

# PACKAGE OUTLINE

## DPW0005A

## X2SON - 0.4 mm max height

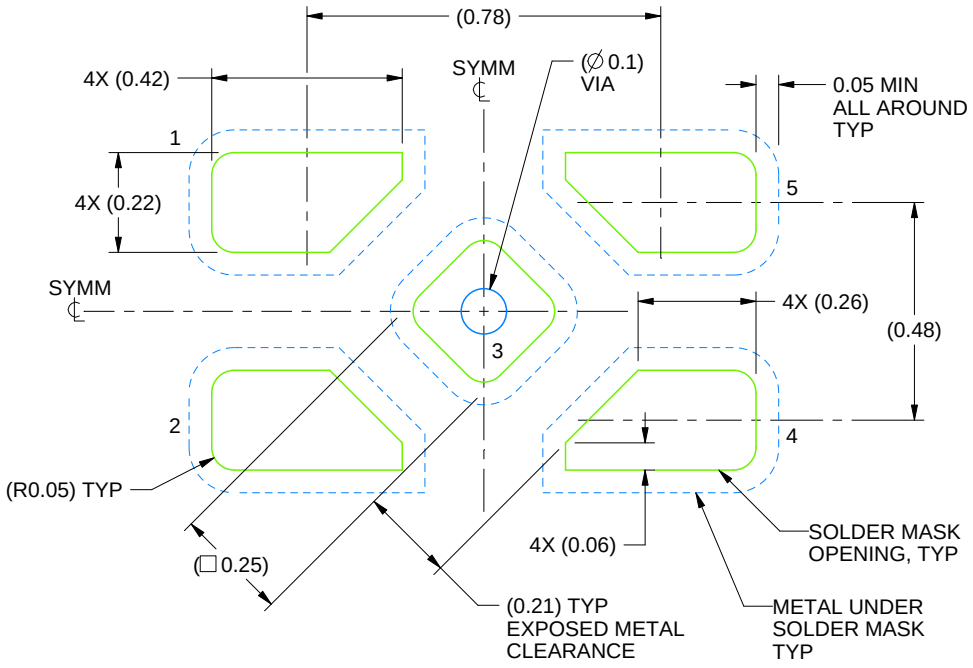
PLASTIC SMALL OUTLINE - NO LEAD




4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.




LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

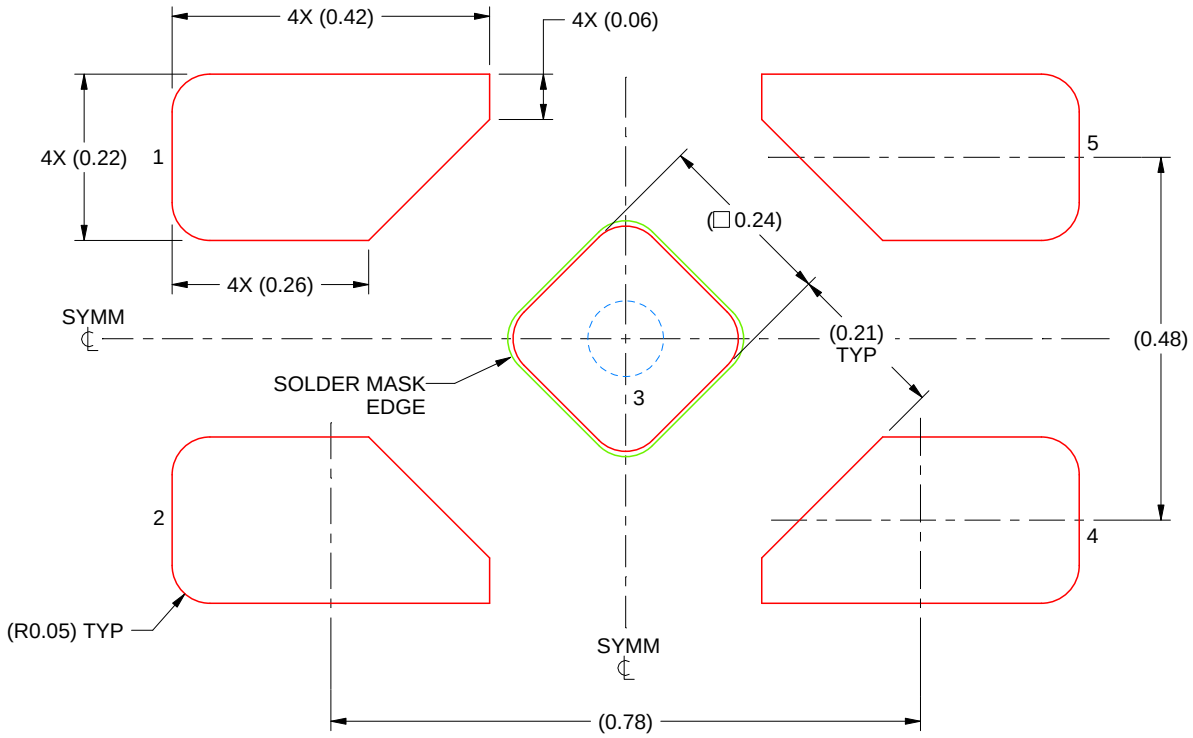
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## DPW0005A

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

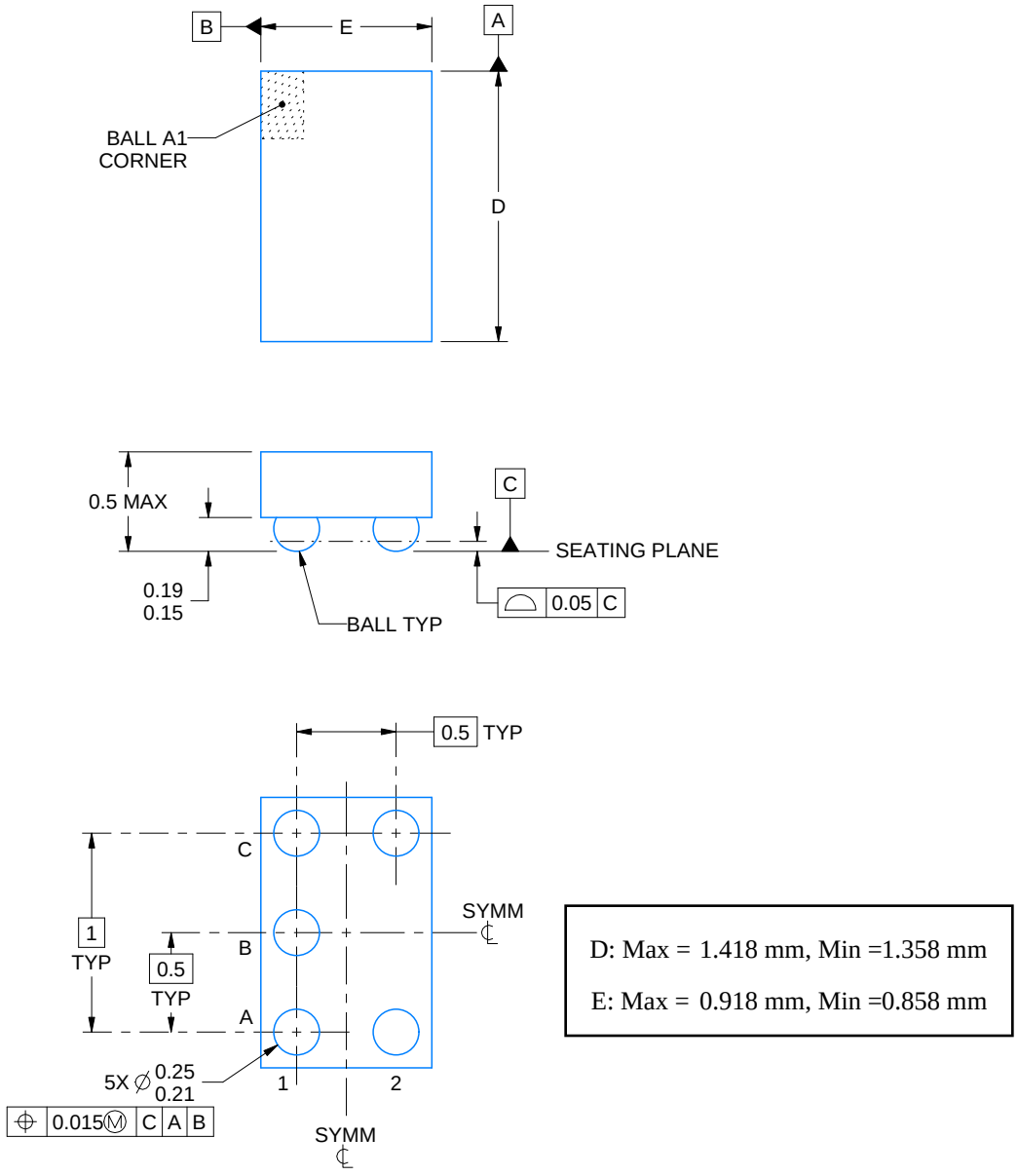
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## YZP0005

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



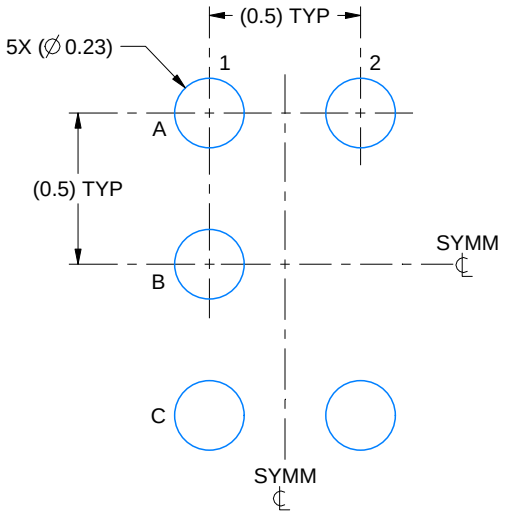

D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

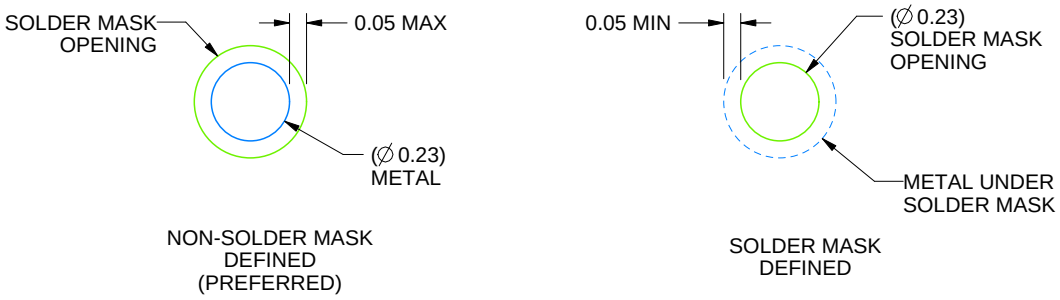
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:40X

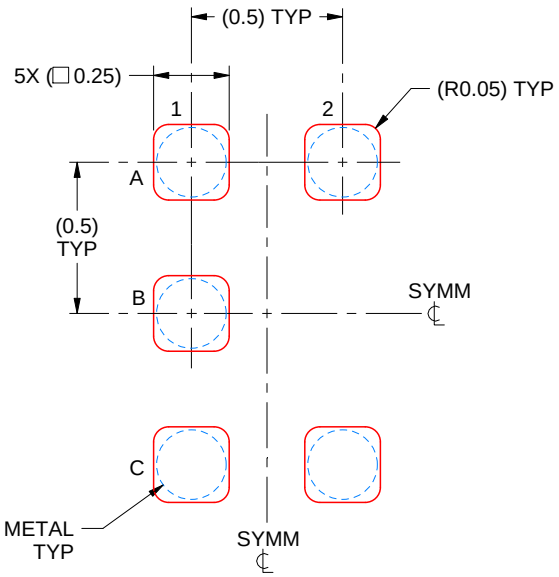



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

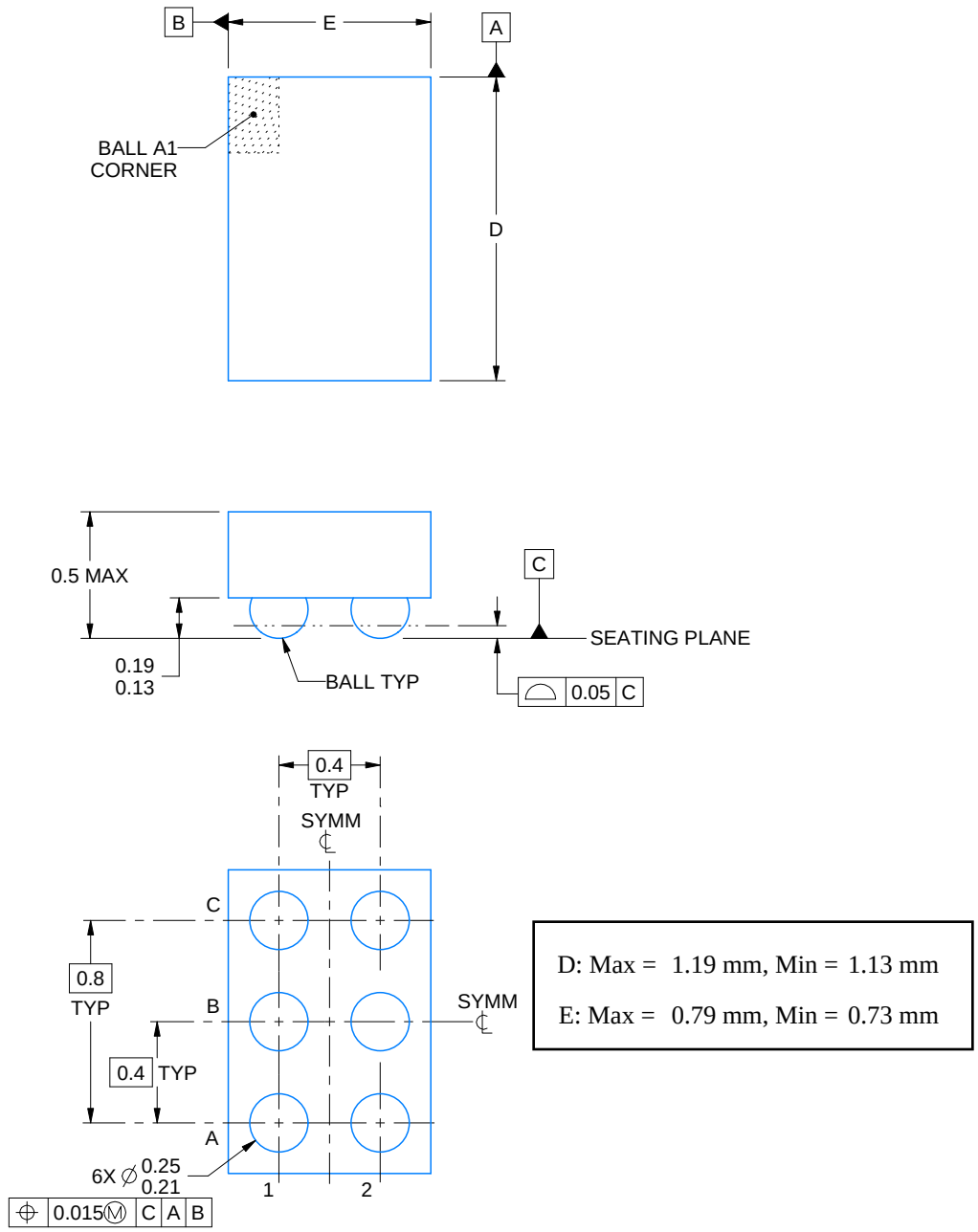
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## YFP0006

## DSBGA - 0.5 mm max height

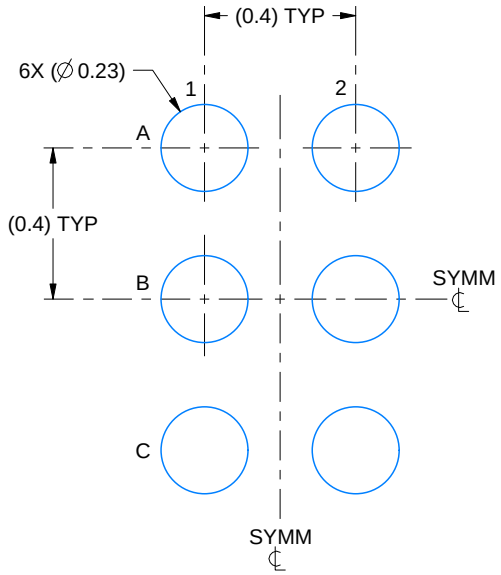
DIE SIZE BALL GRID ARRAY



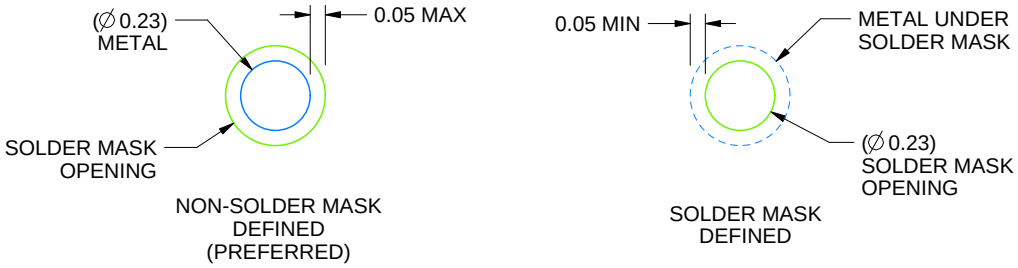

4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:50X

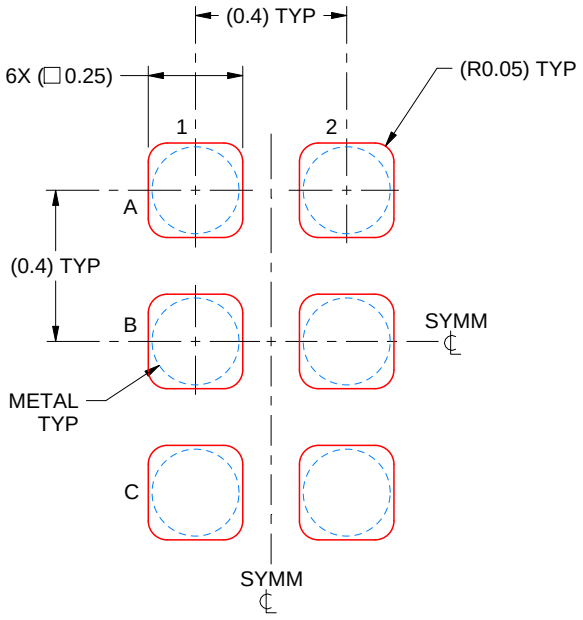



SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

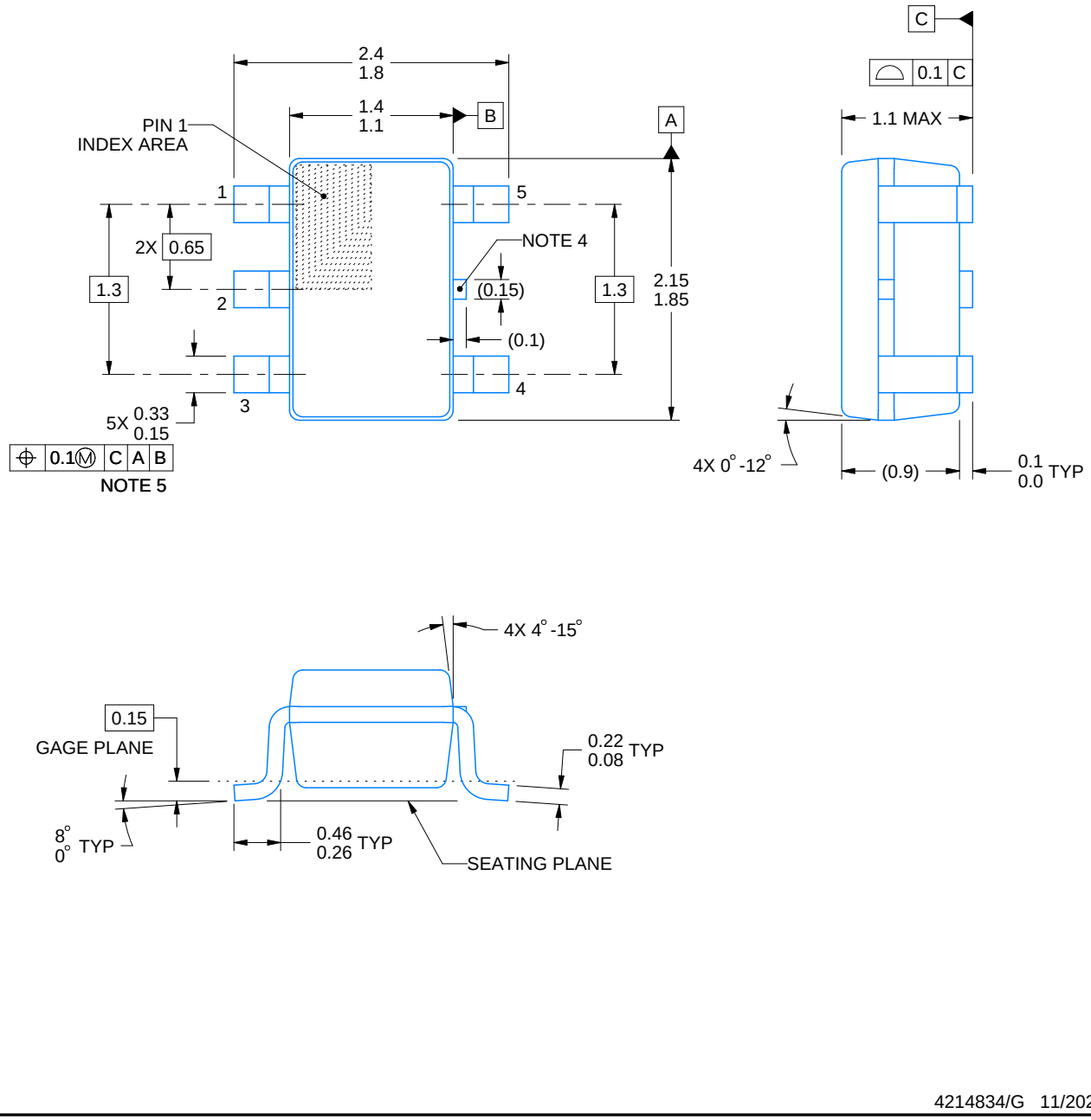
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

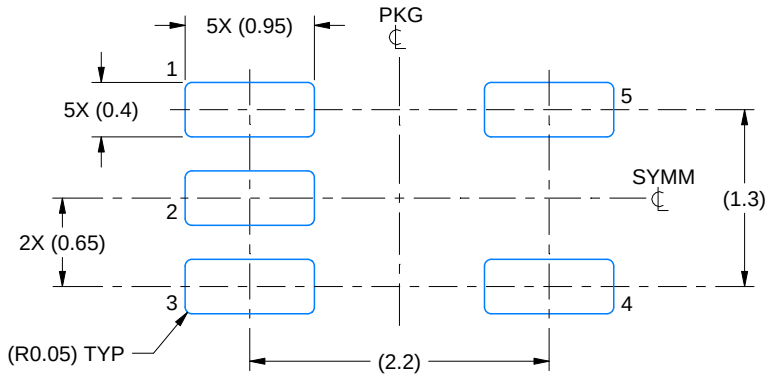
SMALL OUTLINE TRANSISTOR



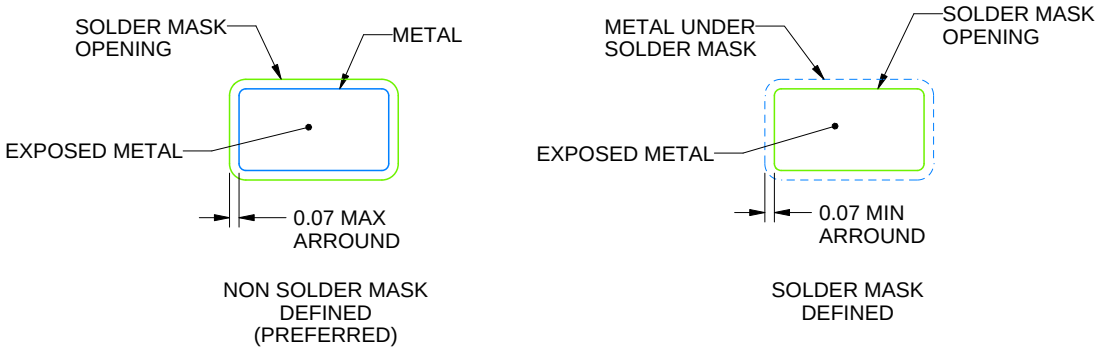

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

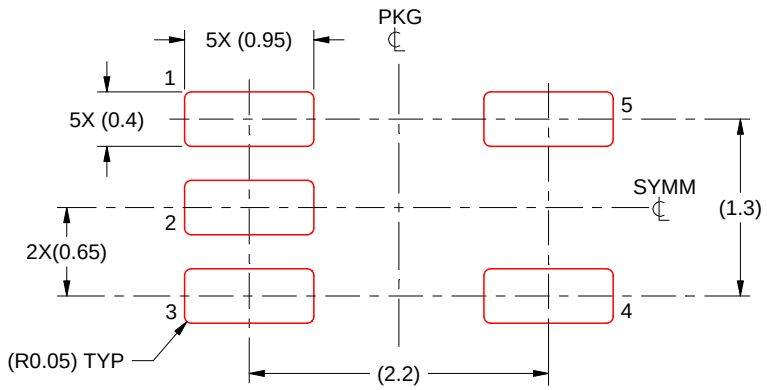



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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