TLK1002A
DUAL SIGNAL CONDITIONING TRANSCEIVER

SLLS661–JUNE 2005

FEATURES

- **Fully Integrated Signal Conditioning Transceiver**
- **1.0–1.3 Gbps Operation**
- **Low Power CMOS Design (<300 mW)**
- **High Differential Output Voltage Swing (1600 mVp-p typical)**
- **400 mVp-p Differential Input Sensitivity**
- **High Input Jitter Tolerance 0.606 UI**
- **Single 1.8 V Power Supply**
- **2.5 V Tolerant Control Inputs**
- **Differential VML Transmit Outputs With No External Components Necessary**
- **No External Filter Components Required for PLLs**
- **Supports Loop-Back Modes**
- **Temperature Rating 0°C to 70°C**
- **Small Footprint 4 mm × 4 mm 24-Lead QFN Package**

APPLICATIONS

- **Resynchronization in Both Directions for 1.25 Gbps Links**
- **Repeater for 1.0625 Gbps Applications**

DESCRIPTION

TLK1002A is a single-chip dual signal conditioning transceiver.

This chip supports data rates from 1.0 Gbps up to 1.3 Gbps. An on-chip clock generation phase-locked loop (PLL) generates the required half-rate clock from an externally applied reference clock. This reference clock equals approximately one tenth of the data rate. It may be off frequency from both received data streams by up to ±200 ppm.

Both data paths are implemented identical. The implemented input buffers provide an input sensitivity of 400 mVp-p differential.

The data paths tolerate up to 0.606 UI total input jitter. Signal retiming is performed by means of phase-locked loop (PLL) circuits. The retimed output signals are fed to VML output buffers, which provide output amplitudes of typical 1600mVp-p differential across the external 2x50 Ω load.

TLK1002A only requires a single 1.8 V supply voltage. Robust design avoids the necessity of special off-chip supply filtering.

Advanced low power CMOS design leads to low power consumption.

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BLOCK DIAGRAM

A simplified block diagram of the TLK1002A circuit is shown in Figure 1. The main circuit parts are described in detail below.

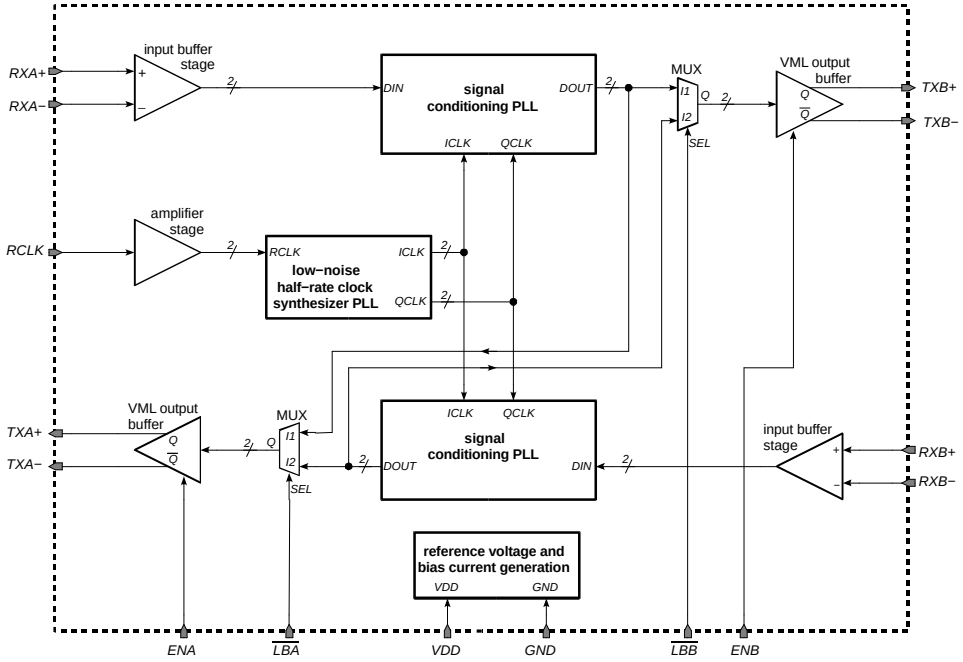


Figure 1. Simplified Block Diagram of the TLK1002A Transceiver

DATA PATHS

The serial input data streams are connected to the input ports *RXA+/RXA–* or *RXB+/RXB–* respectively. The input stages provide on-chip differential 100-Ω termination. The outputs of the input buffer stages are connected to the signal conditioning PLL circuits.

The PLL output signals are fed to multiplexer (MUX) stages, which are used to redirect the data signals if loop back mode is selected.

The multiplexer stages are connected to the output ports *TXB+/TXB–* or *TXA+/TXA–* , respectively, by means of VML output buffer stages. To enable the output buffer stages, *ENA* and *ENB*, which are internally pulled up, must be at high level (*VDD*).

The loop back modes are enabled by means of the control-inputs $\overline{\text{LBA}}$ and $\overline{\text{LBB}}$, which are implemented as active low inputs with integrated pull-up resistors. If $\overline{\text{LBA}}$ is set to low level, the input data applied to the input port *RXA+/RXA–* is retimed and fed to both output ports *TXB+/TXB–* and *TXA+/TXA–*. If $\overline{\text{LBB}}$ is pulled low, the retimed input data signal applied to *RXB+/RXB–* is available at *TXA+/TXA–* and *TXB+/TXB–*.

If a logic low signal is applied to both loop back control inputs the retimed signal connected to *RXA+/RXA–* appears at *TXA+/TXA–*, while the retimed signal applied to *RXB+/RXB–* is fed to *TXB+/TXB–*.

DATA PATHS (continued)

LOW-NOISE HALF-RATE CLOCK GENERATION PLL

In order to achieve the low power requirements, an on-chip half-rate clock synthesizer PLL is implemented. It generates the internally used inphase and quadrature clock signals with 5 times the reference clock frequency.

The required reference clock frequency equals approximately one tenth of the data rate. It may be off frequency from both transmit and receive data streams by up to ±200 ppm.

A valid reference clock must be connected to the RCLK pin to ensure proper operation. In case of a clock absence of up to 4 cycles during clock switch over the CDR will independently re-acquire lock (i.e., without the need of any reset signal), however during re-locking erroneous bits will be transmitted for a limited period of time.

The reference clock may contain jitter, in the order of about 80 ps_{p-p}. However, the jitter components below 10 MHz, which is the bandwidth of the clock generation PLL, must not exceed 40 ps_{p-p}.

Increased reference clock jitter leads to increased output jitter as well as to reduced jitter tolerance.

CONTROL INPUTS

TLK1002A provides a total of four control inputs, which activate the VML output buffer stages and enable the loop-back modes.

These control inputs may be driven from circuits using a different supply voltage. Thus, 2.5 V tolerance is mandatory at these pins. All control inputs provide on-chip pull-up resistors to *VDD*.

REFERENCE VOLTAGE AND BIAS CURRENT GENERATION

The TLK1002A transceiver is supplied by a 1.8 V ±5% supply voltage connected to *VDD*. The voltage is referred to ground (*GND*).

From this voltage all required reference voltages and bias currents are derived by means of the reference voltage and bias current generation block.

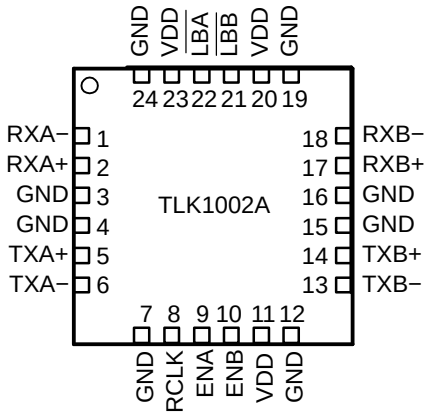
PACKAGE

For the TLK1002A a small footprint 4 mm × 4 mm 24-lead QFN package is used, with a lead pitch of 0.5 mm. The pin out is shown below.

The thermal resistance of the package is about 47°C/W. At a total power consumption of 0.3 W assuming an ambient temperature of 70°C, the maximum junction temperature is below 85°C.

PIN OUT

RGE PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1	RXA–	In	Inverted data input A. On board AC coupled. On-chip 100-Ω differential terminated to RXA+.
2	RXA+	In	Non-inverted data input A. On board AC coupled. On-chip 100-Ω differential terminated to RXA–.
3, 4, 7, 12, 15, 16,19, 24, EP	GND	Supply	Circuit ground. The exposed die pad (EP) must be grounded.
5	TXA+	VML-out	Retimed non-inverted data output A. On board AC coupled.
6	TXA–	VML-out	Retimed inverted data output A. On board AC coupled.
8	RCLK	CMOS-in	Reference clock input. Self biased for AC coupling. This input is 2.5 V tolerant.
9	ENA	CMOS-in	Enable A, on-chip pulled up to VDD. When set to high level, the VML output buffer driving the TXA+/TXA– port is enabled. This input is 2.5 V tolerant.
10	ENB	CMOS-in	Enable B, on-chip pulled up to VDD. When set to high level, the VML output buffer driving the TXB+/TXB– port is enabled. This input is 2.5 V tolerant
11, 20, 23	VDD	Supply	1.8 V ±5% supply voltage
13	TXB–	VML-out	Retimed inverted data output B. On board AC coupled.
14	TXB+	VML-out	Retimed non-inverted data output B. On board AC coupled.
17	RXB+	In	Non-inverted data input B. On board AC coupled. On-chip 100-Ω differential terminated to RXB–.
18	RXB–	In	Inverted data input B. On board AC coupled. On-chip 100-Ω differential terminated to RXB+.
21	$\overline{\text{LBB}}$	CMOS-in	Loop back B, on-chip pulled up to VDD. When pulled to low level, loop back mode B is enabled The input data applied to the input port RXB+/RXB– is retimed and fed to both output ports TXA+/TXA– and TXB+/TXB–. This input is 2.5 V tolerant.
22	$\overline{\text{LBA}}$	CMOS-in	Loop back A, on-chip pulled up to VDD. When pulled to low level, loop back mode A is enabled The input data applied to the input port RXA+/RXA– is retimed and fed to both output ports TXB+/TXB– and TXA+/TXA–. This input is 2.5 V tolerant.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE
V_{DD}	Supply voltage(2)	–0.3 V to 2.5 V
V_{CMOS}	Voltage range at CMOS input terminals (ENA, ENB, $\overline{LBA}$, $\overline{LBB}$, RCLK)(2)	–0.3 V to 3.0 V
	Electrical discharge	2k V (HBM)
T_A	Characterized free-air temperature range (no airflow)	0°C to 70°C
T_{STG}	Storage temperature range	–65°C to 85°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.7	1.8	1.9	V
T_A	Ambient temperature (no airflow, no heatsink)	0		70	°C

DC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		1.7	1.8	1.9	V
I_{VCC2}	Current from 1.8 V supply	ENA = high, ENB = high, $V_{DD} = V_{DD,max}$ PRBS 1.25 Gbps data on both inputs			158	mA
$V_{IL,CMOS}$	Low level CMOS input voltage	V_{DD}= 1.8 V	–0.2		0.6	V
$V_{IH,CMOS}$	High level CMOS input voltage	V_{DD} = 1.8 V	V_{DD}–0.6		2.7	V
$I_{L,CMOS}$	Low level CMOS input current	$V_{DD} = V_{DD,max}$, V_{IL} = 0.0 V			–120	µA
$I_{H,CMOS}$	High level CMOS input current	$V_{DD} = V_{DD,min}$, V_{IH} = 2.7 V			165	µA
R_{PU}	Integrated pull-up resistor to V_{DD}			20		kΩ

AC ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA PATHS						
$Z_{D,IN}$	Differential input impedance			100		Ω
TJ_{IN}	Total input jitter	BER ≤ 10^{-12}, 1.25 Gbps data			0.606	UI
DJ_{IN}	Deterministic input jitter	BER ≤ 10^{-12}, 1.25 Gbps data			0.373	UI_{pp}
$V_{CM,IN}$	Common-mode input voltage			1200		mV
$v_{S,IN}$	Single-ended input voltage swing		200	800	1200	mV_{p-p}
$v_{D,IN}$	Differential input voltage swing		400	1600	2400	mV_{p-p}
$X1_{IN}$	Input eye mask	BER ≤ 10^{-12}, 1.25 Gbps data, See Figure 2			0.303	UI
$Y1_{IN}$			200			mV
$Y2_{IN}$					1200	mV
$t_{R,OUT}$, $t_{F,OUT}$	Output signal rise/fall time	20% to 80%		150	260	ps
TJ_{OUT}	Total output jitter	1.25 Gbps input from 3.3G pattern generator at 0 ppm		0.20	0.28	UI
DJ_{OUT}	Deterministic output jitter	1.25 Gbps input from 3.3G pattern generator at 0 ppm			0.1	UI_{pp}
$V_{CM,OUT}$	Common-mode output voltage		800	1000	1200	mV
$v_{S,OUT}$	Single-ended output voltage swing		440	800	1000	mV_{p-p}
$v_{D,OUT}$	Differential output voltage		880	1600	2000	mV_{p-p}
$X1_{OUT}$	Output eye mask	1.25 Gbps input from 3.3G pattern generator at 0 ppm See Figure 3			0.12	UI
$X2_{OUT}$					0.32	UI
$Y1_{OUT}$			440			mV
$Y2_{OUT}$					1000	mV
t_D	RX to TX latency				25	ns
t_{INI}	Lock acquisition from link down	See (1) and (2)		4		µs
t_{LCK}	Lock recovery on link discontinuity	See (2)		1.6		µs

(1) Assuming maximum initial CDR phase offset and maximum frequency difference between reference clock and input data.
(2) The output data may contain bit errors during lock-in time, dependent on the input-data sequence and the input-data jitter. However it is assured, that the output-data does not contain bits with widths deviating significantly from the nominal bit width.

AC ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE CLOCK AC SPECIFICATIONS						
$V_{IL,RCLK}$	Reference clock low level voltage	DC coupled	–0.3		0.3	V
$V_{IH,RCLK}$	Reference clock high level voltage	DC coupled	1.5		2.1	V
v_{RCLK}	Reference clock swing	AC coupled	1.2		2.4	V_{p-p}
$V_{IH,RCLK}$	Reference clock input threshold (self biasing)	AC coupled		0.9		V
	Clock duty cycle		40%		60%	
$t_{R,RCLK}$, $t_{F,RCLK}$	Rise / fall time	20% to 80%	300		1500	ps
$f_{0,RCLK}$	Reference clock frequency(3)			Baud/10		
$TJ_{RCLK200}$	Reference clock total jitter(4)	Up to 10 MHz			40	ps_{p-p}
TJ_{RCLK}				80		ps_{p-p}
Δf_{RCLK}	Frequency difference between reference clock and incoming data signal	Reference clock and incoming data are off the nominal data rate but in opposite direction	–200		200	ppm

(3) Reference clock is not locked to the data frequency and may deviate by Δf_{RCLK}.
(4) The reference clock may contain jitter, in the order of about 80 ps_{p-p}. However, the jitter components below 10 MHz, which is the bandwidth of the clock generation PLL, must not exceed 40 ps_{p-p}. Increased reference clock jitter leads to increased output jitter as well as to reduced jitter tolerance.

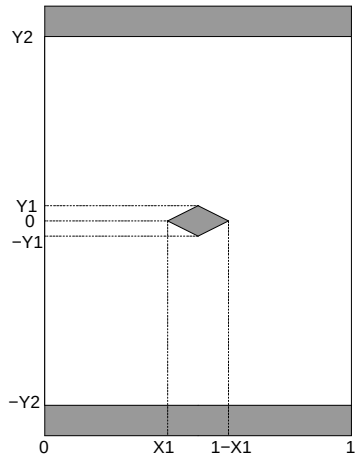


Figure 2. Input Eye Mask

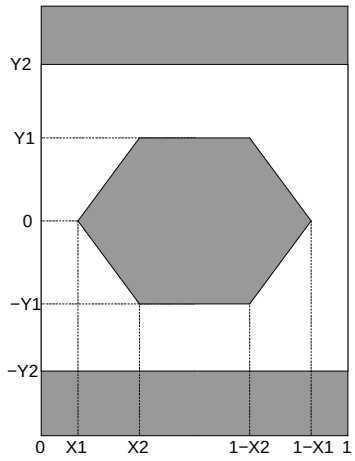


Figure 3. Output Eye Mask

OPERATIONAL MODES

NORMAL OPERATION MODE

In normal operation, the data signal at the *RXA+/RXA–* pins is applied to an input buffer stage, which drives a signal conditioning PLL. The retimed output signal is connected to the output pins *TXB+/TXB–* by means of a multiplexer stage and a VML output buffer.

On the other side, the input signal applied to the *RXB+/RXB–* pins is connected to a signal conditioning PLL by means of an input buffer stage. The retimed output signal of the PLL is connected to the output pins *TXA+/TXA–* using a multiplexer stage as well as a VML output driver.

OPERATIONAL MODES (continued)

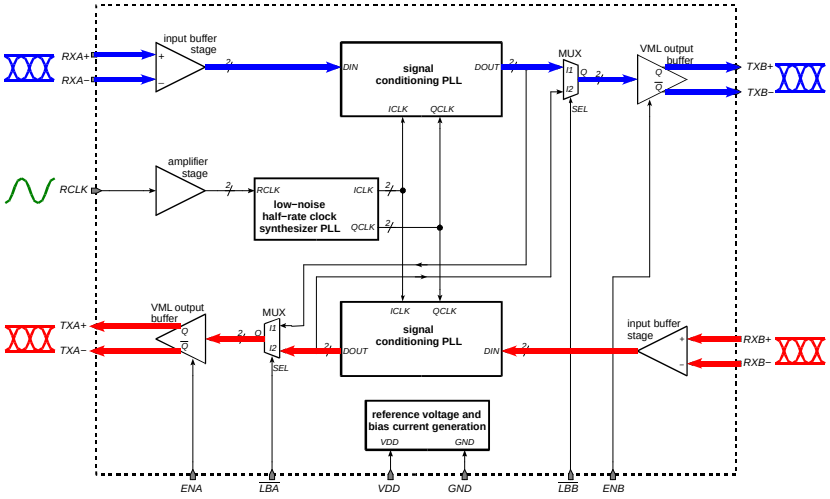


Figure 4. Data Path in Normal Operation Mode

INTERNAL LOOP-BACK MODE A

In internal loop-back mode A operation, which is activated by pulling the $\overline{\text{LBA}}$ pin to logic low level, the input data signal at the *RXA+/RXA–* pins is applied to the input buffer driving a signal conditioning PLL. The retimed output signal is connected to the output pins *TXB+/TXB–* by means of a multiplexer stage and a VML output buffer.

Furthermore, by means of a second multiplexer the same signal is fed to the second VML output buffer, which drives the *TXA+/TXA–* output.

The signal applied to the *RXB+/RXB–* input is not fed to any output in this mode.

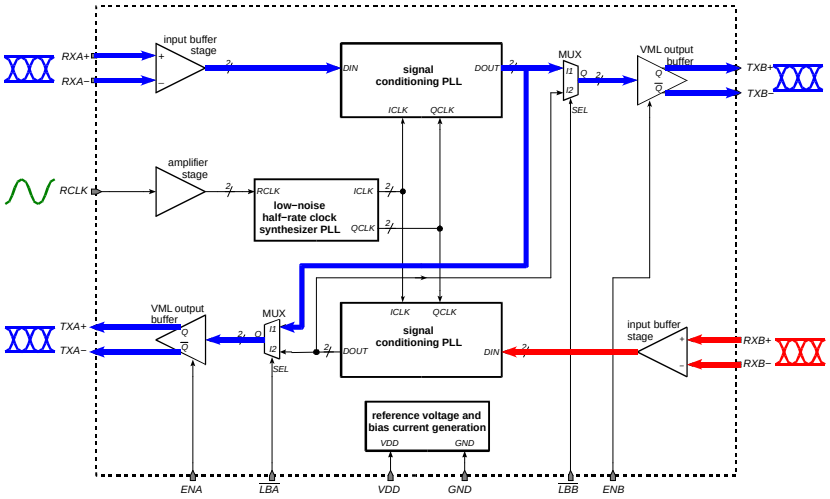


Figure 5. Data Path in Internal Loop-Back Mode A

INTERNAL LOOP-BACK MODE B

In internal loop-back mode B operation, which is activated by pulling the $\overline{\text{LBB}}$ pin low, the input data signal at the *RXB+/RXB–* pins is applied to an input buffer driving a signal conditioning PLL. The retimed output signal is connected to the output pins *TXA+/TXA–* by means of a multiplexer stage and a VML output buffer.

Additionally, by means of a second multiplexer, the same signal is fed to the second VML output buffer, which drives the *TXB+/TXB–* output

OPERATIONAL MODES (continued)

The signals applied to the *RXA+/RXA–* input is not fed to any output in this mode.

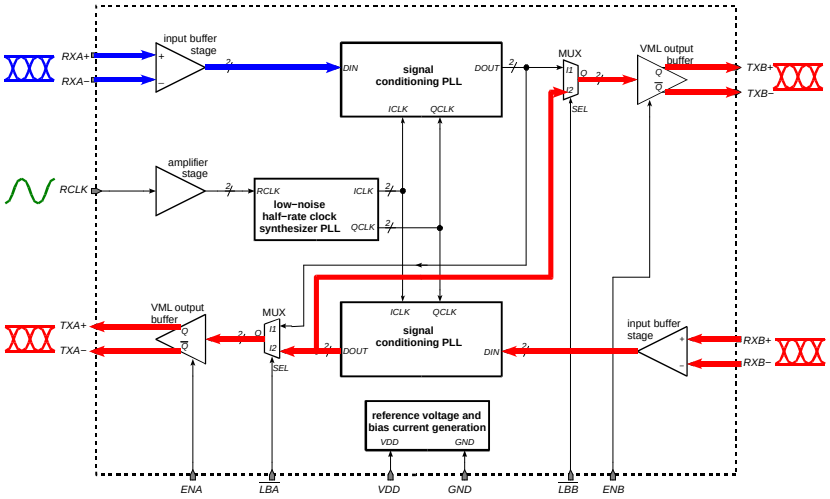


Figure 6. Data Path in Internal Loop-Back Mode B

INTERNAL LOOP-BACK MODES A AND B

If both internal loop-back modes A and B are activated simultaneously, by pulling the $\overline{LBA}$ and the $\overline{LBB}$ pins low, the input data signal at *RXA+/RXA–* is applied to an input buffer driving a signal conditioning PLL. The retimed output signal is fed to the output *TXA+/TXA–* by means of a multiplexer stage and a VML output buffer.

The signals applied to the *RXB+/RXB–* input drives an input buffer connected to a signal conditioning PLL. The retimed output signal is connected to the output pins *TXB+/TXB–* by means of a multiplexer stage and a VML output buffer.

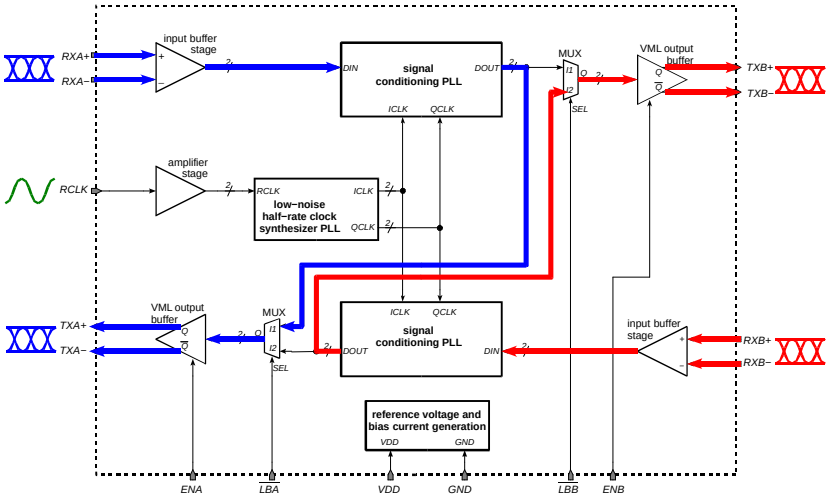


Figure 7. Data Path in Internal Loop-Back Modes A and B

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLK1002ARGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLK 1002A
TLK1002ARGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TLK 1002A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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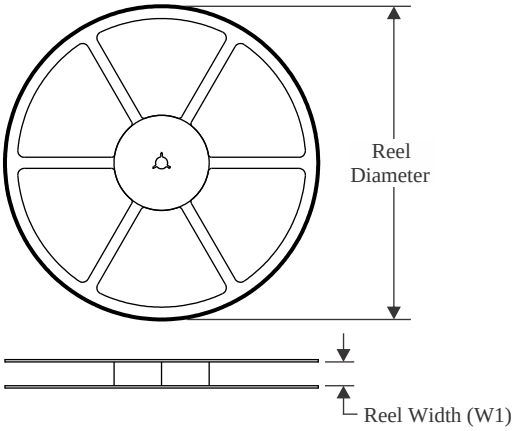
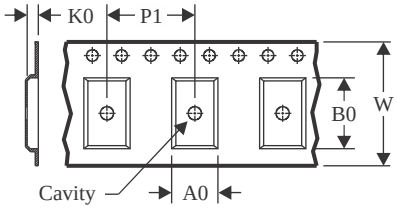
TAPE AND REEL INFORMATION

REEL DIMENSIONS

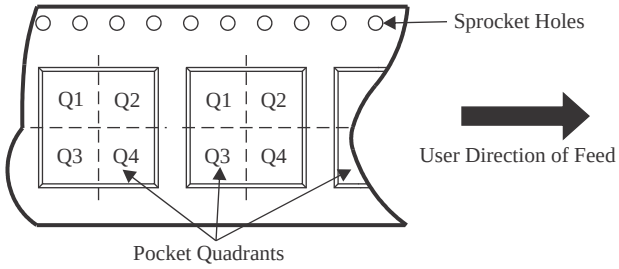


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

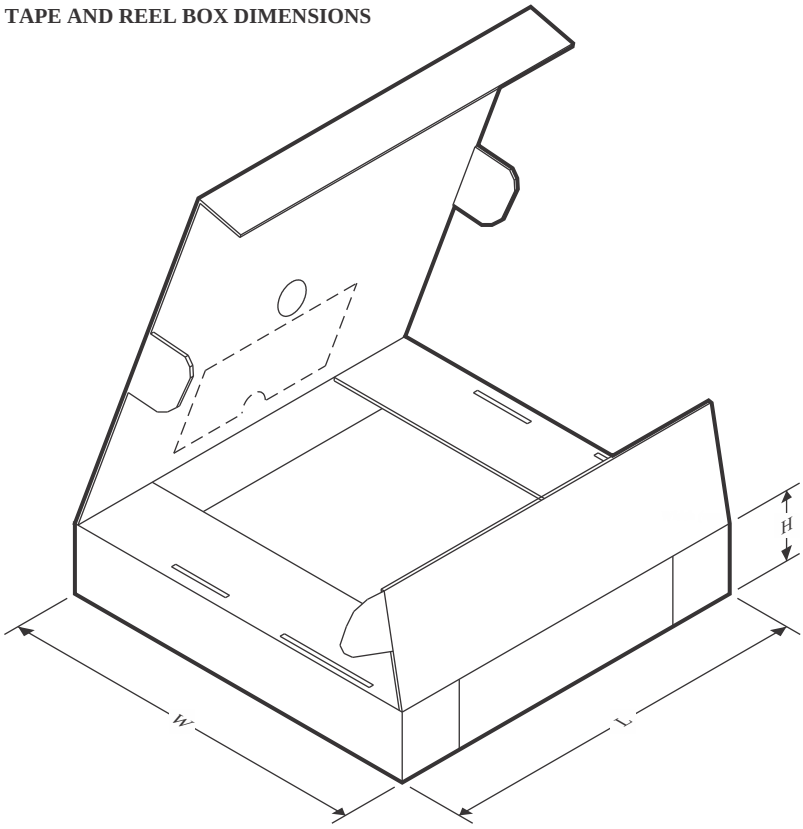
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLK1002ARGET	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



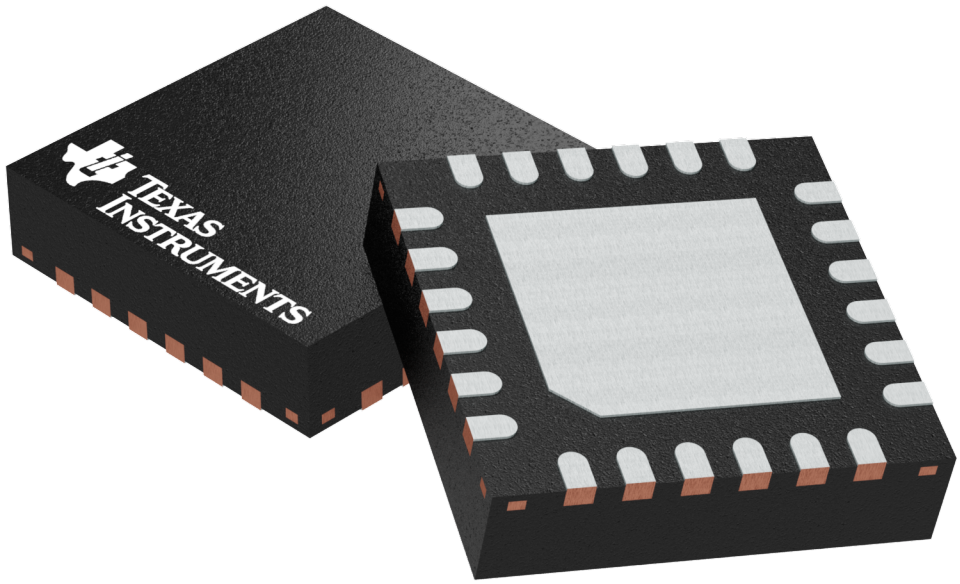
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLK1002ARGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

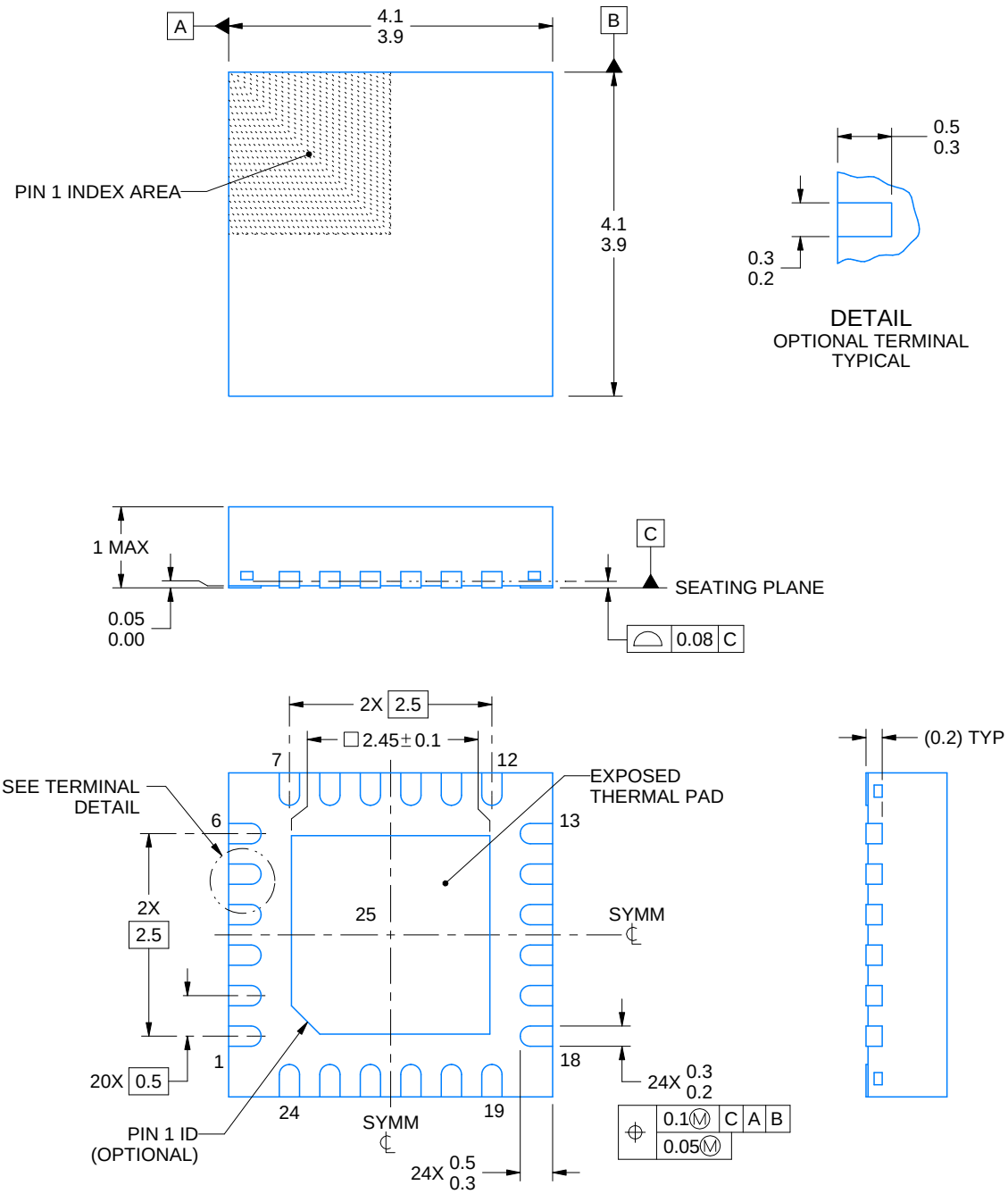
4204104/H

PACKAGE OUTLINE

RGE0024B

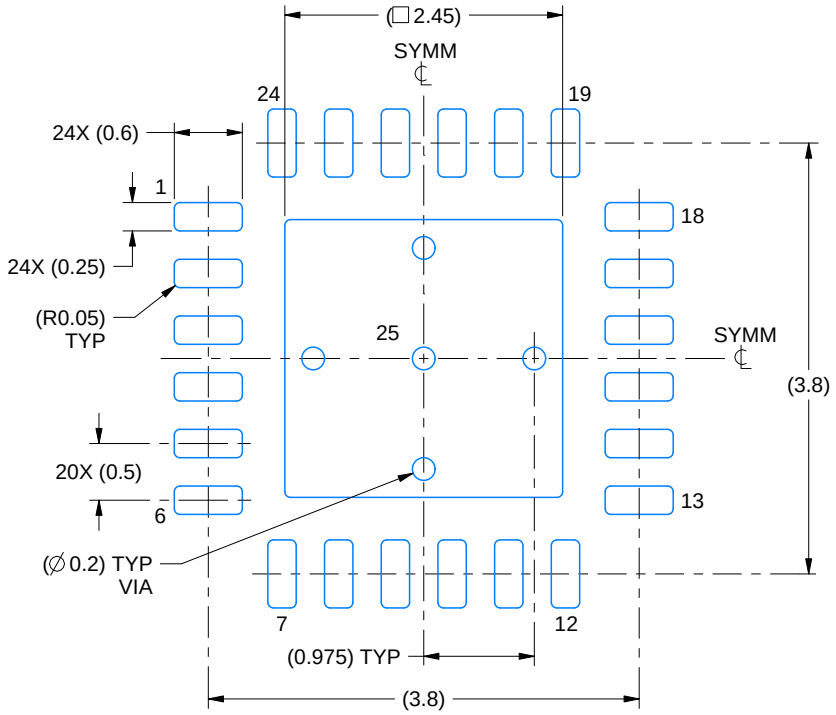
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

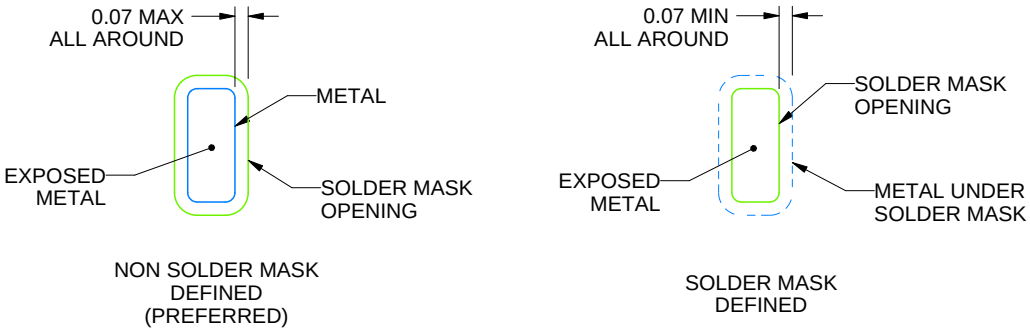


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

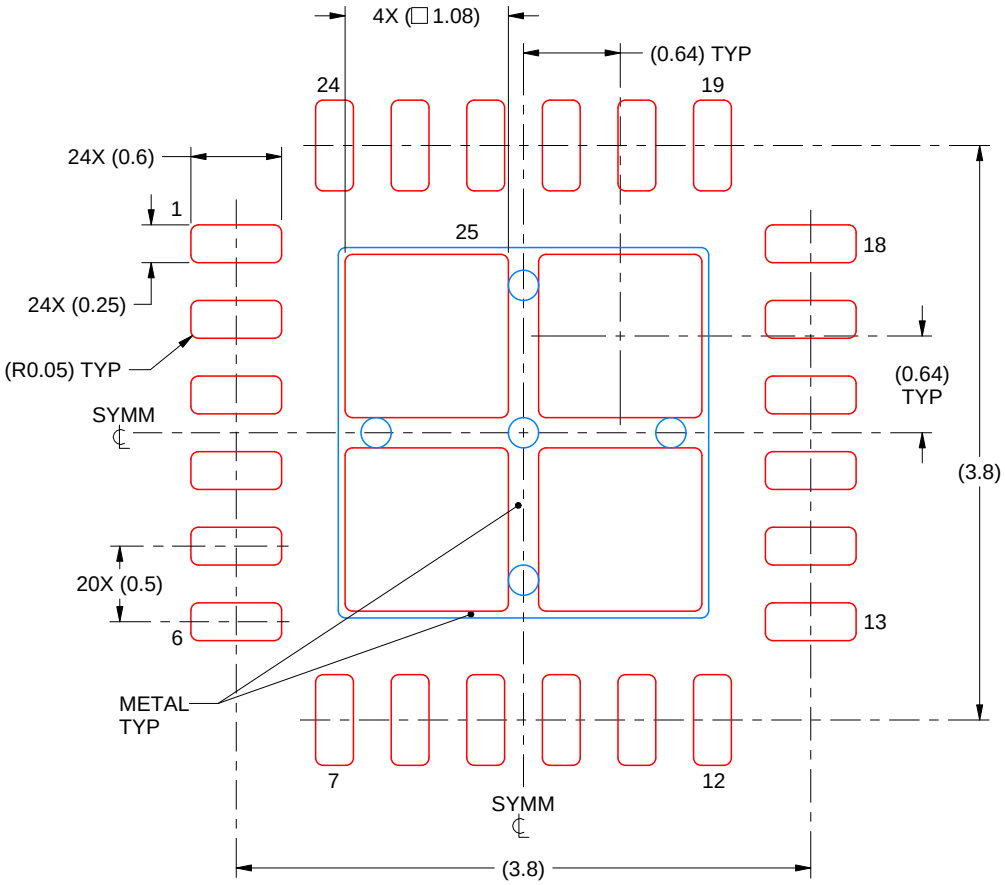


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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