TEXAS INSTRUMENTS
TMP75B-Q1
SBOS721A – OCTOBER 2014 – REVISED JUNE 2022

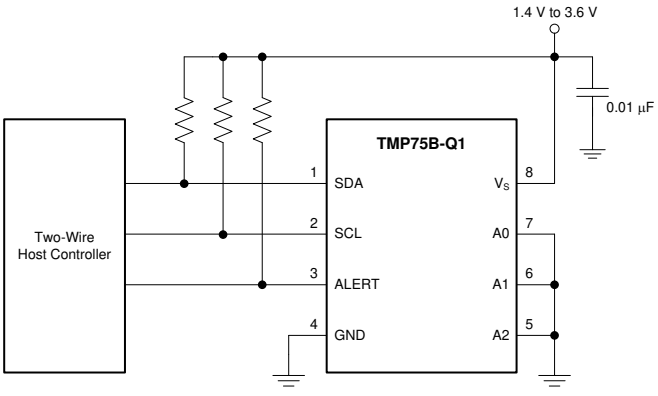
# TMP75B-Q1 1.8-V Digital Temperature Sensor with Two-Wire Interface and Alert

## 1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Temperature grade 1: –40°C to 125°C
  - HBM ESD classification 2
  - CDM ESD classification C4B
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Digital output with two-wire serial interface
- Up to 8 pin-programmable bus addresses
- Programmable overtemperature ALERT
- Shutdown mode for power saving
- One-shot conversion mode
- Operating temperature range: –40°C to 125°C
- Operating supply range: 1.4 V to 3.6 V
- Quiescent current:
  - 45-µA Active (typical)
  - 0.3-µA Shutdown (typical)
- Accuracy:
  - ±0.5°C (typical) from –20°C to 85°C
  - ±1°C (typical) from –40°C to 125°C
- Resolution: 12 bits (0.0625°C)
- Packages: SOIC-8 and VSSOP-8

## 2 Applications

- Automotive embedded systems
- ECU processor temperature monitoring
- TCM processor temperature monitoring
- BCM processor temperature monitoring
- LED headlight thermal control
- Battery thermal protection
- Electrical motor driver thermal protection




**Simplified Schematic**

## 3 Description

The TMP75B-Q1 is an integrated digital temperature sensor with a 12-bit analog-to-digital converter (ADC) that can operate at a 1.8-V supply, and is pin and register compatible with the industry-standard LM75 and TMP75. This device is available in SOIC-8 and VSSOP-8 packages, and requires no external components to sense the temperature. The TMP75B-Q1 is capable of reading temperatures with a resolution of 0.0625°C and is specified over a temperature range of –40°C to 125°C.

The TMP75B-Q1 features SMBus and two-wire interface compatibility, and allows up to eight devices on the same bus with the SMBus overtemperature alert function. The programmable temperature limits and the ALERT pin allow the sensor to operate as a stand-alone thermostat, or an overtemperature alarm for power throttling or system shutdown.

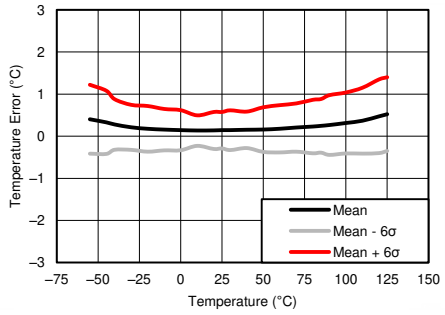
The factory-calibrated temperature accuracy and the noise-immune digital interface make the TMP75B-Q1 the preferred solution for temperature compensation of other sensors and electronic components, without the need for additional system-level calibration or elaborate board layout for distributed temperature sensing.

The TMP75B-Q1 is designed for thermal management and protection of a variety of automotive applications, and is a high-performance alternative to a PCB-mounted NTC thermistor.

**Device Information**(1)

| DEVICE NAME | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TMP75B-Q1 | SOIC (8) | 4.90 mm × 3.90 mm |
| | VSSOP (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.




**Temperature Accuracy (Error) vs. Ambient Temperature**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

| Changes from Revision * (October 2014) to Revision A (June 2022) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Changed all instances of legacy terminology to controller and target where $I^2C$ is mentioned | 1 |
| • Added Functional Safety information to the *Features* section | 1 |


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# 5 Pin Configuration and Functions

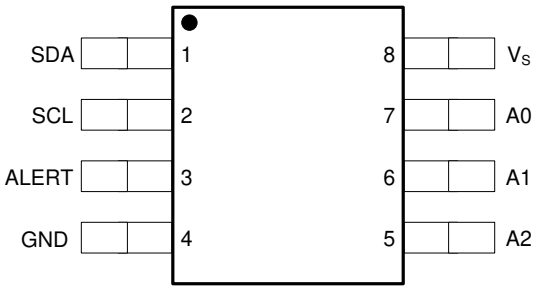


**Figure 5-1. D and DGK Packages 8-Pin SOIC and 8-Pin VSSOP (Top View)**

**Table 5-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| A0 | 7 | I | Address select. Connect to GND or $V_S$. |
| A1 | 6 | I | Address select. Connect to GND or $V_S$. |
| A2 | 5 | I | Address select. Connect to GND or $V_S$. |
| ALERT | 3 | O | Overtemperature alert. Open-drain output; requires a pullup resistor. |
| GND | 4 | — | Ground |
| SCL | 2 | I | Serial clock |
| SDA | 1 | I/O | Serial data. Open-drain output; requires a pullup resistor. |
| $V_S$ | 8 | I | Supply voltage, 1.4 V to 3.6 V |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_S$ | | | 4 | V |
| Input voltage | SDA, SCL, ALERT, A2, A1 | –0.3 | 4 | V |
| | A0 | –0.3 | ($V_S$) + 0.3 | V |
| Sink current | SDA, ALERT | | 10 | mA |
| Operating junction temperature | | –55 | 150 | °C |
| $T_{stg}$ | Storage temperature range | –60 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002[1] | | –2000 | 2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | Corner pins (1, 4, 5, and 8) | –1000 | 1000 | |
| | | | Other pins | –1000 | 1000 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | 1.4 | 1.8 | 3.6 | V |
| Operating free-air temperature, $T_A$ | –40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TMP75B-Q1 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | DGK (VSSOP) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 125.4 | 188.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 71.5 | 79.1 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 65.8 | 109.6 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 21.1 | 15.3 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 65.3 | 108 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.


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## 6.5 Electrical Characteristics

At $T_A$ = –40°C to 125°C and $V_S$ = 1.4 V to 3.6 V, unless otherwise noted. Typical values at $T_A$ = 25°C and $V_S$ = 1.8 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TEMPERATURE INPUT** | | | | | | |
| | Temperature range | | –40 | | 125 | °C |
| | Temperature resolution | | | 0.0625 | | °C |
| | Temperature accuracy (error) | –20°C to 85°C | | ±0.5 | ±2 | °C |
| | | –40°C to 125°C | | ±1 | ±3 | °C |
| **DIGITAL INPUT/OUTPUT** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.7($V_S$) | | $V_S$ | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.3($V_S$) | V |
| $I_{IN}$ | Input current | 0 V < $V_{IN}$ < ($V_S$) + 0.3 V | | | 1 | µA |
| $V_{OL}$ | Low-level output voltage | $V_S$ ≥ 2 V, $I_{OUT}$ = 3 mA | | | 0.4 | V |
| | | $V_S$ < 2 V, $I_{OUT}$ = 3 mA | | | 0.2($V_S$) | V |
| | ADC resolution | | | 12 | | Bit |
| | Conversion time | One-shot mode | 20 | 27 | 35 | ms |
| | Conversion modes | CR1 = 0, CR0 = 0 (default) | | 37 | | Conv/s |
| | | CR1 = 0, CR0 = 1 | | 18 | | Conv/s |
| | | CR1 = 1, CR0 = 0 | | 9 | | Conv/s |
| | | CR1 = 1, CR0 = 1 | | 4 | | Conv/s |
| | Timeout time | | 38 | 54 | 70 | ms |
| **POWER SUPPLY** | | | | | | |
| | Operating supply range | | 1.4 | | 3.6 | V |
| $I_Q$ | Quiescent current | Serial bus inactive, CR1 = 0, CR0 = 0 (default) | | 45 | 89 | µA |
| | | Serial bus inactive, CR1 = 0, CR0 = 1 | | 22 | 48 | µA |
| | | Serial bus inactive, CR1 = 1, CR0 = 0 | | 12 | 30 | µA |
| | | Serial bus inactive, CR1 = 1, CR0 = 1 | | 6.5 | 21 | µA |
| $I_{SD}$ | Shutdown current | Serial bus inactive | | 0.3 | 8 | µA |
| | | Serial bus active, SCL frequency = 400 kHz | | 10 | | µA |
| | | Serial bus active, SCL frequency = 3.4 MHz | | 80 | | µA |

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## 6.6 Typical Characteristics

At $T_A$ = 25°C and $V_S$ = 1.8 V (unless otherwise noted).

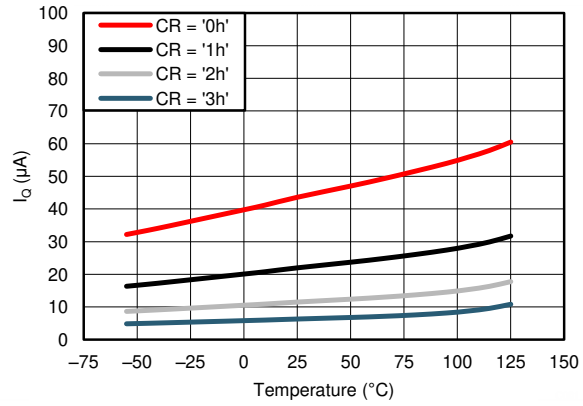


**Figure 6-1. Quiescent Current vs. Temperature**

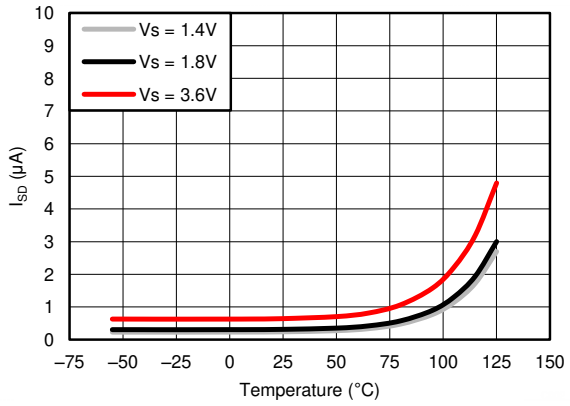


**Figure 6-2. Shutdown Current vs. Temperature**

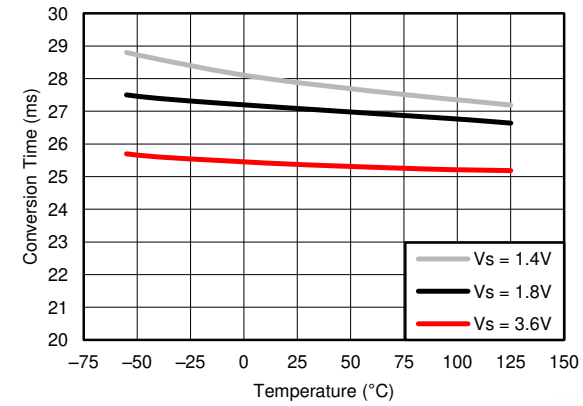


**Figure 6-3. Conversion Time vs. Temperature**

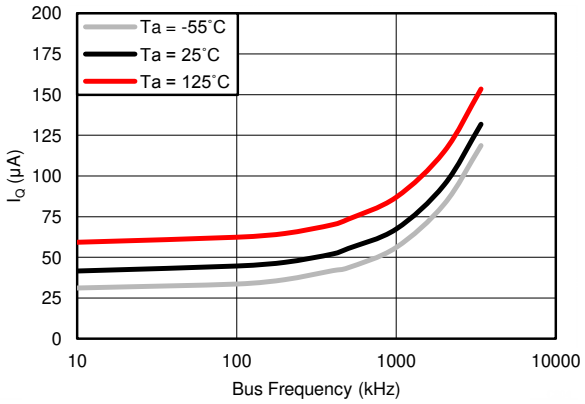


**Figure 6-4. Quiescent Current vs. Bus Frequency**

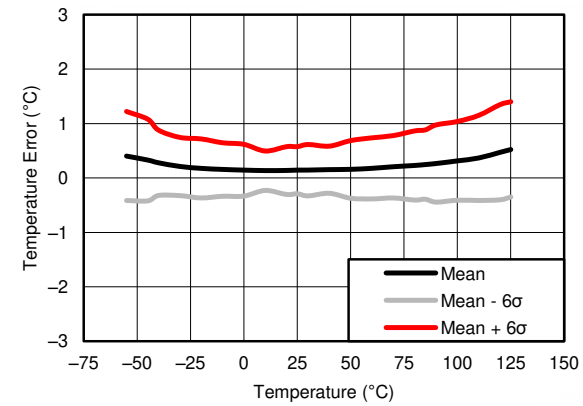


**Figure 6-5. Temperature Error vs. Temperature**

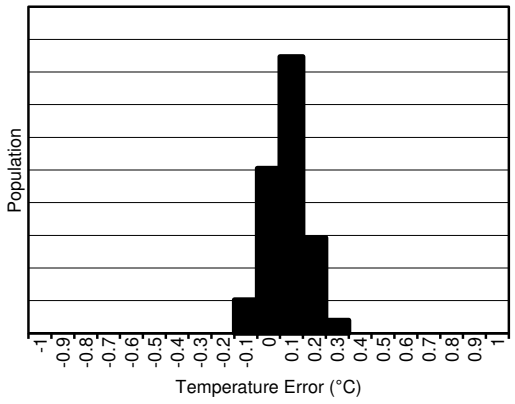


**Figure 6-6. Temperature Error at 25°C**


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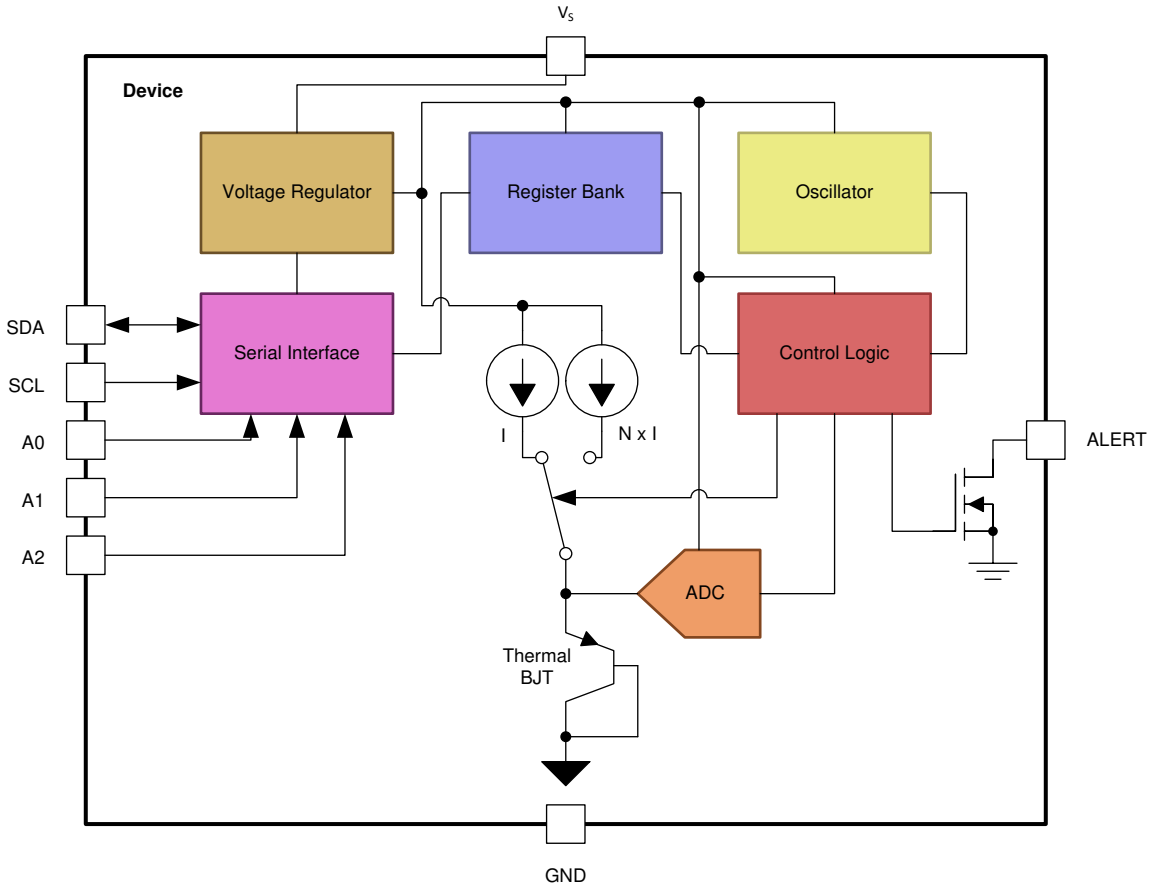
# 7 Detailed Description

## 7.1 Overview

The TMP75B-Q1 is a digital temperature sensor optimal for thermal management and thermal protection applications. The TMP75B-Q1 is two-wire and SMBus interface compatible, and is specified over a temperature range of –40°C to 125°C.

The temperature sensing device for the TMP75B-Q1 is the chip itself. A bipolar junction transistor (BJT) inside the chip is used in a band-gap configuration to produce a voltage proportional to the chip temperature. The voltage is digitized and converted to a 12-bit temperature result in degrees Celsius, with a resolution of 0.0625°C. The package leads provide the primary thermal path because of the lower thermal resistance of the metal. Thus, the temperature result is equivalent to the local temperature of the printed circuit board (PCB) where the sensor is mounted.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Digital Temperature Output

The 12-bit digital output from each temperature measurement conversion is stored in the read-only temperature register. Two bytes must be read to obtain the data; see Figure 7-9. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The temperature result is left-justified with the 12 most significant bits used to indicate the temperature. There is no need to read the second byte if resolution below 1°C is not required. Table 7-1 summarizes the temperature data format. One LSB equals 0.0625°C. Negative numbers are represented in binary twos complement format.

**Table 7-1. Temperature Data Format(1)**

| TEMPERATURE (°C) | DIGITAL OUTPUT | |
|---|---|---|
| | BINARY | HEX |
| 128 | 0111 1111 1111 | 7FF |
| 127.9375 | 0111 1111 1111 | 7FF |
| 100 | 0110 0100 0000 | 640 |
| 80 | 0101 0000 0000 | 500 |
| 75 | 0100 1011 0000 | 4B0 |
| 50 | 0011 0010 0000 | 320 |
| 25 | 0001 1001 0000 | 190 |
| 0.25 | 0000 0000 0100 | 004 |
| 0 | 0000 0000 0000 | 000 |
| –0.25 | 1111 1111 1100 | FFC |
| –25 | 1110 0111 0000 | E70 |
| –55 | 1100 1001 0000 | C90 |

(1) The temperature sensor resolution is 0.0625°C/LSB.

Table 7-1 does not supply a full list of all temperatures. Use the following rules to obtain the digital data format for a given temperature, and vice versa.

To convert positive temperatures to a digital data format:

Divide the temperature by the resolution. Then, convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

Example: (50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:

Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number. Then, multiply the decimal number by the resolution to obtain the positive temperature.

Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = 50°C

To convert negative temperatures to a digital data format:

Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format. Then, generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

Example: (|–25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:

Generate the twos compliment of the 12-bit, left-justified binary number of the temperature result (with MSB = 1, denoting negative temperature result) by complementing the binary number and adding one. This represents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the binary number of the absolute value of the temperature. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by –1 for the negative sign.

Example: 1110 0111 0000 has twos compliment of 0001 1001 0000 = 0001 1000 1111 + 1

Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|–25°C|); (|–25°C|) × (–1) = –25°C

### 7.3.2 Temperature Limits and Alert

The temperature limits are stored in the $T_{LOW}$ and $T_{HIGH}$ registers (Table 7-8 and Table 7-9) in the same format as the temperature result, and their values are compared to the temperature result on every conversion. The outcome of the comparison drives the behavior of the ALERT pin, which can operate as a comparator output or an interrupt, and is set by the TM bit in the configuration register (Table 7-7).

In comparator mode (TM = 0, default), the ALERT pin becomes active when the temperature is equal to or exceeds the value in $T_{HIGH}$ (fault conditions) for a consecutive number of conversions as set by the FQ bits of the configuration register. ALERT clears when the temperature falls below $T_{LOW}$ for the same consecutive number of conversions. The difference between the two limits acts as a hysteresis on the comparator output, and a fault counter prevents false alerts as a result of environmental noise.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds the value in $T_{HIGH}$ for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode (see the *Shutdown Mode* section for shutdown mode description). After the ALERT pin is cleared, this pin becomes active again only when the temperature falls below $T_{LOW}$ for a consecutive number of fault conditions, and remains active until cleared by a read operation of any register, or a successful response to the SMBus alert response address. After the ALERT pin is cleared, the cycle repeats with the ALERT pin becoming active when the temperature equals or exceeds $T_{HIGH}$, and so on. The ALERT pin can also be cleared by resetting the device with the general-call reset command. This action also clears the state of the internal registers in the device and the fault counter memory, returning the device to comparator mode (TM = 0).

The active state of the ALERT pin is set by the POL bit in the configuration register. When POL = 0 (default), the ALERT pin is active low. When POL = 1, the ALERT pin is active high. The operation of the ALERT pin in various modes is shown in Figure 7-1.

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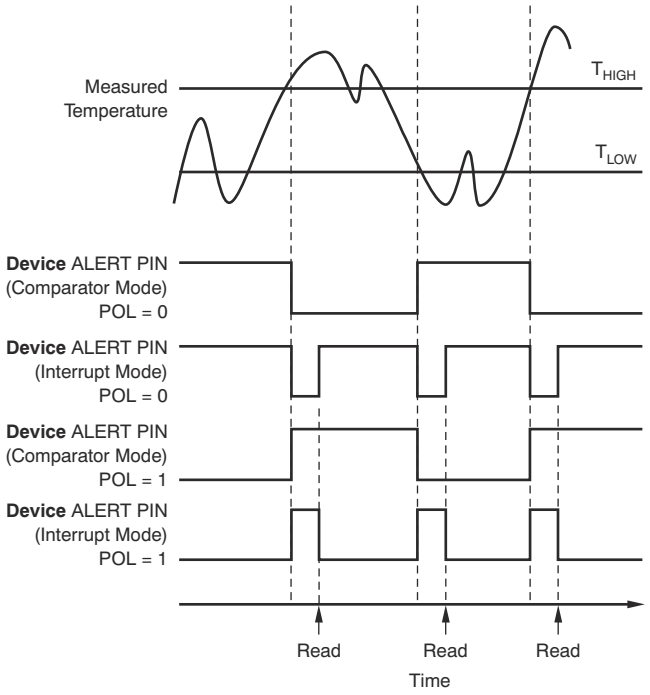


**Figure 7-1. ALERT Pin Modes of Operation**


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### 7.3.3 Serial Interface

The TMP75B-Q1 operates as a target device only on the two-wire bus and SMBus. Connections to the bus are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP75B-Q1 supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3 MHz) modes. All data bytes are transmitted MSB first.

#### *7.3.3.1 Bus Overview*

The device that initiates the transfer is called a *controller*, and the devices controlled by the controller are *targets*. The bus must be controlled by a controller device that generates the serial clock (SCL), controls the bus access, and generates the start and stop conditions.

To address a specific device, initiate a start condition by pulling the data line (SDA) from a high to a low logic level while SCL is high. All targets on the bus shift in the target address byte; the last bit indicates whether a read or write operation follows. During the ninth clock pulse, the target being addressed responds to the controller by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high because any change in SDA while SCL is high is interpreted as a start or stop signal.

After all data have been transferred, the controller generates a stop condition indicated by pulling SDA from low to high, while SCL is high.

#### *7.3.3.2 Serial Bus Address*

To communicate with the TMP75B-Q1, the controller must first communicate with target devices using a target address byte. The target address byte consists of seven address bits, and a direction bit indicating the intent of executing either a read or write operation. The TMP75B-Q1 features three address pins that allow up to eight devices to be addressed on a single bus. The TMP75B-Q1 latches the status of the address pins at the start of a communication. Table 7-2 describes the pin logic levels and the corresponding address values.

**Table 7-2. Address Pin Connections and Target Addresses**

| DEVICE TWO-WIRE ADDRESS | A2 | A1 | A0 |
|---|---|---|---|
| 1001000 | GND | GND | GND |
| 1001001 | GND | GND | $V_S$ |
| 1001010 | GND | $V_S$ | GND |
| 1001011 | GND | $V_S$ | $V_S$ |
| 1001100 | $V_S$ | GND | GND |
| 1001101 | $V_S$ | GND | $V_S$ |
| 1001110 | $V_S$ | $V_S$ | GND |
| 1001111 | $V_S$ | $V_S$ | $V_S$ |

#### *7.3.3.3 Writing and Reading Operation*

Accessing a particular register on the TMP75B-Q1 is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the target address byte with the R/W bit low. Every write operation to the TMP75B-Q1 requires a value for the pointer register (see Figure 7-3).

When reading from the TMP75B-Q1, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a target address byte with the R/W bit low, followed by the pointer register byte. No additional data are required. The controller can then generate a start condition and send the target address byte with the R/W bit high to initiate the read command. See Figure 7-4 for details of this sequence. If repeated reads from the same register are desired, there is no

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need to continually send the pointer register bytes because the TMP75B-Q1 stores the pointer register value until it is changed by the next write operation.

Note that register bytes are sent with the most significant byte first, followed by the least significant byte.

#### *7.3.3.4 Target-Mode Operations*

The TMP75B-Q1 can operate as a target receiver or target transmitter.

##### 7.3.3.4.1 Target Receiver Mode:

The first byte transmitted by the controller is the target address, with the R/W bit low. The TMP75B-Q1 then acknowledges reception of a valid address. The next byte transmitted by the controller is the pointer register. The TMP75B-Q1 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP75B-Q1 acknowledges reception of each data byte. The controller can terminate data transfer by generating a start or stop condition.

##### 7.3.3.4.2 Target Transmitter Mode:

The first byte transmitted by the controller is the target address, with the R/W bit high. The target acknowledges reception of a valid target address. The next byte is transmitted by the target and is the most significant byte of the register indicated by the pointer register. The controller acknowledges reception of the data byte. The next byte transmitted by the target is the least significant byte. The controller acknowledges reception of the data byte. The controller can terminate data transfer by generating a not-acknowledge bit on reception of any data byte, or by generating a start or stop condition.

#### *7.3.3.5 SMBus Alert Function*

The TMP75B-Q1 supports the SMBus alert function. When the TMP75B-Q1 operates in interrupt mode (TM = 1), the ALERT pin may be connected as an SMBus alert signal. When a controller senses that an alert condition is present on the ALERT line, the controller sends an SMBus alert command (00011001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus alert command and responds by returning its target address on the SDA line. The eighth bit (LSB) of the target address byte indicates whether the alert condition is caused by the temperature exceeding $T_{HIGH}$ or falling below $T_{LOW}$. The LSB is high if the temperature is greater than $T_{HIGH}$, or low if the temperature is less than $T_{LOW}$. See Figure 7-5 for details of this sequence.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the target address portion of the SMBus alert command determines which device clears its alert status first. If the TMP75B-Q1 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus alert command. If the TMP75B-Q1 loses the arbitration, its ALERT pin remains active.

#### *7.3.3.6 General Call*

The TMP75B-Q1 responds to a two-wire general call address (0000000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000100, the TMP75B-Q1 latches the status of the address pin, but does not reset. If the second byte is 00000110, the TMP75B-Q1 internal registers are reset to power-up values.

#### *7.3.3.7 High-Speed (Hs) Mode*

In order for the two-wire bus to operate at frequencies above 400 kHz, the controller device must issue an SMBus Hs-mode controller code (00001xxx) as the first byte after a start condition to switch the bus to high-speed operation. The TMP75B-Q1 does not acknowledge this byte, but does switch its input filters on SDA and SCL and its output filters on SDA to operate in Hs-mode, allowing transfers at up to 3 MHz. After the Hs-mode controller code has been issued, the controller transmits a two-wire target address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a stop condition occurs on the bus. Upon receiving the stop condition, the TMP75B-Q1 switches the input and output filters back to fast-mode operation.

#### *7.3.3.8 Timeout Function*

The TMP75B-Q1 resets the serial interface if SCL or SDA are held low for 54 ms (typical) between a start and stop condition. If the TMP75B-Q1 is pulled low, it releases the bus and then waits for a start condition. To avoid


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activating the timeout function, it is necessary to maintain a communication speed of at least 1 kHz for the SCL operating frequency.

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### 7.3.3.9 Two-Wire Timing

The TMP75B-Q1 is two-wire and SMBus compatible. Figure 7-2 to Figure 7-5 describe the various operations on the TMP75B-Q1. Parameters for Figure 7-2 are defined in Table 7-3. Bus definitions are:

**Bus Idle** Both SDA and SCL lines remain high.

**Start Data Transfer** A change in the state of the SDA line, from high to low, while the SCL line is high defines a start condition. Each data transfer is initiated with a start condition.

**Stop Data Transfer** A change in the state of the SDA line from low to high while the SCL line is high defines a stop condition. Each data transfer is terminated with a repeated start or stop condition.

**Data Transfer** The number of data bytes transferred between a start and a stop condition is not limited, and is determined by the controller device.

The receiver acknowledges the transfer of data. It is also possible to use the TMP75B-Q1 for single-byte updates. To update only the MS byte, terminate communication by issuing a start or stop condition on the bus.

**Acknowledge** Each receiving device, when addressed, must generate an acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a controller receives data, the termination of the data transfer can be signaled by the controller generating a *not-acknowledge* (1) on the last byte transmitted by the target.

**Table 7-3. Timing Diagram Requirements**

| PARAMETER | | | FAST MODE | | HIGH-SPEED MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{(SCL)}$ | SCL operating frequency | $V_S \geq 1.8$ V | 0.001 | 0.4 | 0.001 | 3 | MHz |
| | | $V_S < 1.8$ V | 0.001 | 0.4 | 0.001 | 2.5 | MHz |
| $t_{(BUF)}$ | Bus free time between stop and start conditions | $V_S \geq 1.8$ V | 1300 | | 160 | | ns |
| | | $V_S < 1.8$ V | 1300 | | 260 | | ns |
| $t_{(HDSTA)}$ | Hold time after repeated start condition. After this period, the first clock is generated. | | 600 | | 160 | | ns |
| $t_{(SUSTA)}$ | Repeated start condition setup time | | 600 | | 160 | | ns |
| $t_{(SUSTO)}$ | Stop condition setup time | | 600 | | 160 | | ns |
| $t_{(HDDAT)}$ | Data hold time | $V_S \geq 1.8$ V | 0 | 900 | 0 | 100 | ns |
| | | $V_S < 1.8$ V | 0 | 900 | 0 | 140 | ns |
| $t_{(SUDAT)}$ | Data setup time | $V_S \geq 1.8$ V | 100 | | 10 | | ns |
| | | $V_S < 1.8$ V | 100 | | 20 | | ns |
| $t_{(LOW)}$ | SCL clock low period | $V_S \geq 1.8$ V | 1300 | | 190 | | ns |
| | | $V_S < 1.8$ V | 1300 | | 240 | | ns |
| $t_{(HIGH)}$ | SCL clock high period | | 600 | | 60 | | ns |
| $t_{R(SDA)}$, $t_{F(SDA)}$ | Data rise and fall time | | | 300 | | 80 | ns |
| $t_{R(SCL)}$, $t_{F(SCL)}$ | Clock rise and fall time | | | 300 | | 40 | ns |
| $t_R$ | Clock and data rise time for SCLK ≤ 100 kHz | | | 1000 | | | ns |


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### 7.3.3.10 Two-Wire Timing Diagrams

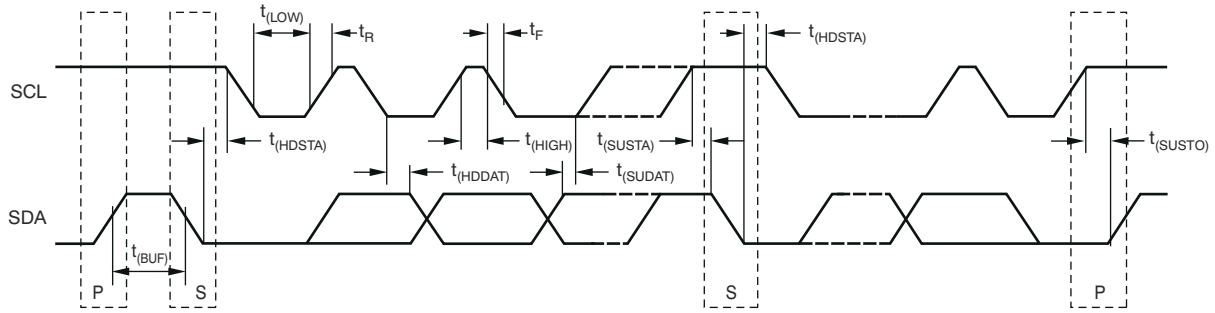
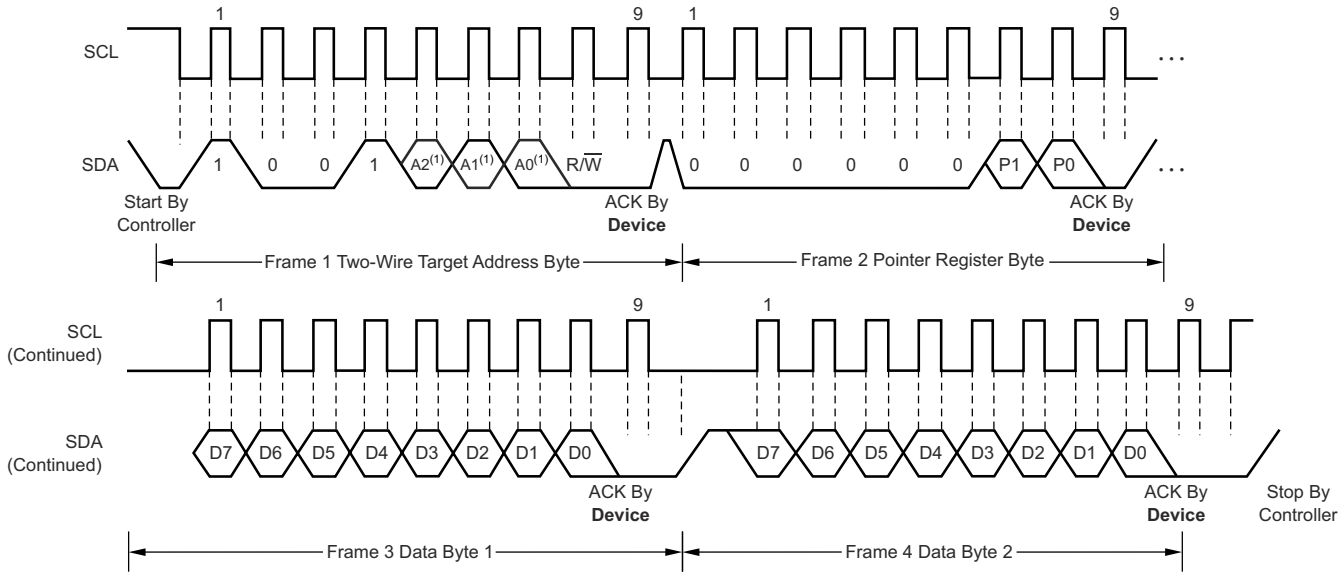
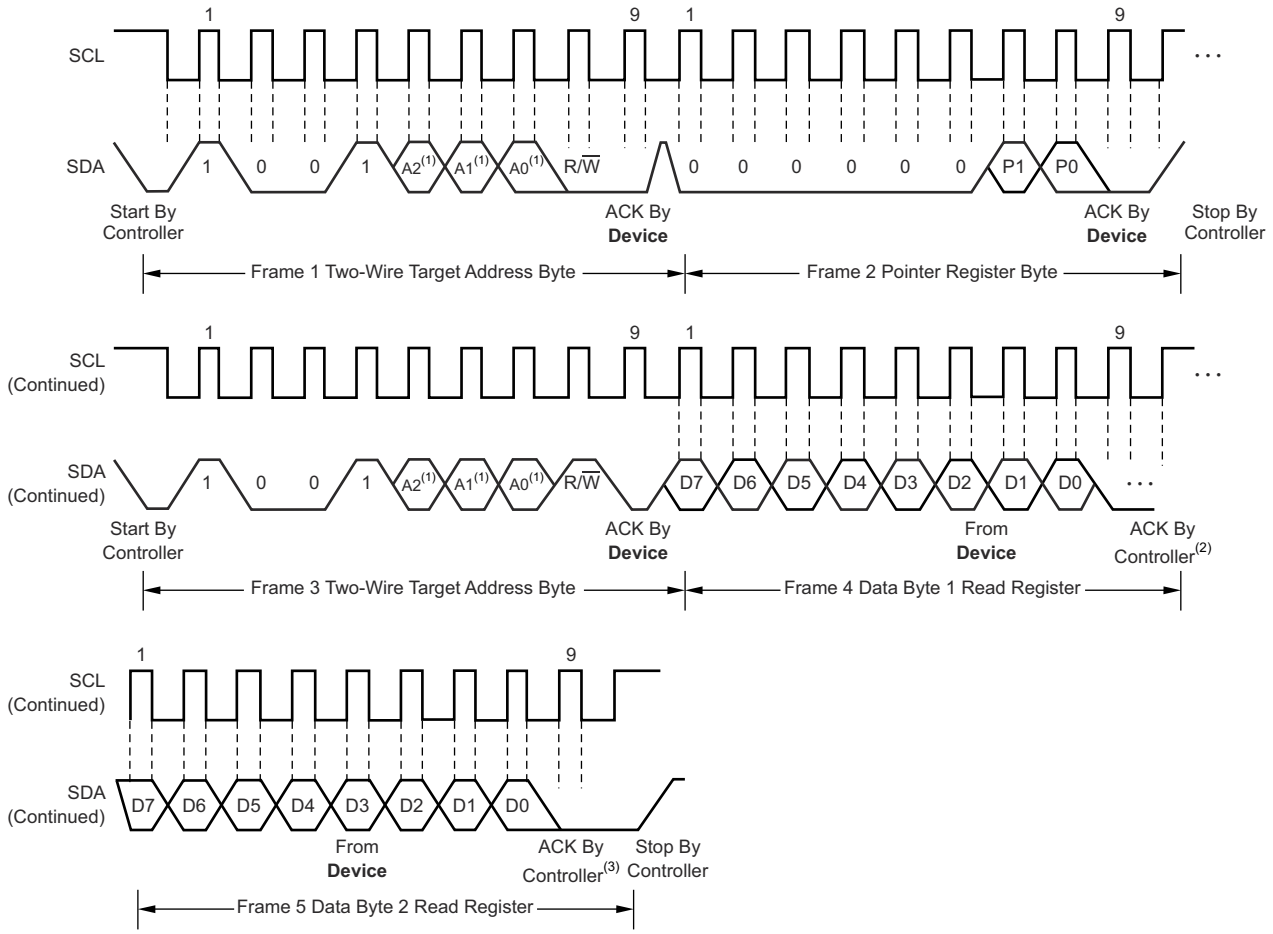



**Figure 7-2. Two-Wire Timing Diagram**



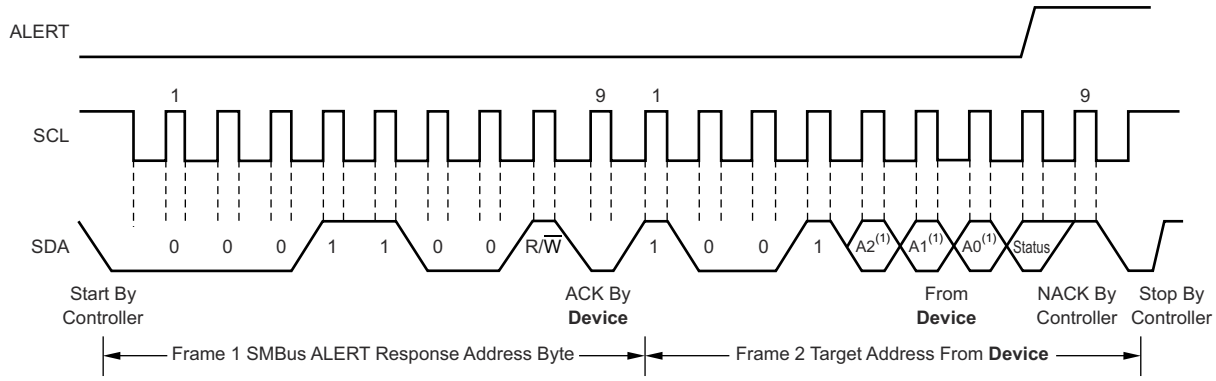

A. The value of A0, A1, and A2 are determined by the connections of the corresponding pins.

**Figure 7-3. Two-Wire Timing Diagram for Write Word Format**




A. The value of A0, A1, and A2 are determined by the connections of the corresponding pins.
B. Controller should leave SDA high to terminate a single-byte read operation.
C. Controller should leave SDA high to terminate a two-byte read operation.

**Figure 7-4. Two-Wire Timing Diagram for Read Word Format**




A. The value of A0, A1, and A2 are determined by the connections of the corresponding pins.

**Figure 7-5. Timing Diagram for SMBus Alert**

## 7.4 Device Functional Modes

### 7.4.1 Continuous-Conversion Mode

The default mode of the TMP75B-Q1 is continuous conversion, where the ADC performs continuous temperature conversions and stores each result to the temperature register, overwriting the result from the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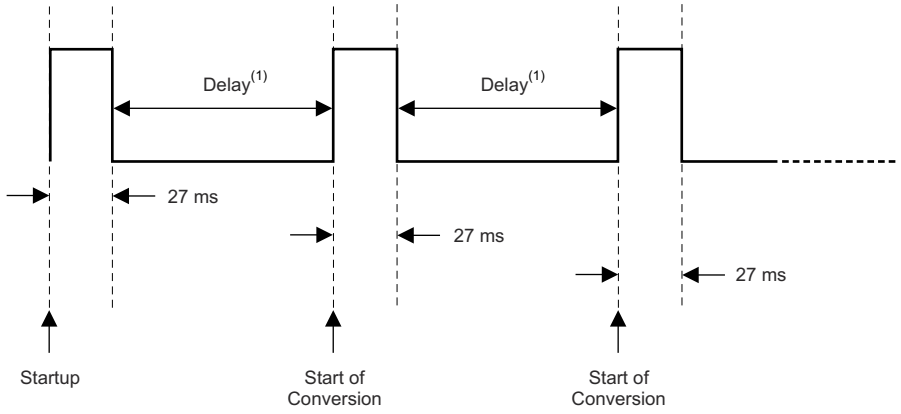
previous conversion. Conversion rate bits CR1 and CR0 in the configuration register configure the TMP75B-Q1 for typical conversion rates of 37 Hz, 18 Hz, 9 Hz, or 4 Hz. The TMP75B-Q1 has a typical conversion time of 27 ms. To achieve different conversion rates, the TMP75B-Q1 makes a conversion, and then powers down and waits for the appropriate delay set by CR1 and CR0. The default rate is 37 Hz (no delay between conversions).Table 7-4 shows the settings for CR1 and CR0.

**Table 7-4. Conversion Rate Settings**

| CR1 | CR0 | CONVERSION RATE (TYP) | $I_Q$ (TYP) |
|---|---|---|---|
| 0 | 0 | 37 Hz (continuous conversion, default) | 45 µA |
| 0 | 1 | 18 Hz | 22 µA |
| 1 | 0 | 9 Hz | 12 µA |
| 1 | 1 | 4 Hz | 6.5 µA |

After power-up or a general-call reset, the TMP75B-Q1 immediately starts a conversion, as shown in Figure 7-6. The first result is available after 27 ms (typical). The active quiescent current during conversion is 45 µA (typical at 25°C). The quiescent current during delay is 1 µA (typical at 25°C).




A. Delay is set by the CR bits in the configuration register.

**Figure 7-6. Conversion Start**

### 7.4.2 Shutdown Mode

Shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, and reduces current consumption to typically less than 0.3 µA. Shutdown mode is enabled when the SD bit in the configuration register is set to 1; the device shuts down after the current conversion is completed. When SD is equal to 0, the device operates in continuous-conversion mode. When shutdown mode is enabled, the ALERT pin and fault counter clear in both comparator and interrupt modes; however, this clearing occurs with the rising edge of the shutdown signal. After shutdown is enabled, reprogramming shutdown does not clear the ALERT pin and the fault counter until a rising edge is generated on the shutdown signal.

### 7.4.3 One-Shot Mode

The TMP75B-Q1 features a *one-shot* temperature measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This mode reduces power consumption in the TMP75B-Q1 when continuous temperature monitoring is not required. When the configuration register is read, the OS bit always reads zero.

## 7.5 Programming

Figure 7-7 shows the internal register structure of the TMP75B-Q1. Use the 8-bit pointer register to address a given data register. The pointer register uses the two LSBs to identify which of the data registers respond to a read or write command. Figure 7-8 identifies the bits of the pointer register byte.

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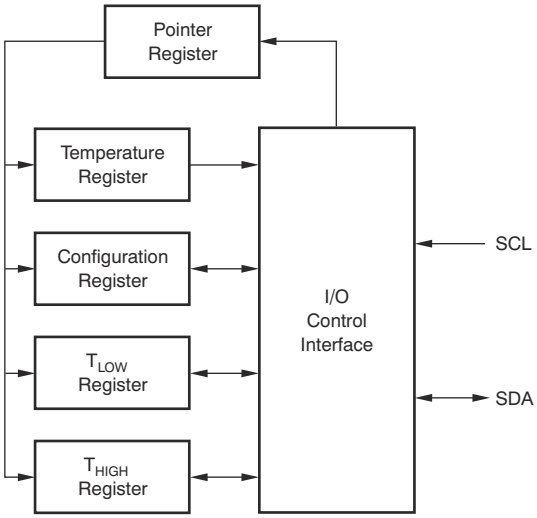


**Figure 7-7. Internal Register Structure**


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## 7.6 Register Map

Table 7-5 describes the registers available in the TMP75B-Q1 with their pointer addresses, followed by the description of the bits in each register.

**Table 7-5. Register Map and Pointer Addresses**

| P1 | P0 | REGISTER |
|---|---|---|
| 0 | 0 | Temperature register (read only, default) |
| 0 | 1 | Configuration register (read/write) |
| 1 | 0 | $T_{LOW}$ register (read/write) |
| 1 | 1 | $T_{HIGH}$ register (read/write) |

**Figure 7-8. Pointer Register (pointer = N/A) [reset = 00h]**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **Reserved** | | | | | | P1 | P0 |
| W-0h | | | | | | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

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**Figure 7-9. Temperature Register (pointer = 0h) [reset = 0000h]**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T3 | T2 | T1 | T0 | **Reserved** | | | |
| R-0h | | | | R-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-6. Temperature Register Description**

| Name | Description |
|---|---|
| T11 to T4 | The 8 MSBs of the temperature result (resolution of 1°C) |
| T3 to T0 | The 4 LSBs of the temperature result (resolution of 0.0625°C) |

**Figure 7-10. Configuration Register (pointer = 1h) [reset = 00FFh]**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| OS | CR | | FQ | | POL | TM | SD |
| R/W-0h | R/W-0h | | R/W-0h | | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Reserved** | | | | | | | |
| R-FFh | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7-7. Configuration Register Description**

| Name | Description |
|---|---|
| OS | One-shot mode<br>In shutdown (SD = 1), write 1 to start a conversion. OS always reads back 0. |
| CR | Conversion rate control<br>CR = 0h: 37-Hz conversion rate (typ) (default)<br>CR = 1h: 18-Hz conversion rate (typ)<br>CR = 2h: 9-Hz conversion rate (typ)<br>CR = 3h: 4-Hz conversion rate (typ) |
| FQ | Fault queue to trigger the ALERT pin<br>FQ = 0h: 1 fault (default)<br>FQ = 1h: 2 faults<br>FQ = 2h: 4 faults<br>FQ = 3h: 6 faults |
| POL | ALERT polarity control<br>POL = 0: ALERT is active low (default)<br>POL = 1: ALERT is active high |
| TM | ALERT thermostat mode control<br>TM = 0: ALERT is in comparator mode (default)<br>TM = 1: ALERT is in interrupt mode |
| SD | Shutdown control bit<br>SD = 0: Device is in continuous conversion mode (default)<br>SD = 1: Device is in shutdown mode |

**Figure 7-11. $T_{LOW}$: Temperature Low Limit Register (pointer = 2h) [reset = 4B00h]**[(1)]

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|


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**Figure 7-11. $T_{LOW}$: Temperature Low Limit Register (pointer = 2h) [reset = 4B00h](1) (continued)**

| L11 | L10 | L9 | L8 | L7 | L6 | L5 | L4 |
|---|---|---|---|---|---|---|---|
| R/W-4Bh | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| L3 | L2 | L1 | L0 | **Reserved** | | | |
| R/W-0h | | | | R-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) 4B00h = 75°C.

**Table 7-8. $T_{LOW}$ Register Description**

| Name | Description |
|---|---|
| L11 to L4 | The 8 MSBs of the temperature low limit (resolution of 1°C) |
| L3 to L0 | The 4 LSBs of the temperature low limit (resolution of 0.0625°C) |

**Figure 7-12. $T_{HIGH}$: Temperature High Limit Register (pointer = 3h) [reset = 5000h](1)**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| H11 | H10 | H9 | H8 | H7 | H6 | H5 | H4 |
| R/W-50h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| H3 | H2 | H1 | H0 | **Reserved** | | | |
| R/W-0h | | | | R-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) 5000h = 80°C.

**Table 7-9. $T_{HIGH}$ Register Description**

| Name | Description |
|---|---|
| H11 to H4 | The 8 MSBs of the temperature high limit (resolution of 1°C) |
| H3 to H0 | The 4 LSBs of the temperature high limit (resolution of 0.0625°C) |

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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The TMP75B-Q1 is used to measure the PCB temperature of the location it is mounted. The programmable address options allow up to eight locations on the board to be monitored on a single serial bus. Connecting the ALERT pins together and programming the temperature limit registers to desired values allows for a temperature watchdog operation of all devices, interrupting the host controller only if the temperature exceeds the limits.

## 8.2 Typical Application

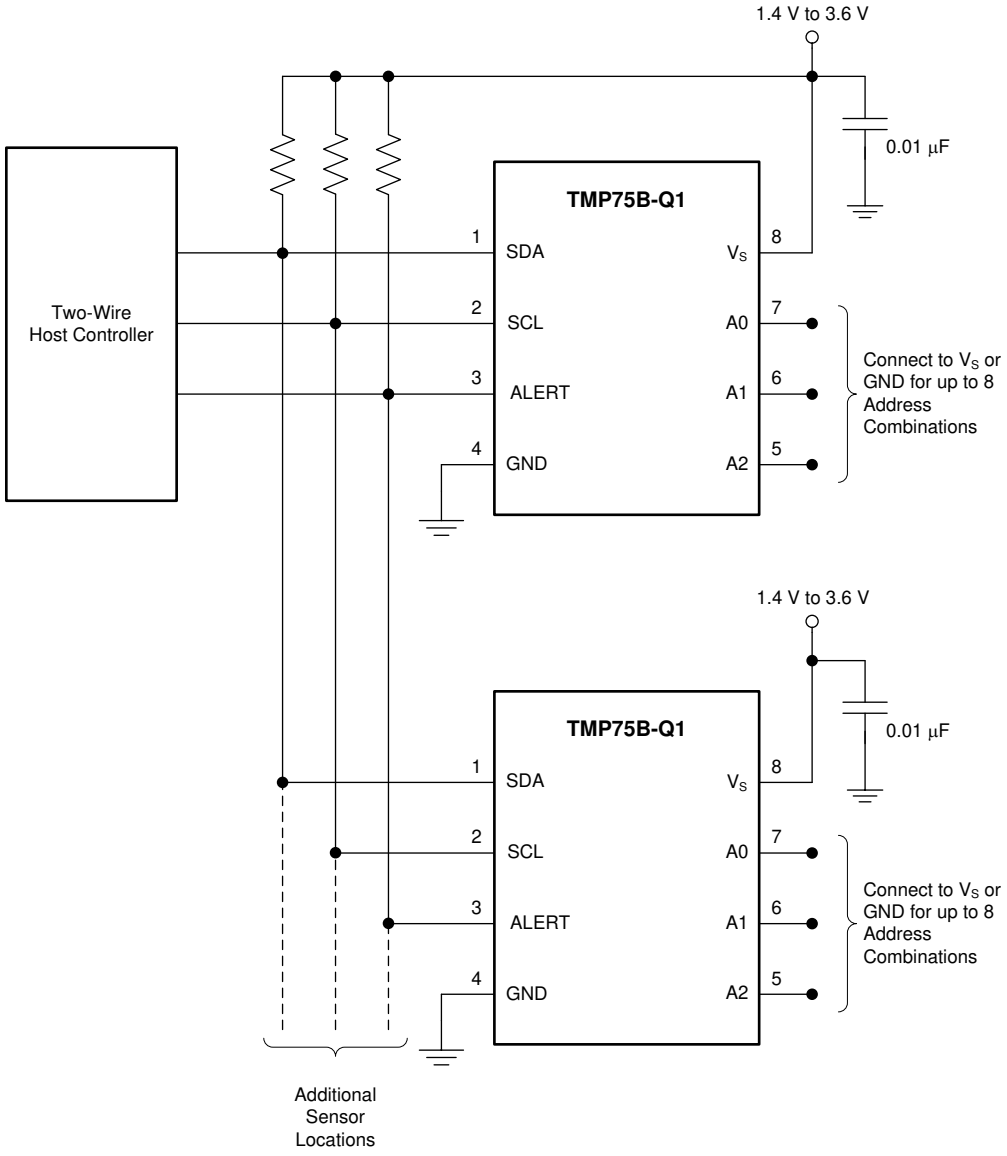


**Figure 8-1. Temperature Monitoring of Multiple Locations on a PCB**


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### 8.2.1 Design Requirements

The TMP75B-Q1 only requires pullup resistors on SDA and ALERT, although a pullup resistor is typically present on the SCL as well. A 0.01-µF bypass capacitor on the supply is recommended, as shown in Figure 8-1. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than $V_S$ through the pullup resistors. To configure one of eight different addresses on the bus, connect A0, A1, and A2 to either $V_S$ or GND.

### 8.2.2 Detailed Design Procedure

The TMP75B-Q1 should be placed in close proximity to the heat source to be monitored, with a proper layout for good thermal coupling. This ensures that temperature changes are captured within the shortest possible time interval.

### 8.2.3 Application Curve

Figure 8-2 shows the step response of the TMP75B-Q1 to a submersion in an oil bath of 100°C from room temperature (27°C). The time-constant, or the time for the output to reach 63% of the input step, is 1.5 seconds.

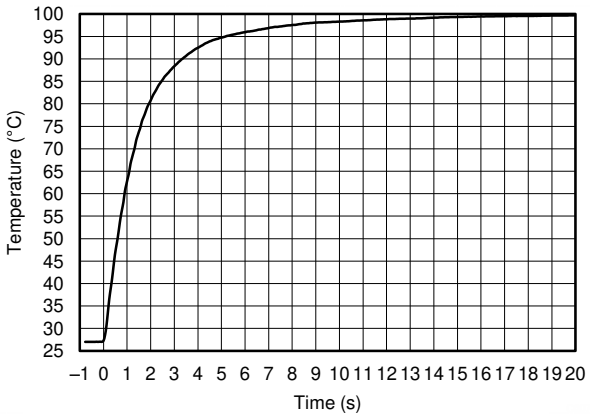


**Figure 8-2. Temperature Step Response**

## 9 Power-Supply Recommendations

The TMP75B-Q1 operates with power supply in the range of 1.4 V to 3.6 V. It is optimized for operation at 1.8-V supply but can measure temperature accurately in the full supply range.

A power-supply bypass capacitor is recommended; place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

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# 10 Layout

## 10.1 Layout Guidelines

Place the temperature sensor as close as possible and run copper planes on the ground or other layers to ensure good thermal coupling to the heat source for fast settling and accurate measurement of the temperature of the hot spot.

Place the power-supply bypass capacitor as close as possible to the supply and ground pins.

Pull up the open-drain output pins (SDA and ALERT) to a supply voltage rail ($V_S$ or higher but up to 3.6 V) through 10-kΩ pullup resistors. Smaller values of the resistors can be used to compensate for long bus traces that can cause an increase in capacitance and slow rise time for the open-drain outputs; the values should not be less than 1kΩ to avoid self-heating effects due to increased current through the part in the low states of the outputs.

## 10.2 Layout Example

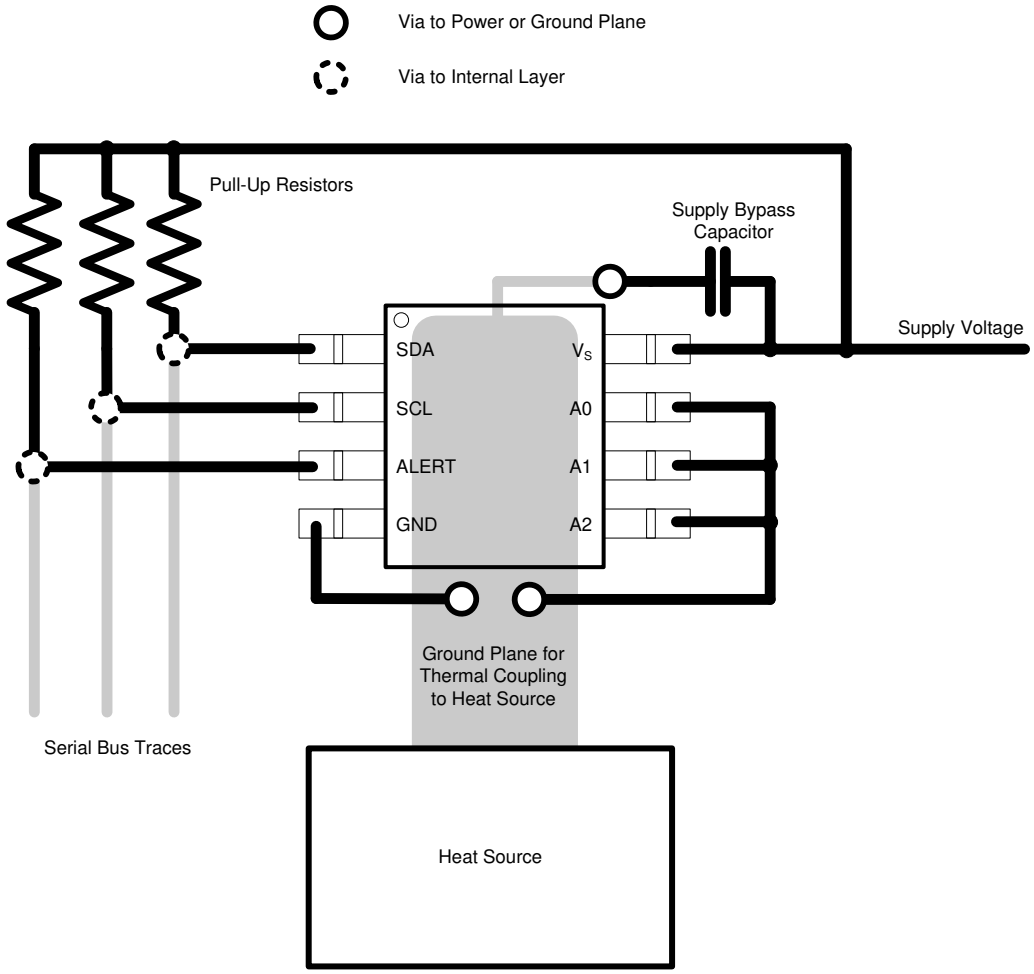


**Figure 10-1. Layout Example**


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# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

SBOU141 — TMP75xEVM User's Guide

## 11.2 Trademarks

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# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMP75BQDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | T75BQ | Samples |
| TMP75BQDGKTQ1 | OBSOLETE | VSSOP | DGK | 8 | | TBD | Call TI | Call TI | -40 to 125 | T75BQ | |
| TMP75BQDRQ1 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | T75BQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TMP75B-Q1 :**

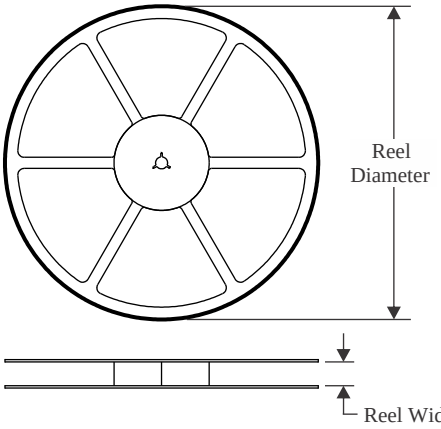
- Catalog : TMP75B

NOTE: Qualified Version Definitions:

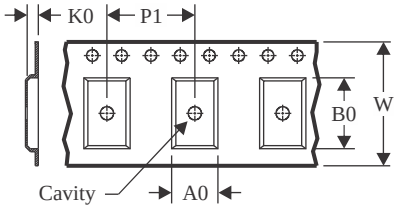
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

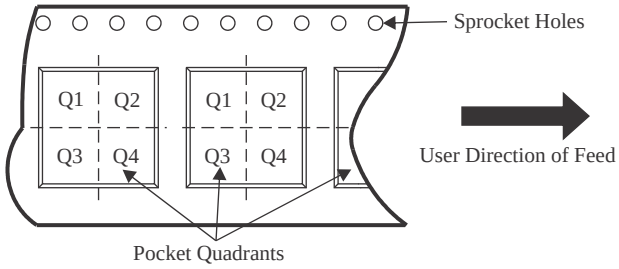



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

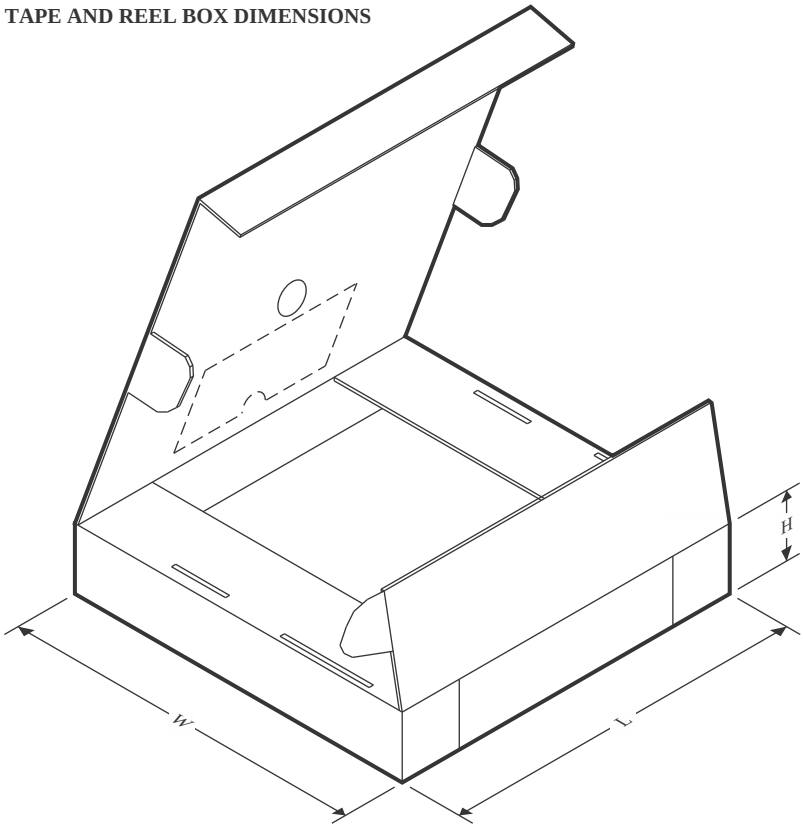
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

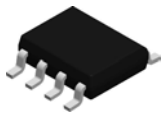
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMP75BQDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TMP75BQDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMP75BQDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TMP75BQDRQ1 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |

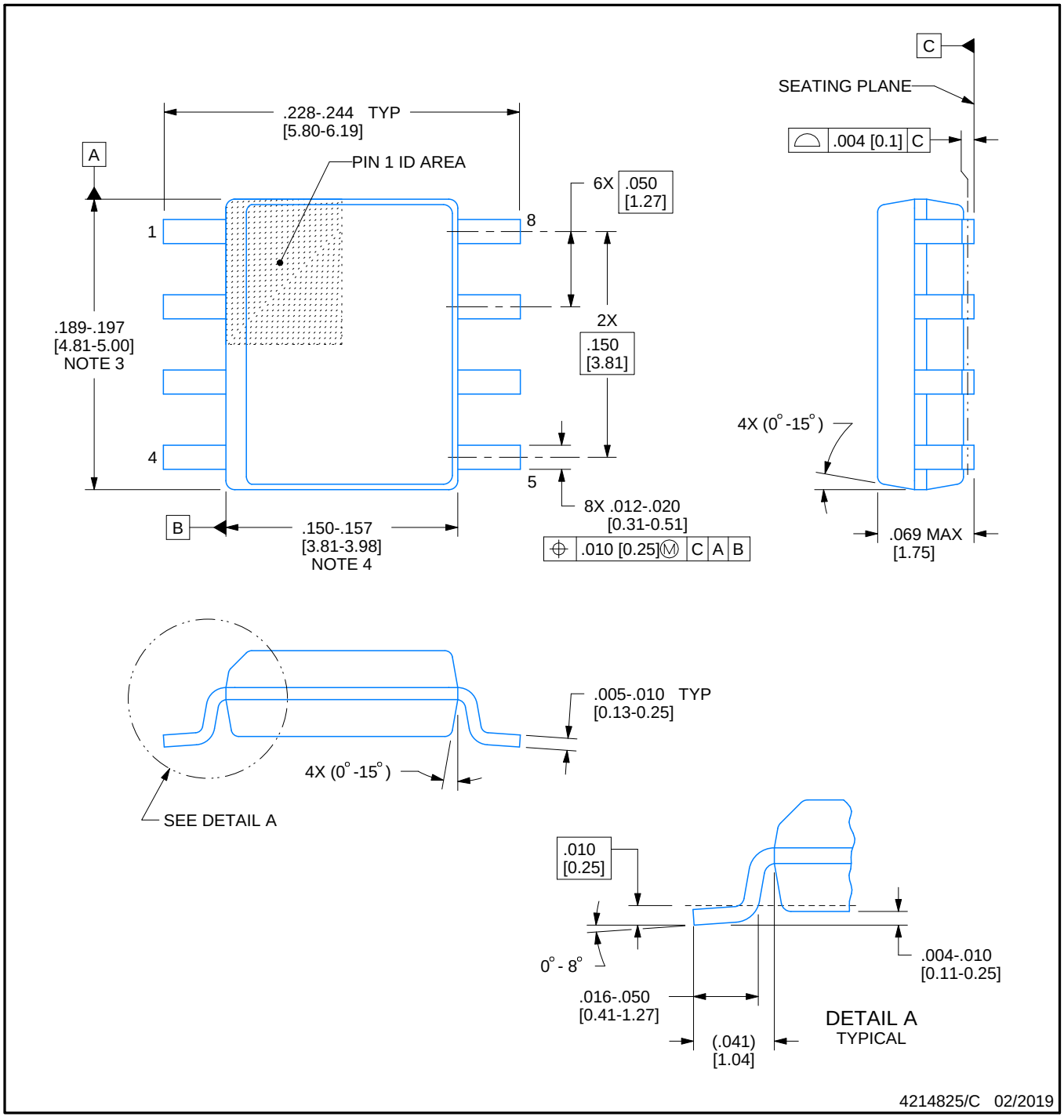


# PACKAGE OUTLINE

## D0008A

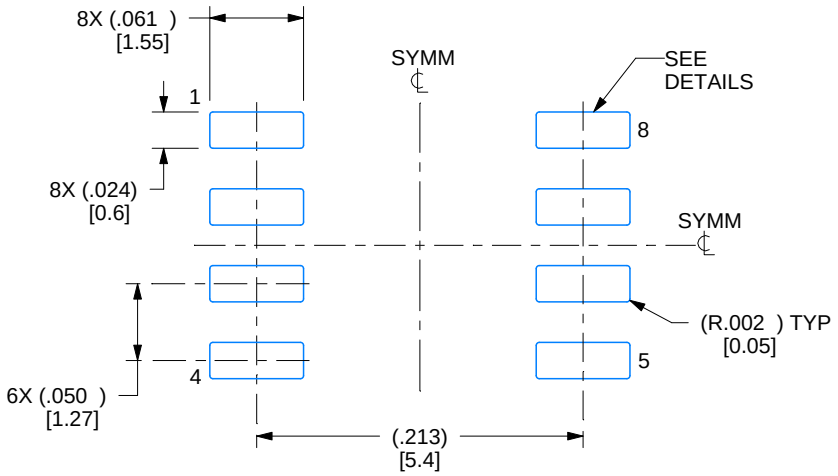
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

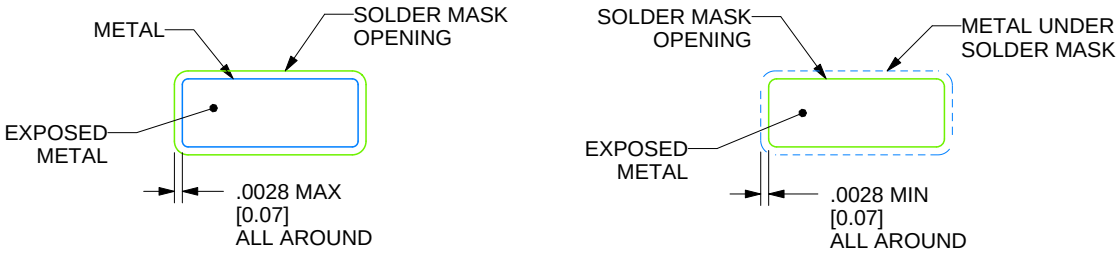



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

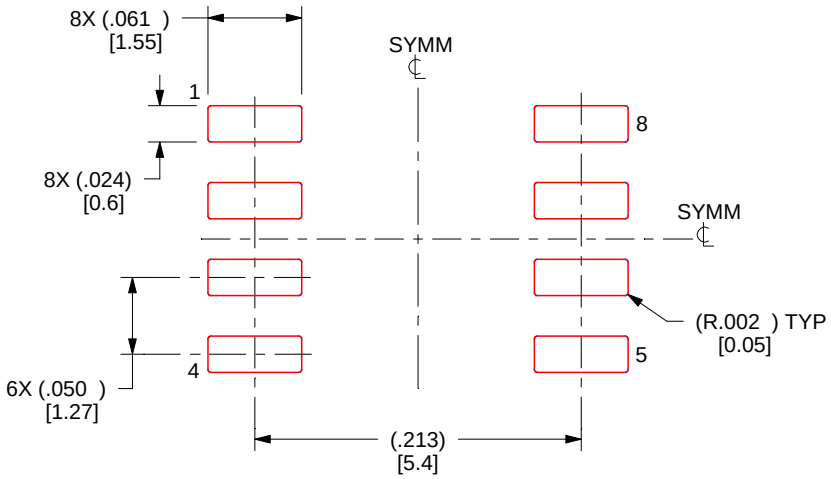
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

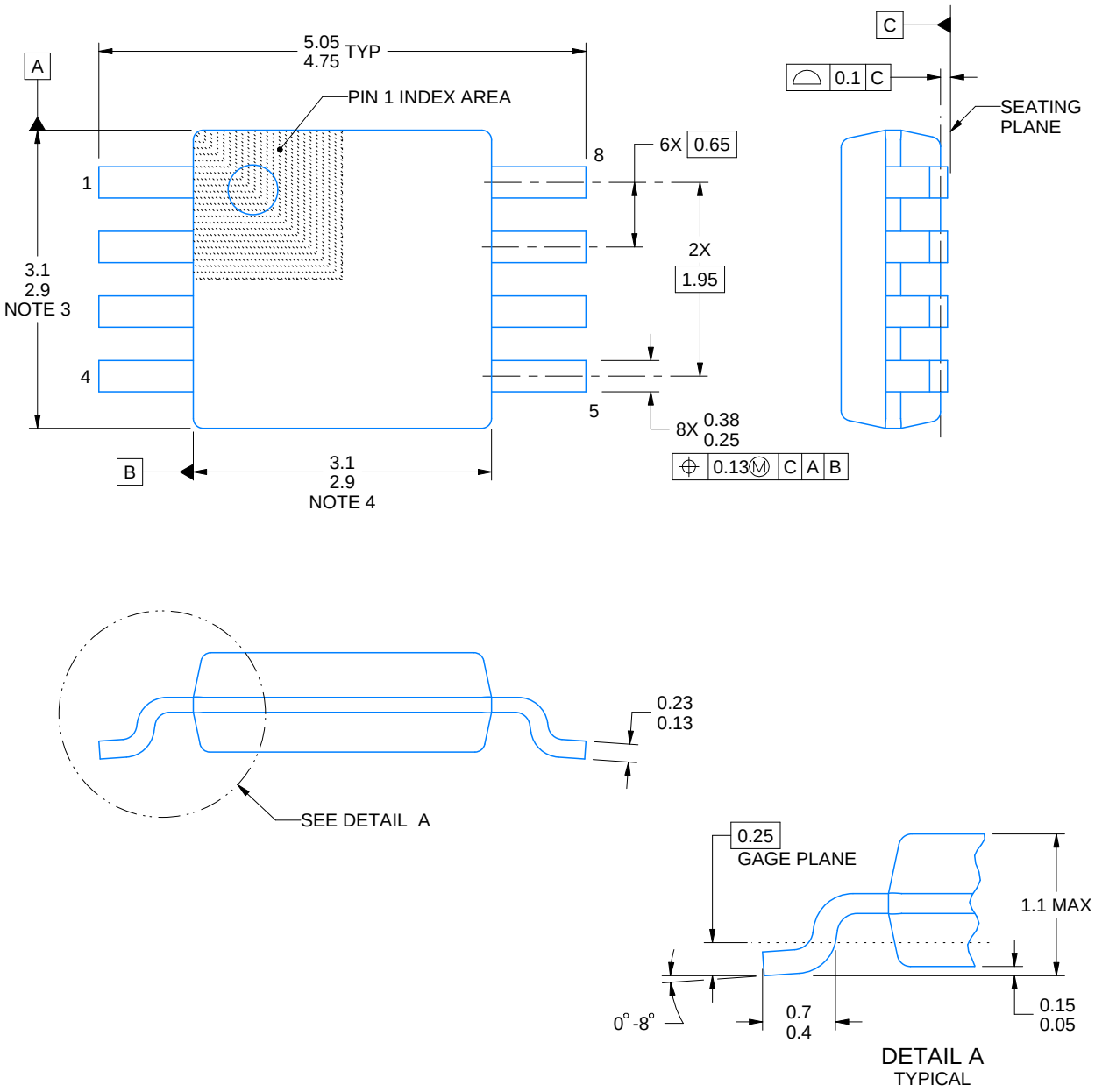
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGK0008A

## VSSOP - 1.1 mm max height

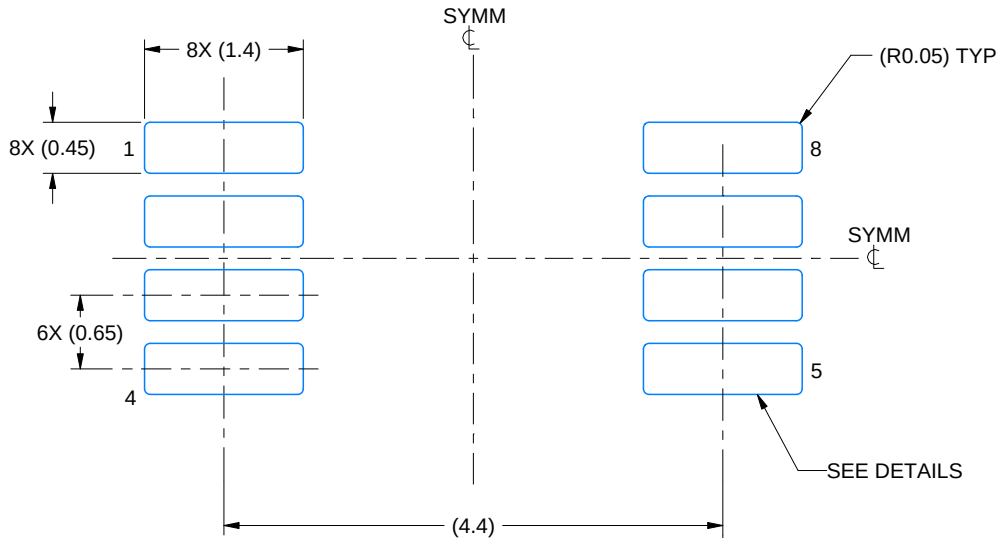
SMALL OUTLINE PACKAGE



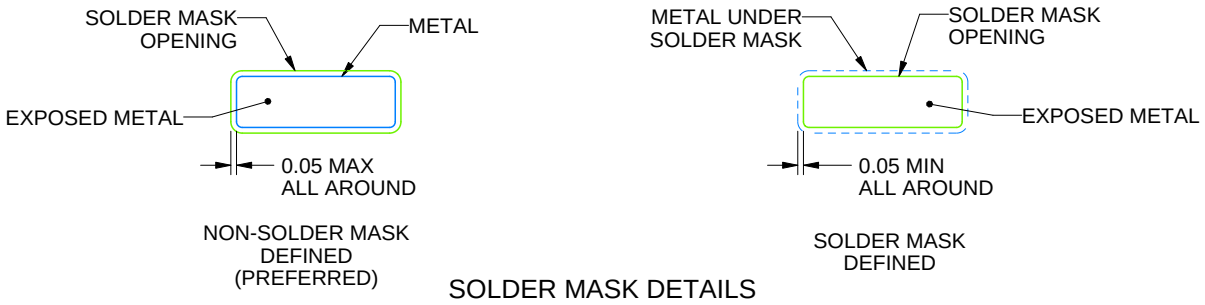

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

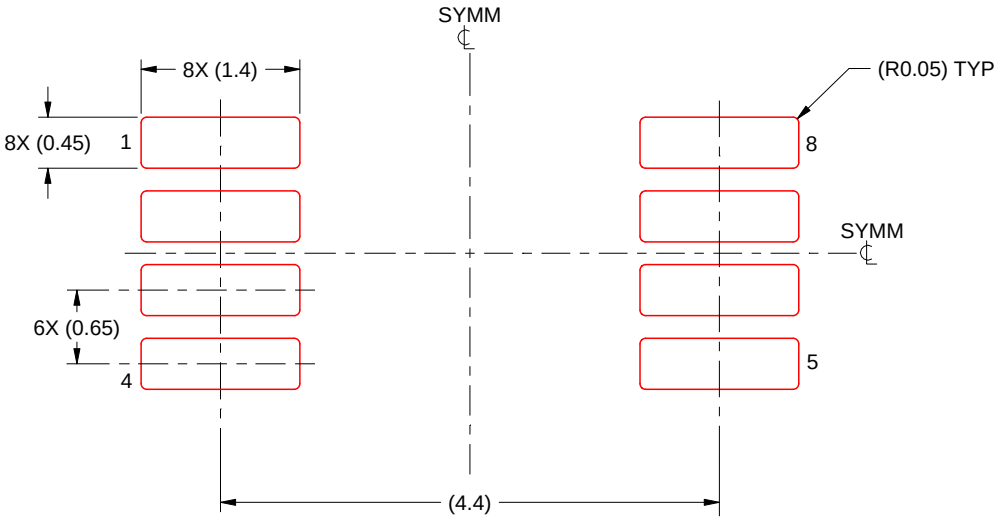



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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