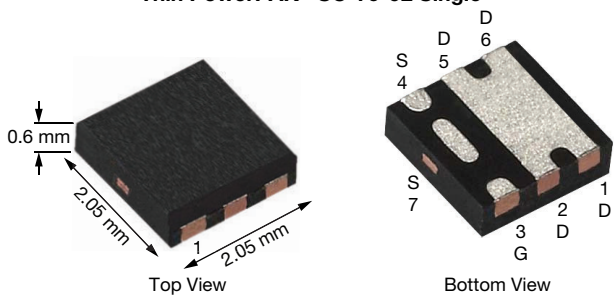
P-Channel 12 V (D-S) MOSFET

Thin PowerPAK® SC-70-6L Single



Marking code: B7

FEATURES

- TrenchFET® Gen III p-channel power MOSFET
- Thermally enhanced PowerPAK® SC-70 package
  - Small footprint area
  - Low on-resistance
- 100 % R_g tested
- $R_{DS(on)}$ rating at V_{GS} = -1.8 V
- Built in ESD protection with Zener diode
- Typical ESD performance: 3500 V
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

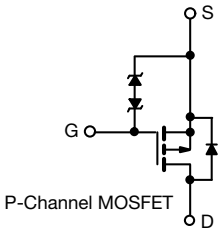
Pb-free

RoHS COMPLIANT

HALOGEN FREE

APPLICATIONS

- Smart phones, tablet PCs, mobile computing
  - Battery switch
  - Charger switch
  - Load switch



PRODUCT SUMMARY	
V_{DS} (V)	-12
$R_{DS(on)}$ max. (Ω) at V_{GS} = -4,5 V	0.0130
$R_{DS(on)}$ max. (Ω) at V_{GS} = -3.7 V	0.0145
$R_{DS(on)}$ max. (Ω) at V_{GS} = -2.5 V	0.0190
$R_{DS(on)}$ max. (Ω) at V_{GS} = -1.8 V	0.0320
Q_g typ. (nC)	33
I_D (A)	-12
Configuration	Single

ORDERING INFORMATION	
Package	Thin PowerPAK SC-70-6L
Lead (Pb)-free and halogen-free	SiA477EDJT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-12	V
Gate-source voltage		V_{GS}	± 8	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	-12 [a]	A
	T_C = 70 °C		-12 [a]	
	T_A = 25 °C		-12 [a, b, c]	
	T_A = 70 °C		-11 [b, c]	
Pulsed drain current (t = 100 µs)		I_{DM}	-50	
Continuous source-drain diode current	T_C = 25 °C	I_S	-12 [a]	
	T_A = 25 °C		-2.9 [b, c]	
Maximum power dissipation	T_C = 25 °C	P_D	19	W
	T_C = 70 °C		12	
	T_A = 25 °C		3.5 [b, c]	
	T_A = 70 °C		2.2 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [b, f]	t ≤ 5 s	R_{thJA}	28	36	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	5.3	6.5	

Notes

a. Package limited
b. Surface mounted on 1" x 1" FR4 board
c. t = 5 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 80 °C/W

For technical questions, contact: pmostechsupport@vishay.com

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-12	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = -250 µA	-	-3.9	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	2.5	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-0.4	-	-1	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V	-	-	± 12	µA
		V_{DS} = 0 V, V_{GS} = ± 4.5 V	-	-	± 1	
Zero gate voltage drain current	I_{DSS}	V_{DS} = -12 V, V_{GS} = 0 V	-	-	-1	
		V_{DS} = -12 V, V_{GS} = 0 V, T_J = 55 °C	-	-	-10	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≤ -5 V, V_{GS} = -4.5 V	-20	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -4.5 V, I_D = -5 A	-	0.0110	0.0130	Ω
		V_{GS} = -3.7 V, I_D = -5 A	-	0.0114	0.0145	
		V_{GS} = -2.5 V, I_D = -3 A	-	0.0145	0.0190	
		V_{GS} = -1.8 V, I_D = -1 A	-	0.0228	0.0320	
Forward transconductance [a]	g_{fs}	V_{DS} = -6 V, I_D = -5 A	-	30	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = -6 V, V_{GS} = 0 V, f = 1 MHz	-	3050	-	pF
Output capacitance	C_{oss}		-	725	-	
Reverse transfer capacitance	C_{rss}		-	740	-	
Total gate charge	Q_g	V_{DS} = -6 V, V_{GS} = -10 V, I_D = -10 A	-	55	83	nC
		V_{DS} = -6 V, V_{GS} = -4.5 V, I_D = -10 A	-	33	50	
Gate-source charge	Q_{gs}		-	4.3	-	
Gate-drain charge	Q_{gd}		-	8.9	-	
Gate resistance	R_g	f = 1 MHz	1.2	6	12	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = -6 V, R_L = 1 Ω I_D ≅ -10 A, V_{GEN} = -4.5 V, R_g = 1 Ω	-	25	50	ns
Rise time	t_r		-	25	50	
Turn-off delay time	$t_{d(off)}$		-	70	140	
Fall time	t_f		-	50	100	
Turn-on delay time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 1 Ω I_D ≅ -10 A, V_{GEN} = -8 V, R_g = 1 Ω	-	10	20	
Rise time	t_r		-	20	40	
Turn-off delay time	$t_{d(off)}$		-	90	180	
Fall time	t_f		-	46	90	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	-12	A
Pulse diode forward current	I_{SM}		-	-	-50	
Body diode voltage	V_{SD}	I_S = -10 A, V_{GS} = 0 V	-	-0.8	-1.2	V
Body diode reverse recovery time	t_{rr}	I_F = -10 A, di/dt = 100 A/µs, T_J = 25 °C	-	60	120	ns
Body diode reverse recovery charge	Q_{rr}		-	39	80	nC
Reverse recovery fall time	t_a		-	22	-	ns
Reverse recovery rise time	t_b		-	38	-	

Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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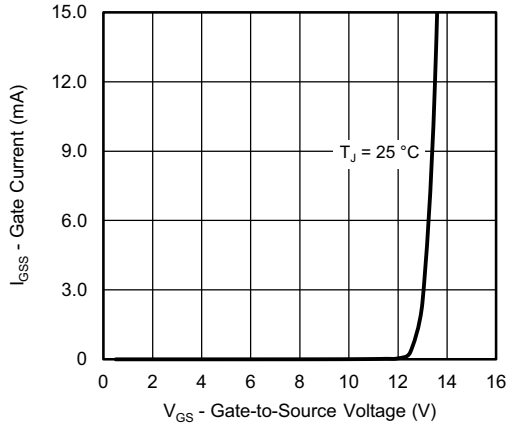
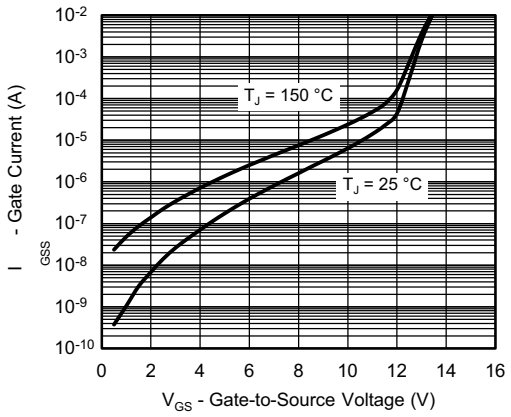


Gate Current vs. Gate-Source Voltage



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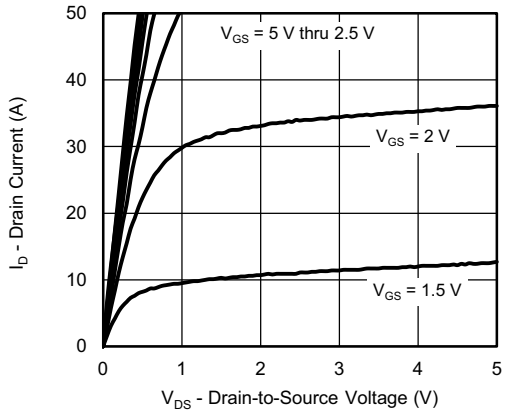
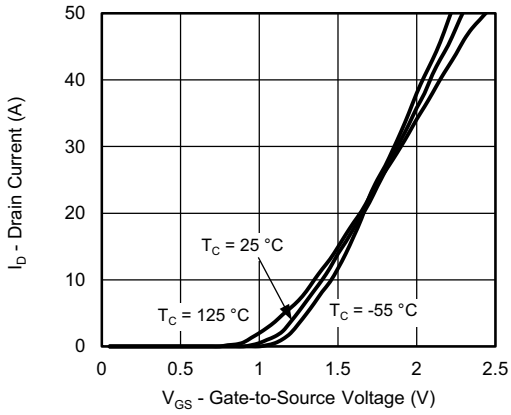
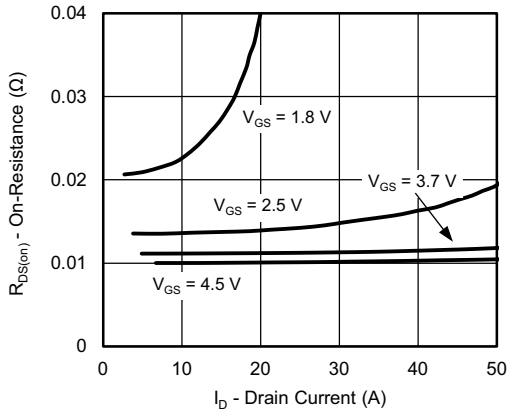


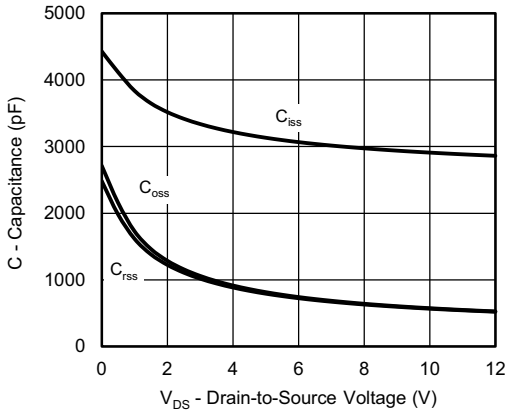
Output Characteristics



Transfer Characteristics



On-Resistance vs. Drain Current



Capacitance

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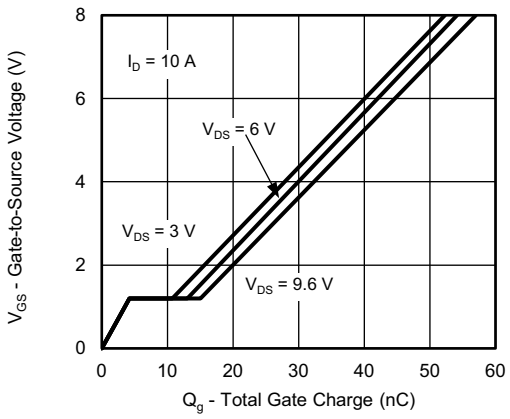
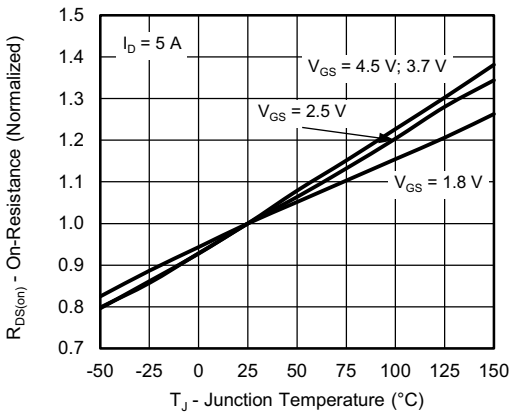
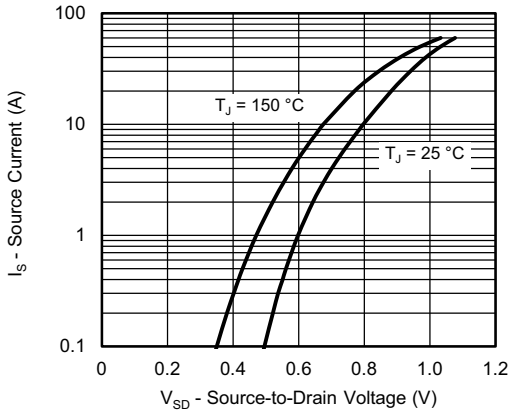


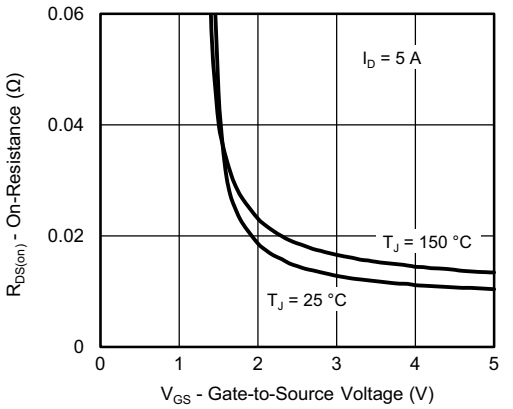
Gate Charge



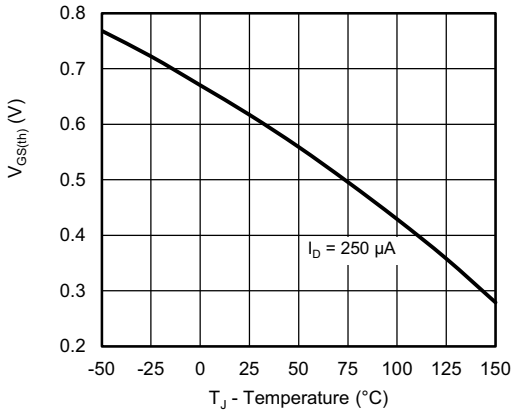
On-Resistance vs. Junction Temperature



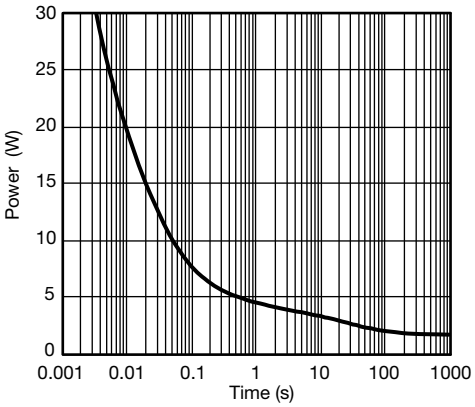
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

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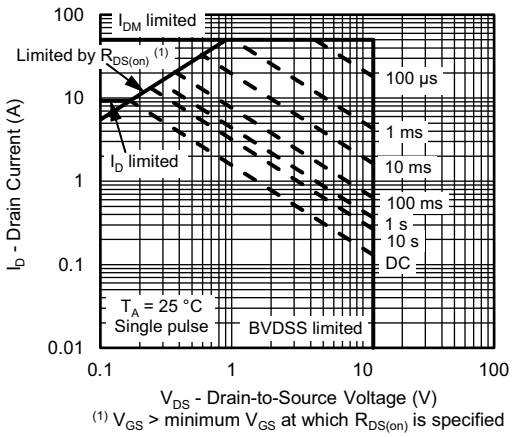
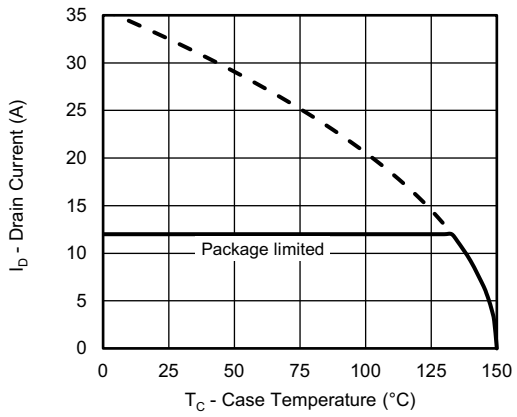
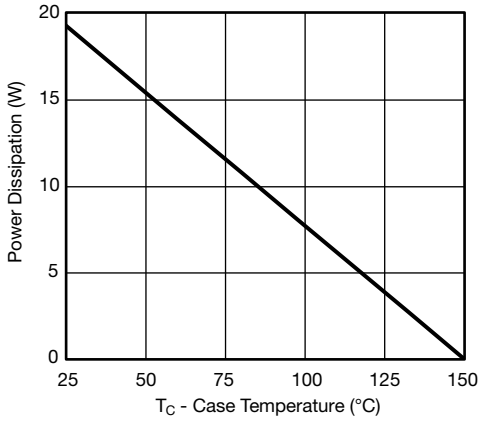


Safe Operating Area, Junction-to-Ambient



Current Derating [a]



Power Derating

Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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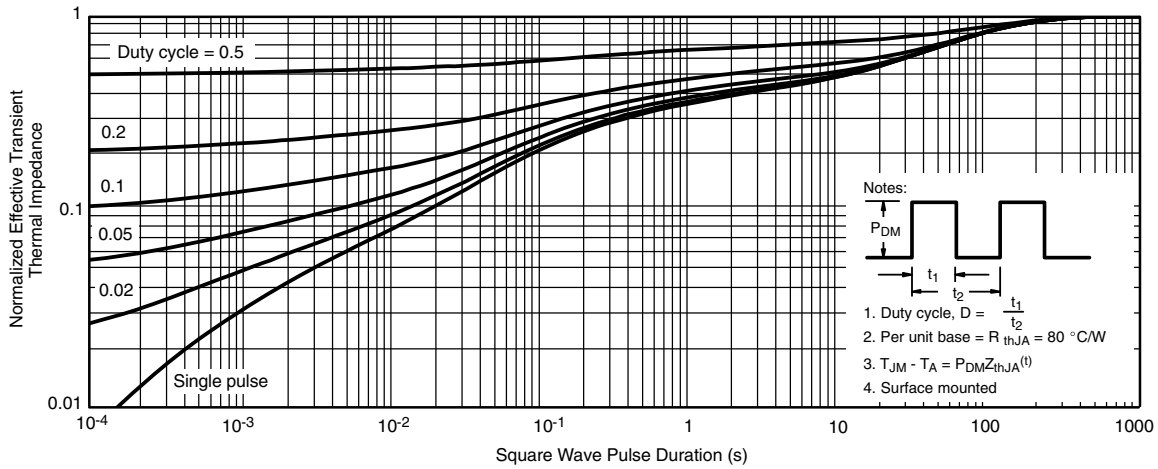
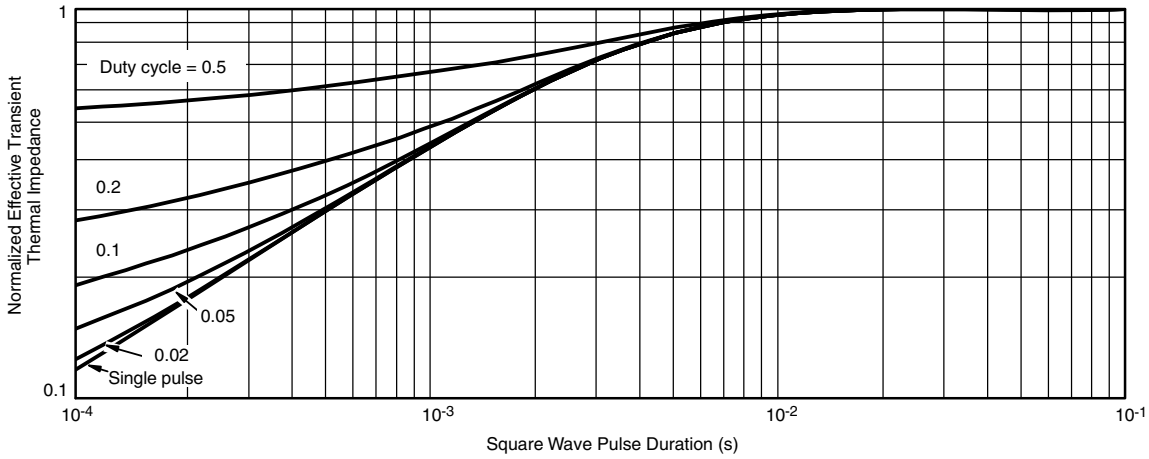


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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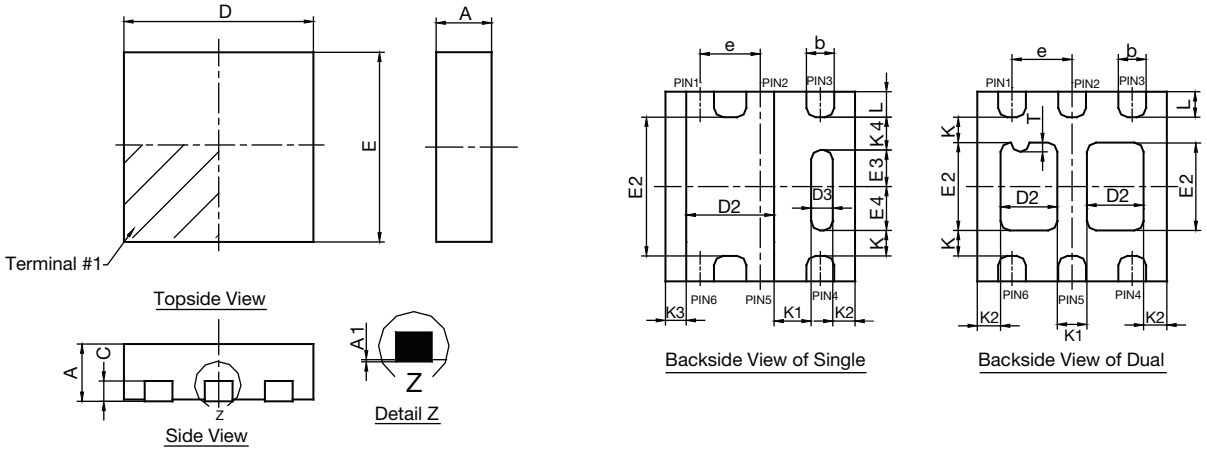
Case Outline for PowerPAK® SC70T



DIM.	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.525	0.60	0.65	0.0206	0.024	0.026	0.525	0.60	0.65	0.0206	0.024	0.026
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D2	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D3	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E2	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E3	0.345	0.395	0.445	0.014	0.016	0.018						
E4	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP.			0.011 TYP.			0.275 TYP.			0.011 TYP.		
K1	0.400 TYP.			0.016 TYP.			0.320 TYP.			0.013 TYP.		
K2	0.240 TYP.			0.009 TYP.			0.252 TYP.			0.010 TYP.		
K3	0.225 TYP.			0.009 TYP.								
K4	0.355 TYP.			0.014 TYP.								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C12-0160-Rev. B, 05-Mar-12 DWG: 5994												

Notes

1. All dimensions are in millimeter. Millimeters will govern.
2. Package outline exculsive of mold flash and metal burr.
3. Package outline inclusive of plating

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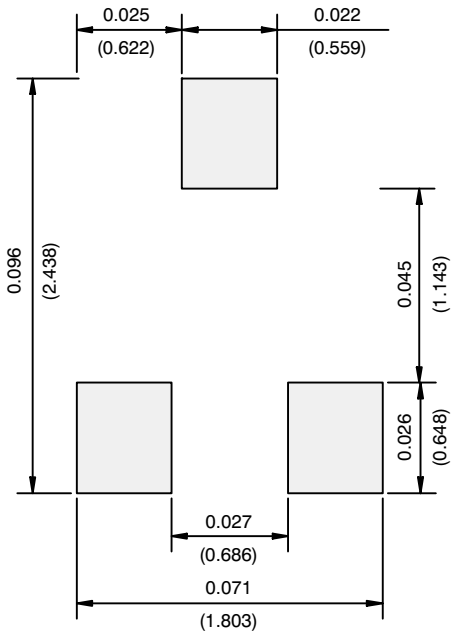
RECOMMENDED MINIMUM PADS FOR SC-70: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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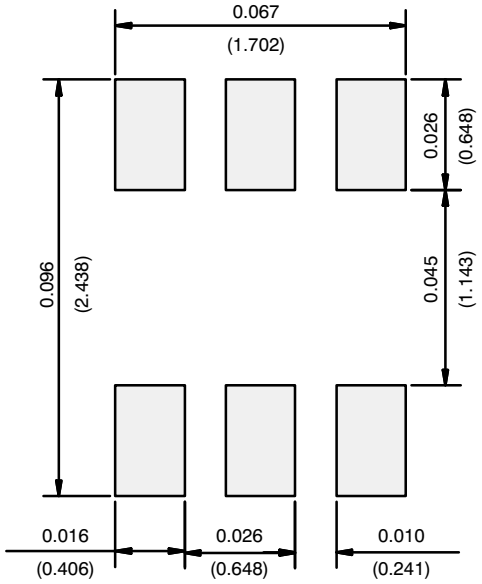
APPLICATION NOTE

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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